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CENTRAL DISTRICT OF CALIFORNIA
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United States Court of Appeals for the Federal Circuit

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Plaintiff-Appellee

v.

BROADCOM LIMITED, NKA BROADCOM INC., BROADCOM CORPORATION, AVAGO TECHNOLOGIES LIMITED, NKA AVAGO TECHNOLOGIES INTERNATIONAL SALES PTE. LIMITED, APPLE INC.,
Defendants-Appellants

2020-2222, 2021-1527

Appeals from the United States District Court for the Central District of California in No. 2:16-cv-03714-GW-AGR, Judge George H. Wu.

Decided: February 4, 2022

KATHLEEN M. SULLIVAN, Quinn Emanuel Urquhart & Sullivan, LLP, Los Angeles, CA, argued for plaintiff-appellee. Also represented by JAMES R. ASPERGER; BRIAN P. BIDDINGER, EDWARD J. DEFRANCO, New York, NY; TODD MICHAEL BRIGGS, KEVIN P.B. JOHNSON, Redwood Shores, CA; DEREK L. SHAFFER, Washington, DC; KEVIN ALEXANDER SMITH, San Francisco, CA.

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WILLIAM F. LEE, Wilmer Cutler Pickering Hale and Dorr LLP, Boston, MA, argued for defendants-appellants. Also represented by LAUREN B. FLETCHER, MADELEINE C. LAUPHEIMER, JOSEPH J. MUELLER; STEVEN JARED HORN, DAVID P. YIN, Washington, DC; MARK D. SELWYN, Palo Alto, CA.

Before LOURIE, LINN, and DYK, *Circuit Judges*.

Opinion for the Court filed by *Circuit Judge* LINN.

Opinion concurring-in-part and dissenting-in-part filed by *Circuit Judge* DYK.

LINN, *Circuit Judge*.

Broadcom Limited, Broadcom Corporation, and Avago Technologies Ltd. (collectively "Broadcom") and Apple Inc. ("Apple") appeal from the adverse decision of the District Court for the Central District of California in an infringement suit filed by the California Institute of Technology ("Caltech") for infringement of its U.S. Patents No. 7,116,710 ("the '710 patent"), No. 7,421,032 ("the '032 patent"), and No. 7,916,781 ("the '781 patent").

Because the district court did not err in its construction of the claim limitation "repeat" and because substantial evidence supports the jury's verdict of infringement of the asserted claims of the '710 and '032 patents, we affirm the district court's denial of JMOL on infringement thereof. We also affirm the district court's conclusion that claim 13 of the '781 patent is patent-eligible but vacate the jury's verdict of infringement thereof because of the district court's failure to instruct the jury on the construction of the claim term "variable number of subsets." We thus remand for a new trial on infringement of claim 13 of the '781 patent. We further affirm the district court's summary judgment findings of no invalidity based on IPR estoppel and its determination of no inequitable conduct. We affirm the

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district court's decision with respect to its jury instructions on extraterritoriality. But because Caltech's two-tier damages theory cannot be supported on this record, we vacate the jury's damages award and remand for a new trial on damages.

BACKGROUND

I. The Caltech Patents

Caltech's '710 and '032 patents disclose circuits that generate and receive irregular repeat and accumulate ("IRA") codes, a type of error correction code designed to improve the speed and reliability of data transmissions. Wireless data transmissions are ordinarily susceptible to corruption arising from noise or other forms of interference. IRA codes help to identify and correct corruption after it occurs.

The encoding process begins with the processing of data before it is transmitted. The data consists of information bits in the form of 1's and 0's. The information bits are input into an encoder, a device that generates codewords comprised of parity bits and the original information bits. Parity bits are appended at the end of a codeword. Codewords are created in part by repeating information bits in order to increase the transmission's reliability. When noise or other forms of interference introduce errors into the codewords during transmission, the decoder identifies these errors and relies on the codeword's redundant incorporation of the original string of information bits to correct and eliminate the errors.

Before Caltech's patents, error correction codes had already incorporated repetition and irregular repetition. These codes, however, were less than optimally efficient because they were either encoded or decoded in quadratic time, which meant that the number of computations

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required to correct a given number of bits far exceeded the number of bits ultimately corrected.

In the '710 and '032 patents, the IRA codes are linear-time encodable and decodable, rather than quadratic. '710 patent, col. 2, ll. 6–7 ("The encoded data output from the inner coder may be transmitted on a channel and decoded in linear time."); *id.* col. 2, l. 59 ("The inner coder 206 may be a linear rate-1 coder."); *id.* col. 3, ll. 25–26 ("An IRA code is a linear code."). Using a linear code means that the relationship between the bits corrected and the computations required is directly proportional. Minimizing the number of calculations that an encoder or decoder must perform permits smaller, more efficient chips with lower power requirements.

The claimed improvement involves encoding the information bits through a process of irregular repetition, scrambling, summing, and accumulation. Repeating inputted information bits is necessary to increase the reliability of data transmissions, and irregular repetition minimizes the number of times that information bits are repeated. Minimizing the number of times that an information bit is repeated is crucial to the efficiency of the claimed inventions because the repetitions impact the device's coding rate or speed, as well as the code's complexity. The fewer repeated bits there are, the fewer number of computations that an encoder must perform, which in turn permits smaller circuits, decreased power requirements, and decreased operating temperatures in devices incorporating the circuits.

The claims and accompanying specifications of the Caltech patents make clear that each inputted information bit must be repeated. The parties agree that every claim at issue requires irregular repetition of information bits either explicitly or via the court's construction. This is so even where the irregular repetition is not expressly

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required by the claims. For example, the agreed-upon construction of a Tanner graph in the '032 patent requires that "every message bit is repeated . . . ." J. App'x 33. Furthermore, the claims and accompanying specifications make clear that each bit must be repeated irregularly, stating, for example in the '710 patent, "a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times." '710 patent, col. 2, ll. 53–58.

The '781 patent discloses and claims a method for creating codewords in which "information bits appear in a variable number of subsets." Before trial, Apple and Broadcom sought summary judgment that claim 13 was unpatentable under 35 U.S.C. § 101. After finding that the claims were directed to a patent-eligible subject matter (step 1 of *Alice*[1])—a method of performing error correction and detection encoding with the requirement of irregular repetition—the court declined to reach whether they contained an inventive concept (step 2 of *Alice*). To support patentability, Caltech argued that the "variable number of subsets" language required irregular information bit repetition. The district court agreed and adopted and relied on Caltech's interpretation to deny summary judgment of unpatentability. No party on appeal challenges this claim interpretation.

II. The Accused Products

Caltech alleged infringement by certain Broadcom Wi-Fi chips and Apple products incorporating those chips, including smartphones, tablets, and computers. The accused Broadcom chips were developed and supplied to Apple pursuant to Master Development and Supply Agreements

[1] Alice Corp. Pty. Ltd. v. CLS Bank Int'l, 573 U.S. 208 (2014).

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