

EXHIBIT 4

(12) **United States Patent**
Sasabayashi et al.(10) **Patent No.:** **US 8,044,907 B2**(45) **Date of Patent:** **Oct. 25, 2011**(54) **LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME**(75) Inventors: **Takashi Sasabayashi**, Kawasaki (JP); **Arihiro Takeda**, Sagamihara (JP); **Hiroyasu Inoue**, Kawasaki (JP); **Kazuya Ueda**, Kawasaki (JP); **Yoshio Koike**, Kawasaki (JP); **Hideaki Tsuda**, Kawasaki (JP); **Yasutoshi Tasaka**, Kawasaki (JP); **Hidefumi Yoshida**, Kawasaki (JP); **Kunihiro Tashiro**, Kawasaki (JP); **Tsuyoshi Kamada**, Kawasaki (JP); **Kimiaki Nakamura**, Kawasaki (JP)(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **12/961,009**(22) Filed: **Dec. 6, 2010**(65) **Prior Publication Data**

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Related U.S. Application Data

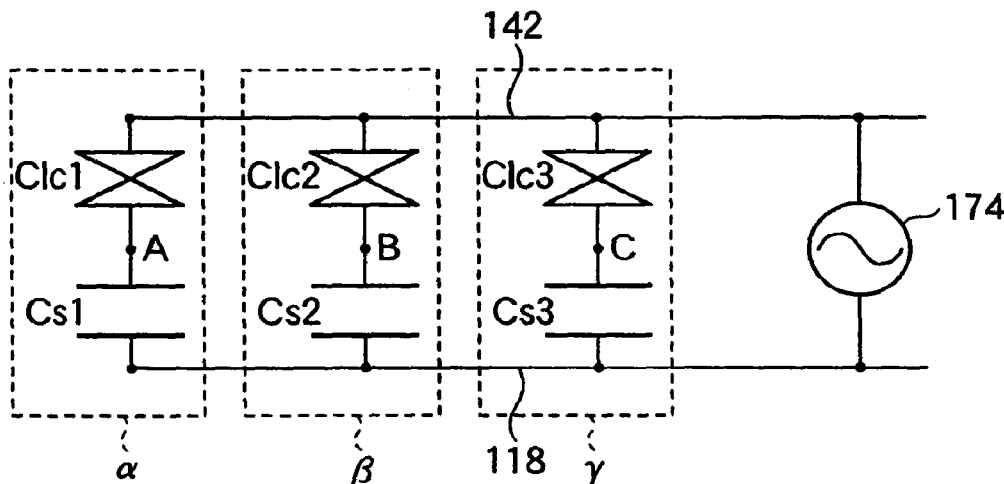
(62) Division of application No. 12/827,030, filed on Jun. 30, 2010, which is a division of application No. 11/299,799, filed on Dec. 12, 2005, now Pat. No. 7,859,500, which is a division of application No. 10/796,783, filed on Mar. 9, 2004, now Pat. No. 7,262,824.

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**
G09G 3/36 (2006.01)(52) **U.S. Cl.** **345/92**; 345/87; 345/89; 345/90; 345/204; 349/42; 349/144(58) **Field of Classification Search** 345/87-100, 345/204, 211-213, 690; 349/42, 43, 144
See application file for complete search history.(56) **References Cited****U.S. PATENT DOCUMENTS**4,840,460 A * 6/1989 Bernot et al. 349/144
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(Continued)*Primary Examiner* — Quan-Zhen Wang*Assistant Examiner* — Jennifer T Nguyen(74) *Attorney, Agent, or Firm* — Greer, Burns & Crain, Ltd.(57) **ABSTRACT**

A liquid crystal display including two substrates, gate bus lines, liquid crystal molecules, and a polymer that determines directions in which the liquid crystal molecules tilt. A plurality of divisional areas are arranged on one of the substrates. The pixels are aligned in a column between drain bus lines. A pixel electrode is formed at each of the divisional areas. A first thin film transistor drives a first divisional area, and a second thin film transistor drives a second divisional area of the same column. The first and second thin film transistors are electrically connected to the same gate bus line. Either the pixel electrodes formed at each of the divisional areas are electrically insulated from each other, or they are connected to each other through a high resistance. A first threshold voltage within the first divisional area is different from a second threshold voltage of the second divisional area.

8 Claims, 57 Drawing Sheets

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FIG.1A

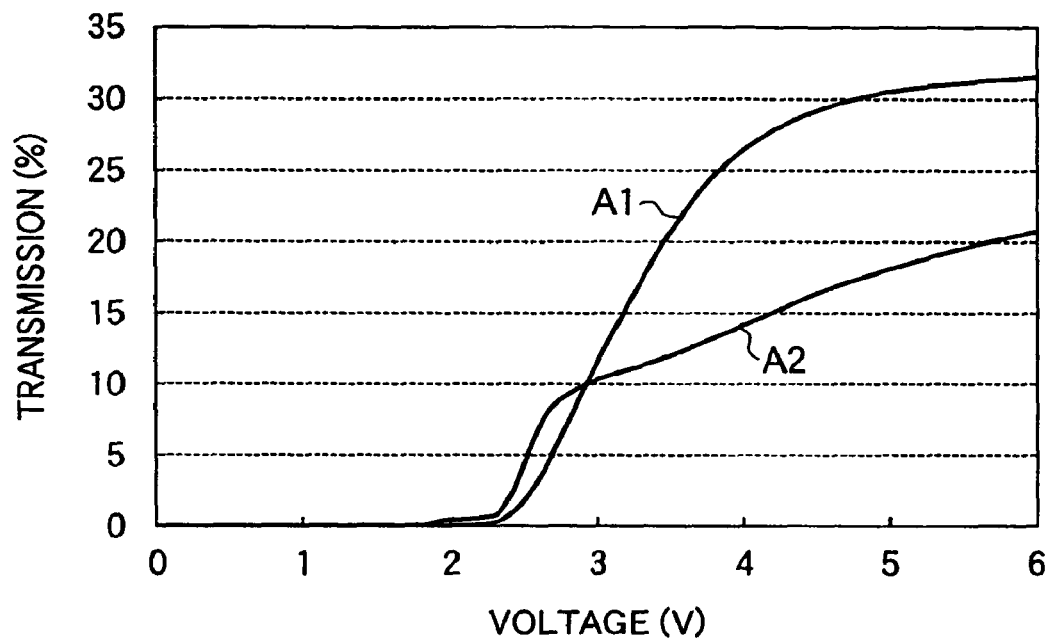


FIG.1B

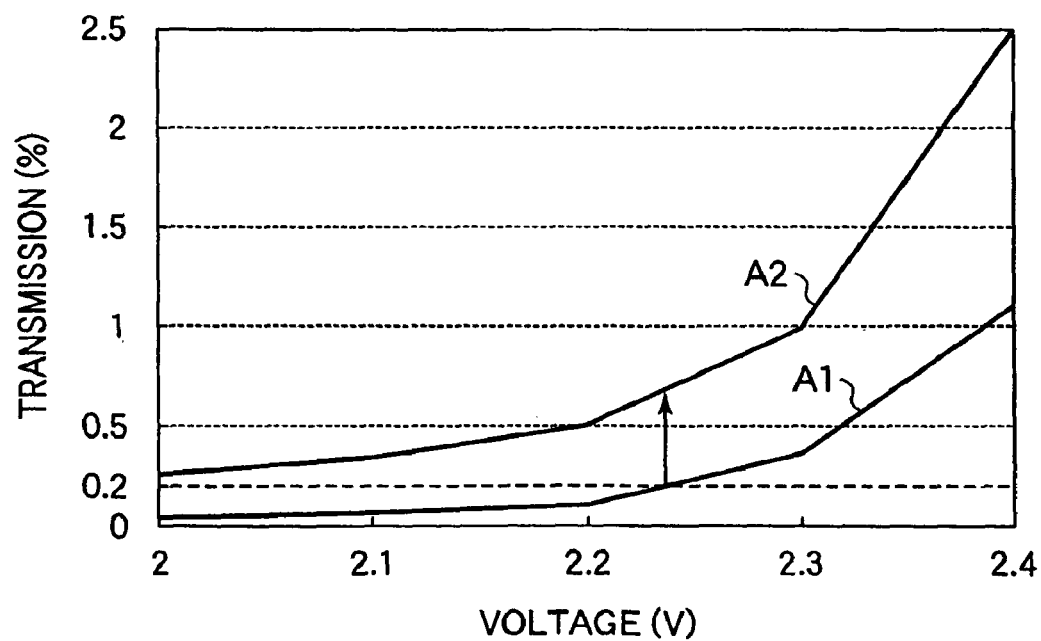


FIG.2

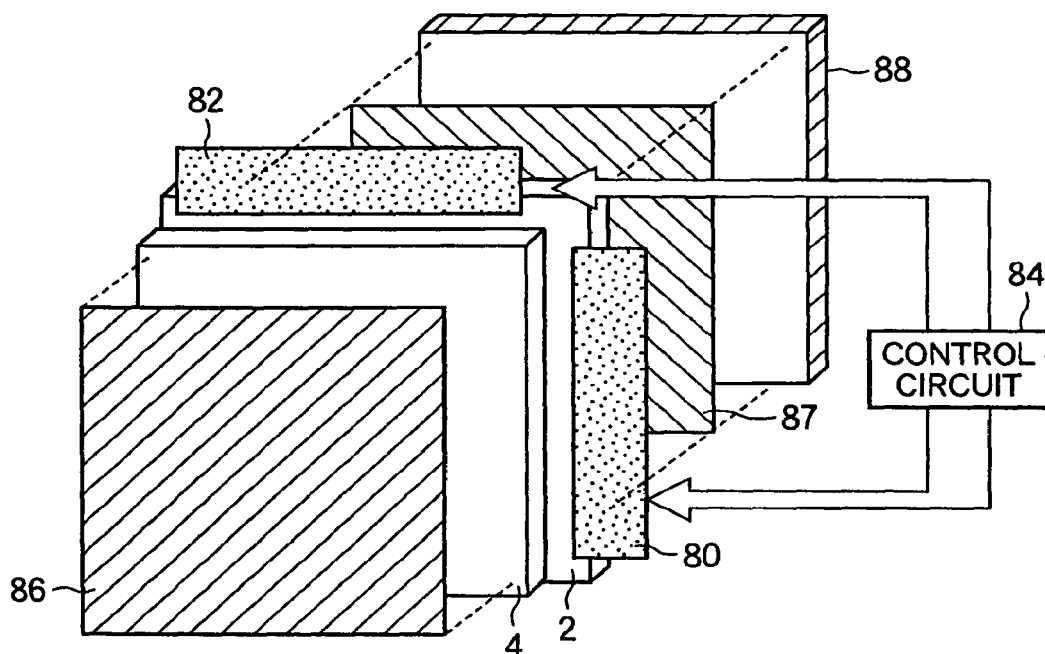
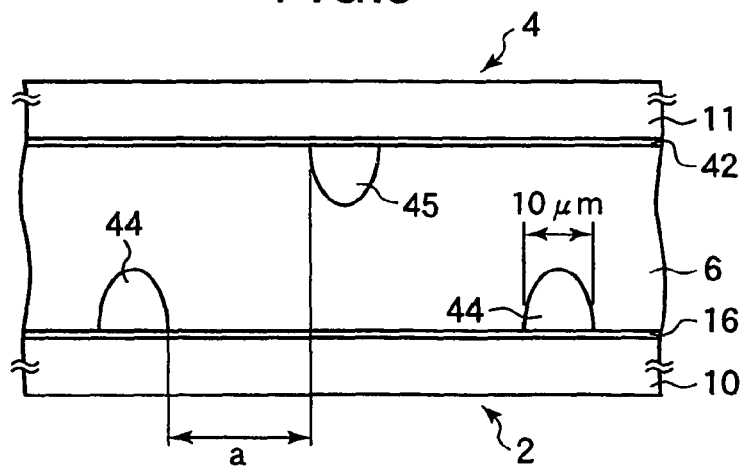


FIG.3



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