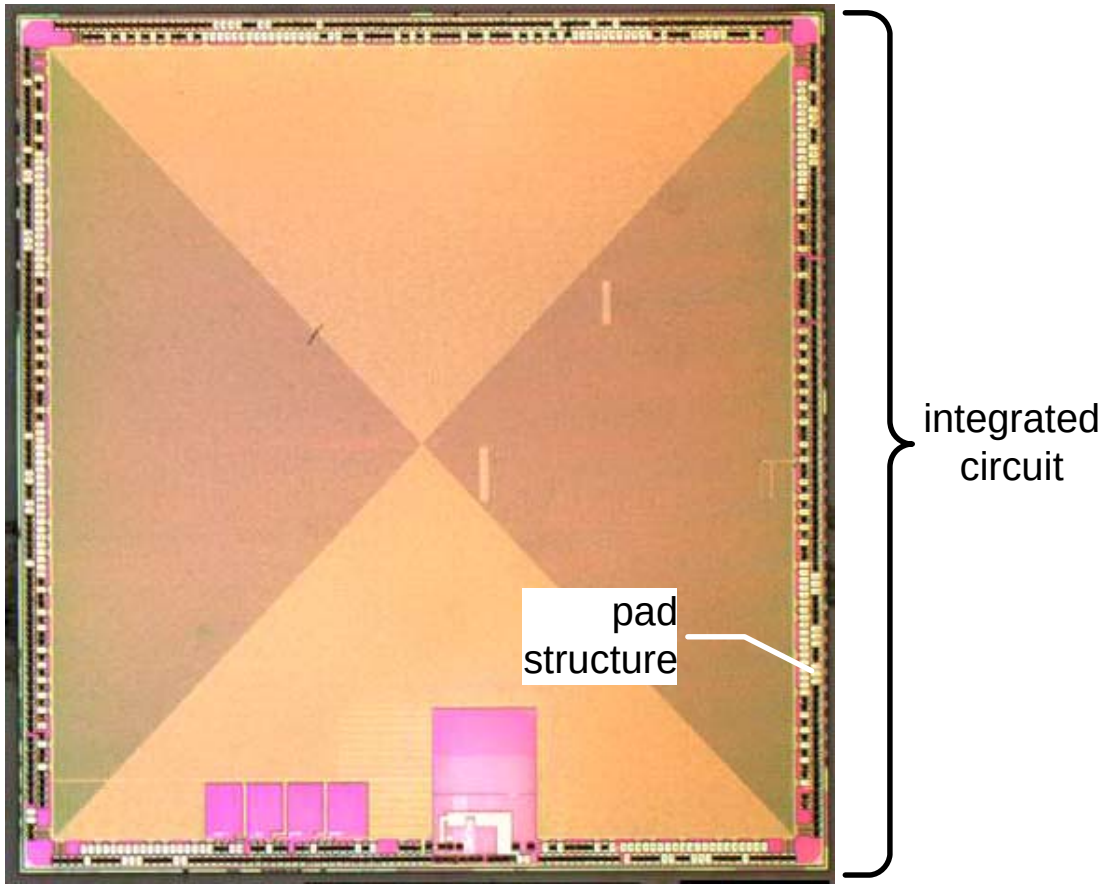
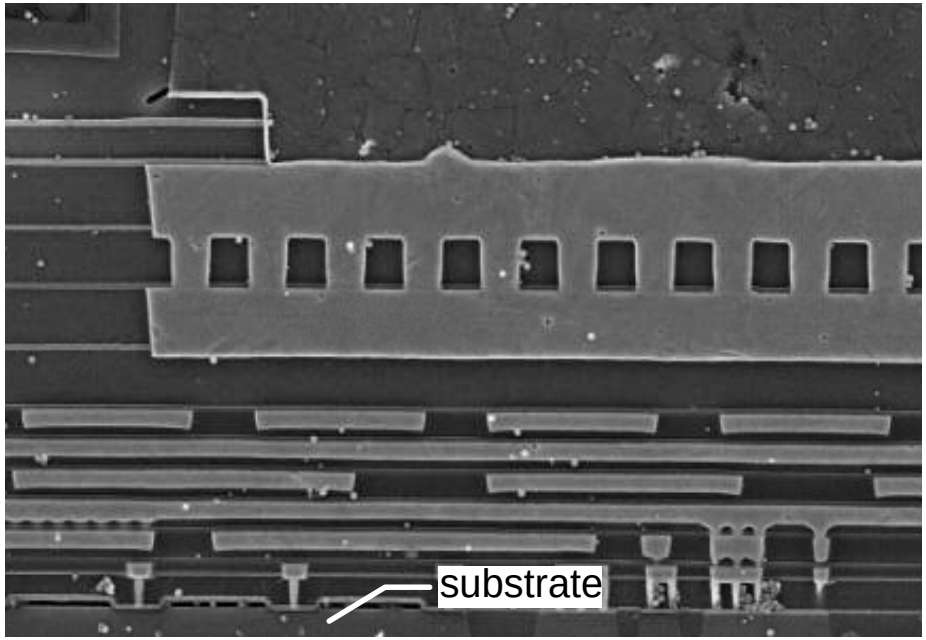
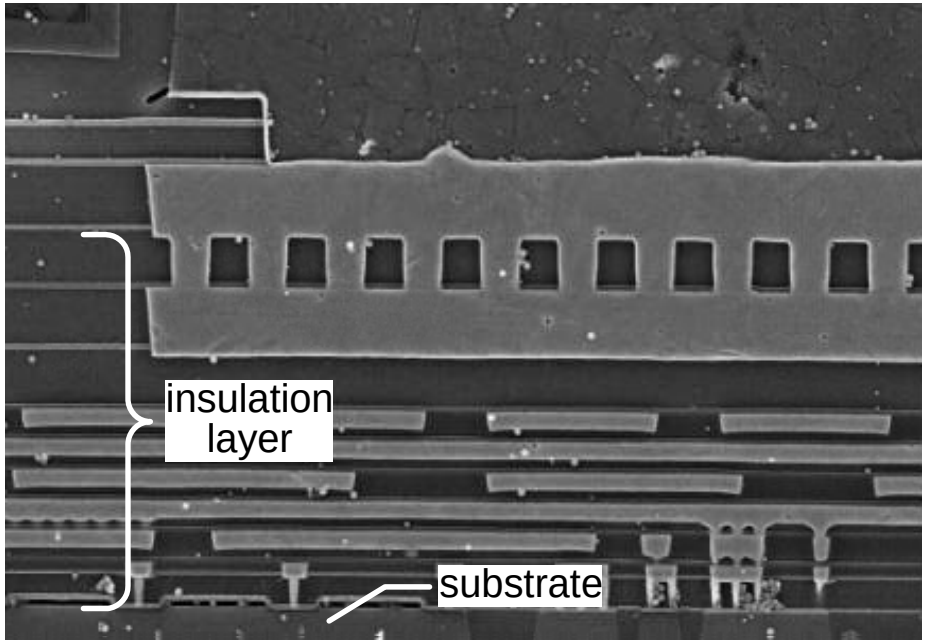
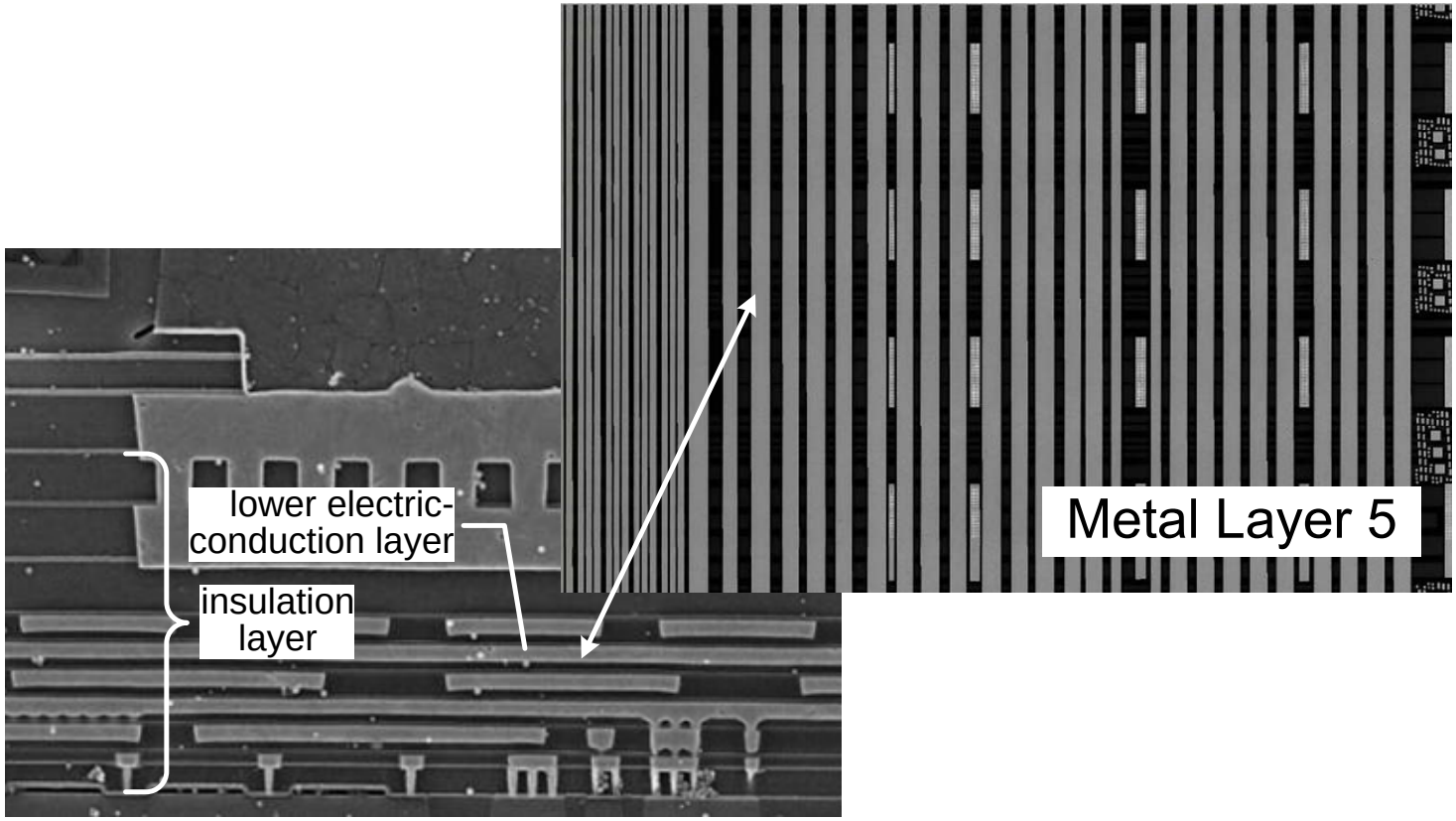
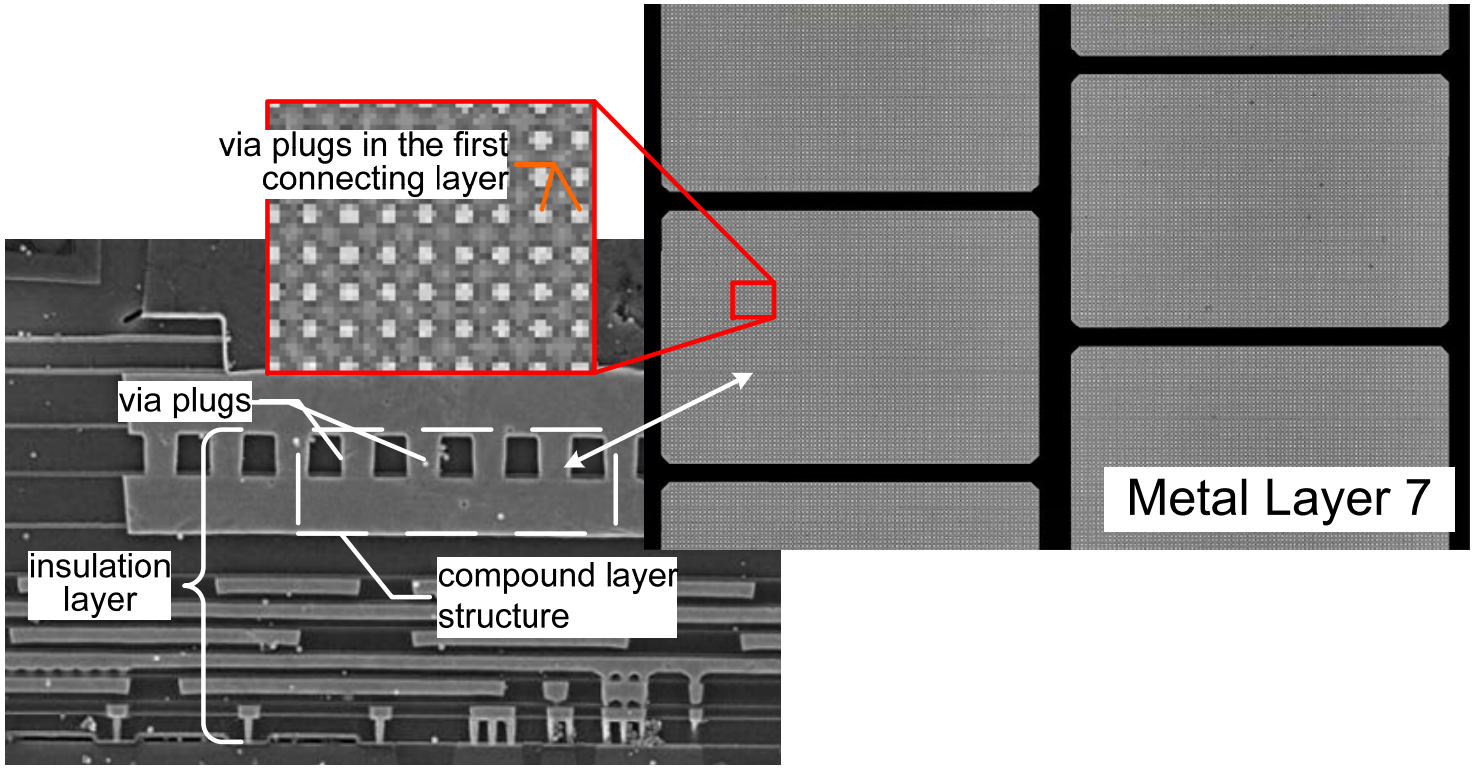
EXHIBIT 10

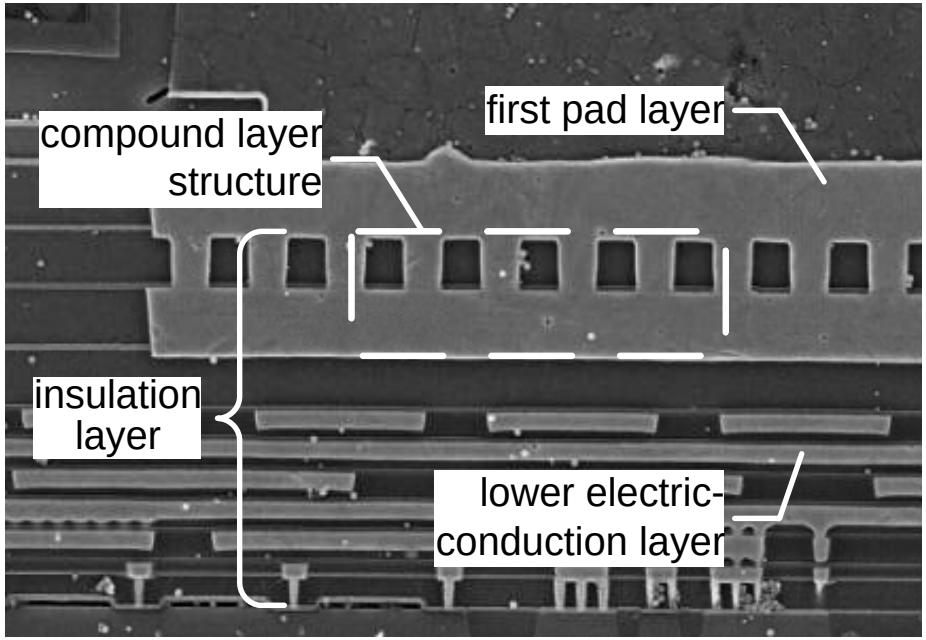
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
1. An integrated circuit (IC) device having a pad structure formed thereon, the IC device comprising:	 The LSI SandForce SF-2281VB1-SDC chip includes an integrated circuit having pad structures formed thereon. The above image of the SF-2281VB1-SDC chip illustrates both the integrated circuit and bond pad structures formed thereon.

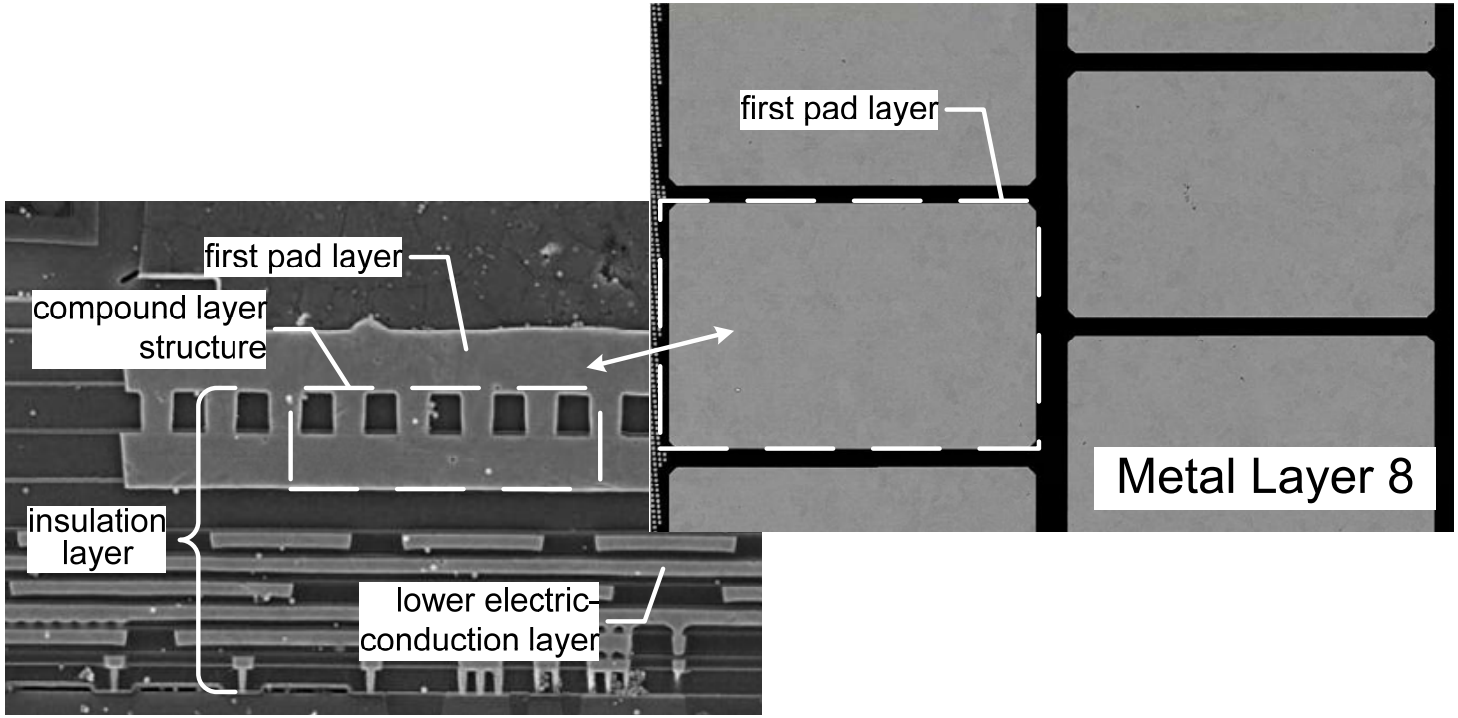
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
a) a substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. An annotation on the lower part of the image indicates the substrate.

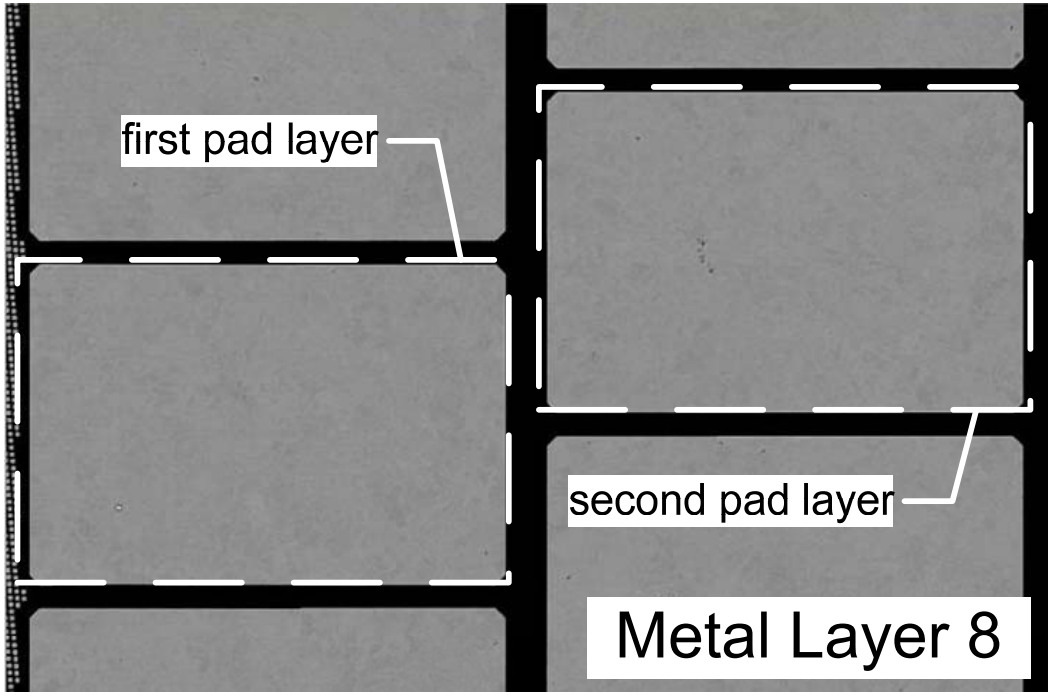
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
b) an insulation layer formed on the substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. The dark portions above the substrate illustrate the insulation layer formed on the substrate in which electric-conduction layers and via layers are formed.

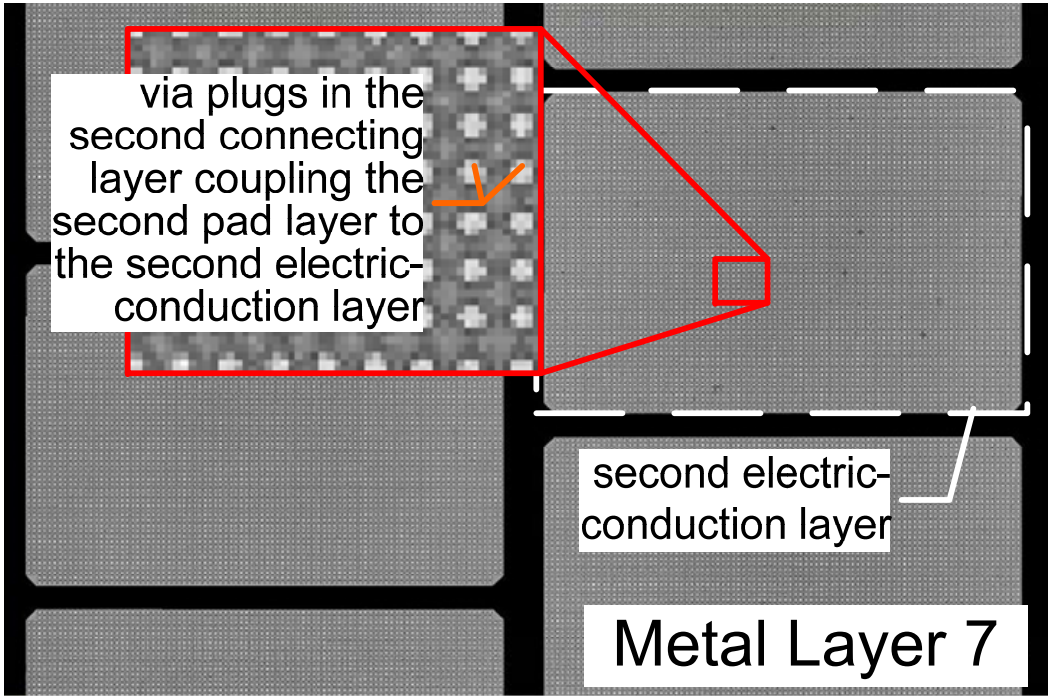
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
c) a lower electric-conduction layer formed in the insulation layer;	 The left side of the above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip with an annotation indicating a lower electric-conduction layer formed in the insulation layer. The right side of the above image shows the metal routing of metal layer 5 of the SF-2281VB1-SDC chip. The double-ended arrow maps the metal routing of layer 5 to the cross section image.

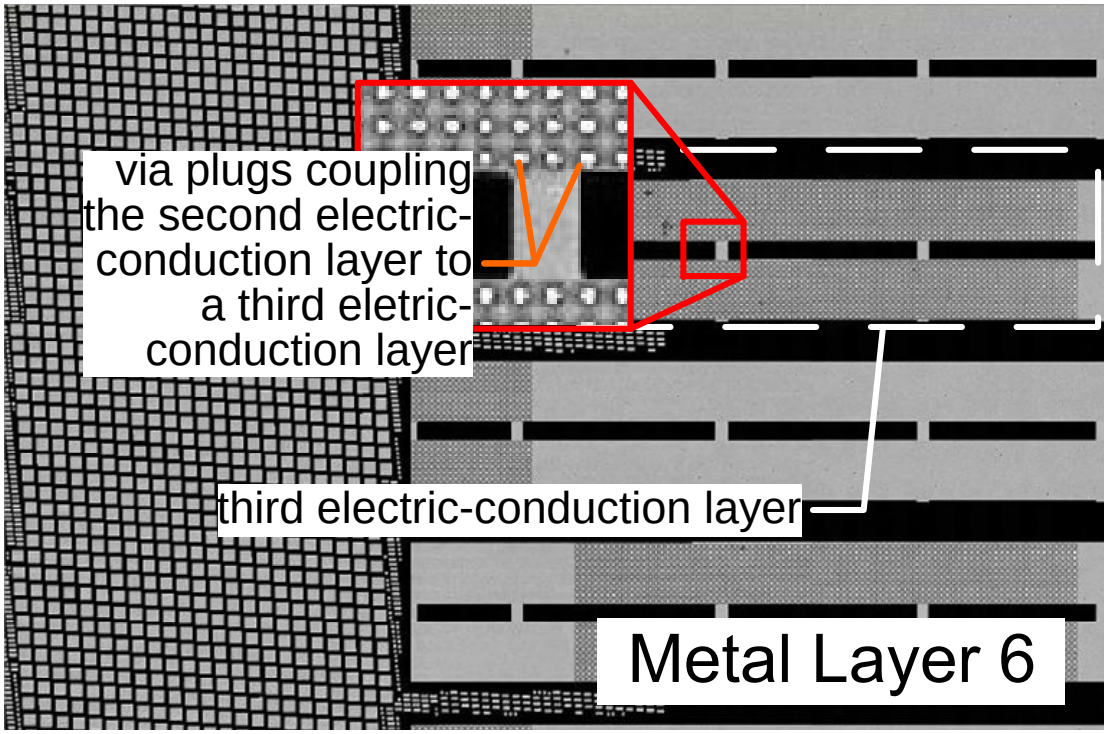
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
d) a compound layer structure formed in the insulation layer;	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. An annotation on the cross section indicates the compound layer structure formed in the insulation layer. The compound layer structure includes both a first electric-conduction layer and a connecting layer including via plugs coupling the first electric-conduction layer to a first pad layer. The right side of the above image shows metal layer 7. The double-ended arrow maps a portion of metal layer 7 to the cross section image. The magnified portion outlined in red shows both the first electric-conduction layer in grey and the via plugs in the first connecting layer that couple the first electric-conduction layer to the first pad layer.

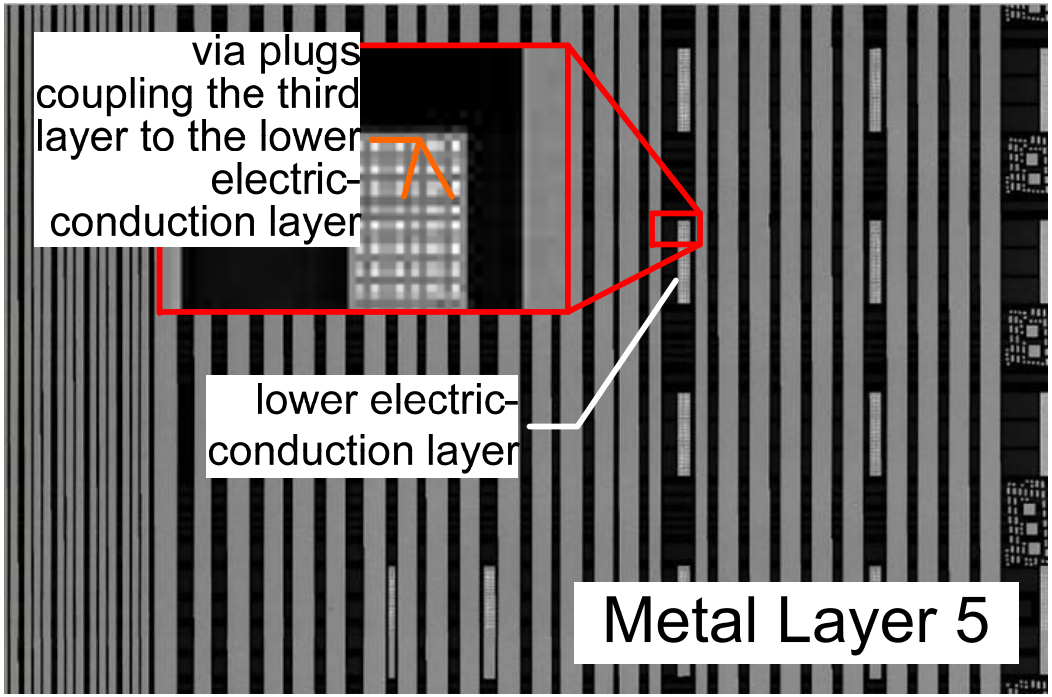
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
e) a first pad layer formed on the insulation layer and coupled to the compound layer structure, wherein the first pad layer and the compound layer structure are spaced apart from the lower electric-conduction layer; and	 The above image shows a cross section of a bond pad on the SF-228CB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The first pad layer and the compound layer structure are shown to be spaced apart from the lower electric-conduction layer by a portion of the insulation layer.

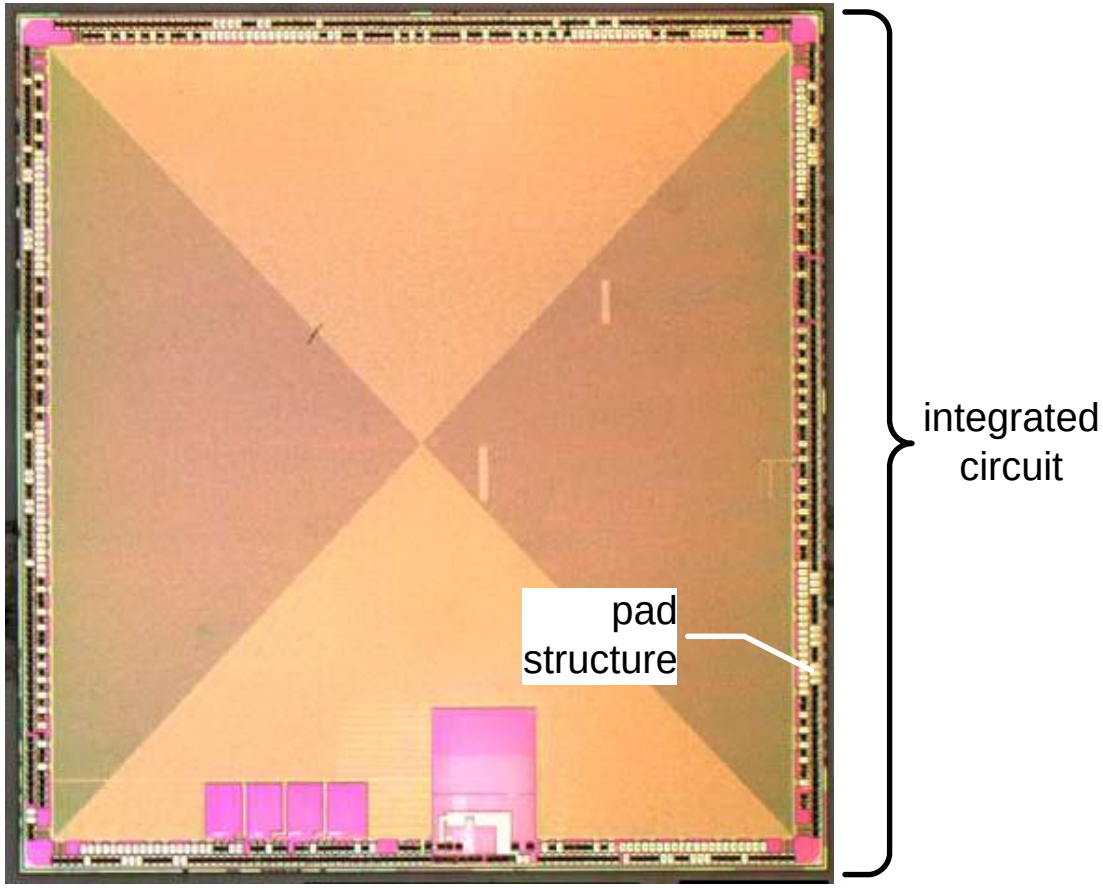
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The right side of the above image shows metal layer 8. The double-ended arrow maps a first pad layer of metal layer 8 to the first pad layer shown in the cross section image.

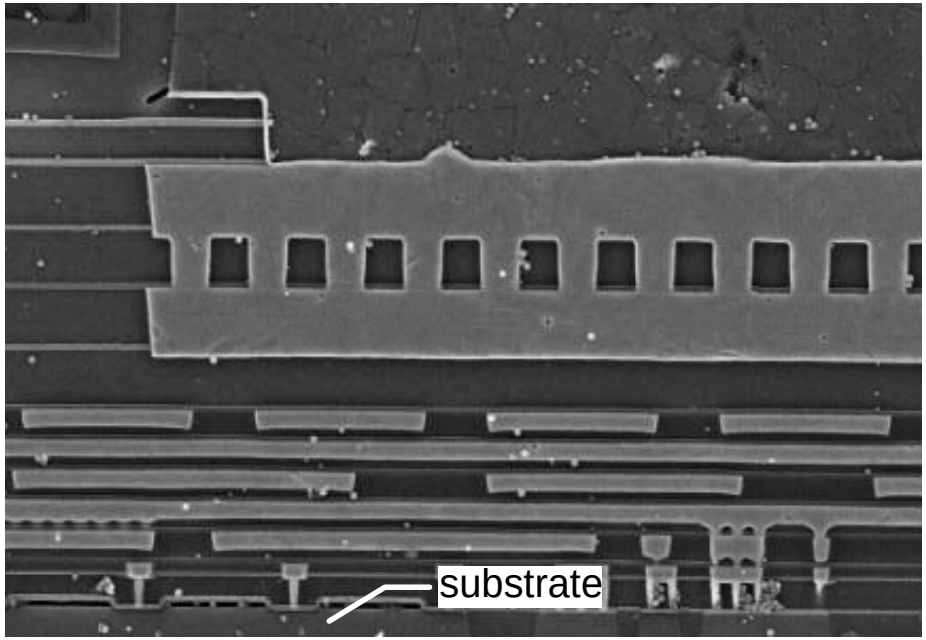
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
f) a second pad layer formed on the insulation layer and coupled to the lower electric-conduction layer.	 The above image shows the layout of metal layer 8 of the LSI SF-2281VB1-SDC chip. The image includes an annotation indicating a second pad layer of metal layer 8.

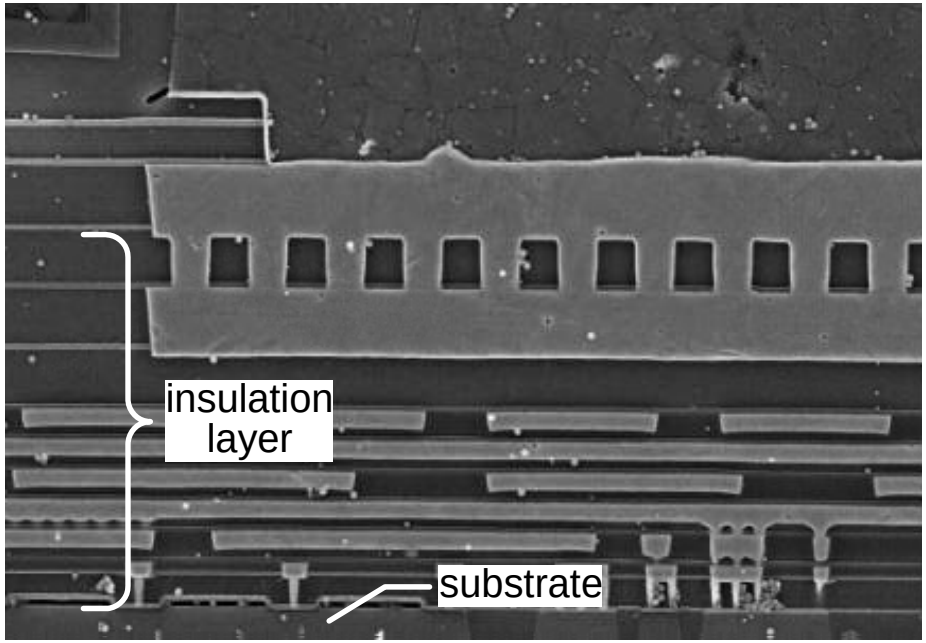
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The above image shows the layout of metal layer 7 of the LSI SF-2281VB1-SDC chip. The image includes a magnified portion outlined in red showing the second electric-conduction layer in grey and via plugs in the second connecting layer that couple the second electric-conduction layer to the second pad layer shown above in the image of metal layer 8.

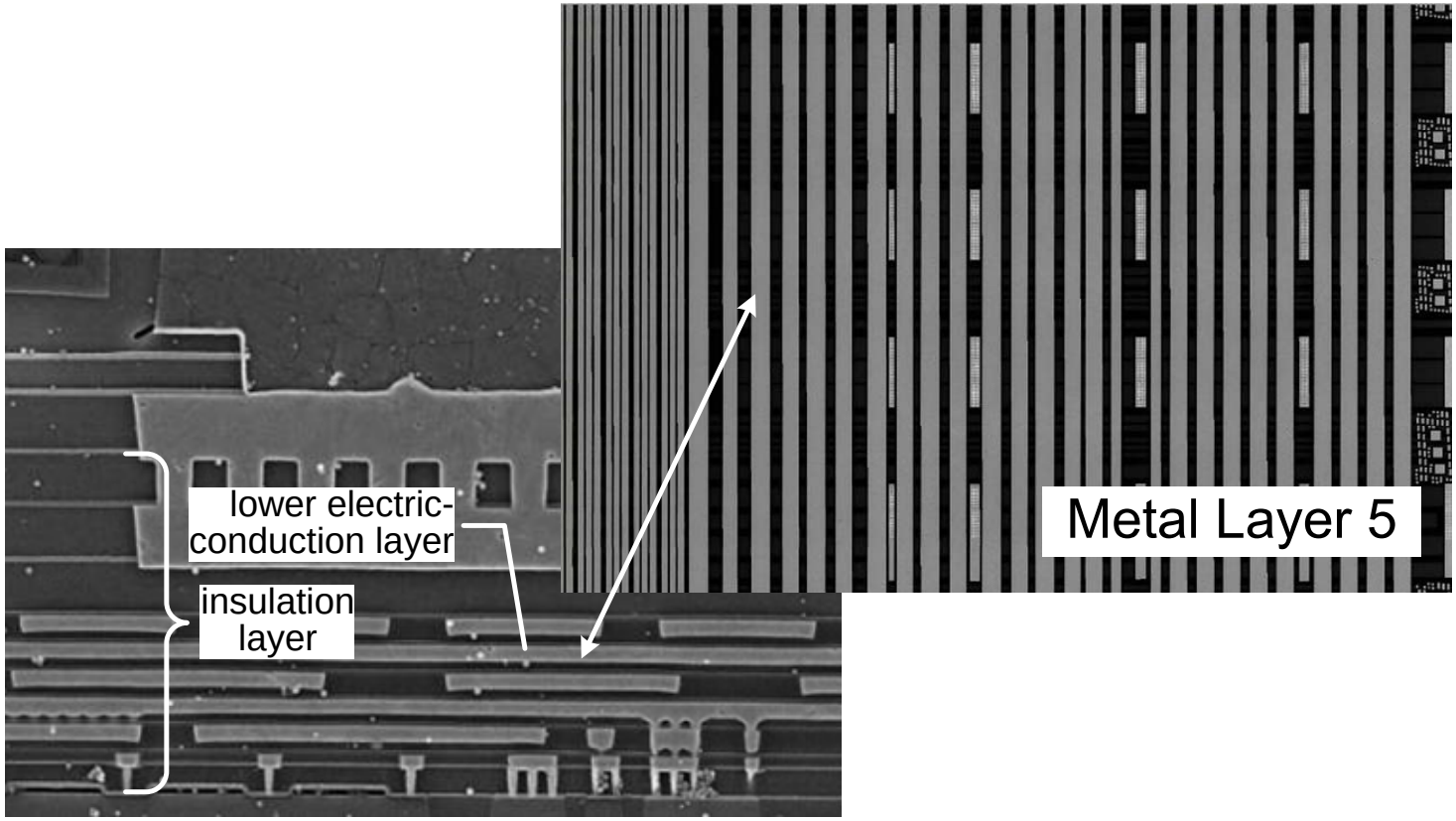
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The above image shows the layout of metal layer 6 of the LSI SF-2281VB1-SDC chip. The image includes a magnified portion outlined in red showing a third electric-conduction layer in grey and via plugs in a third connecting layer that couple the third electric-conduction layer to the second electric-conduction layer shown above in the image of metal layer 7.

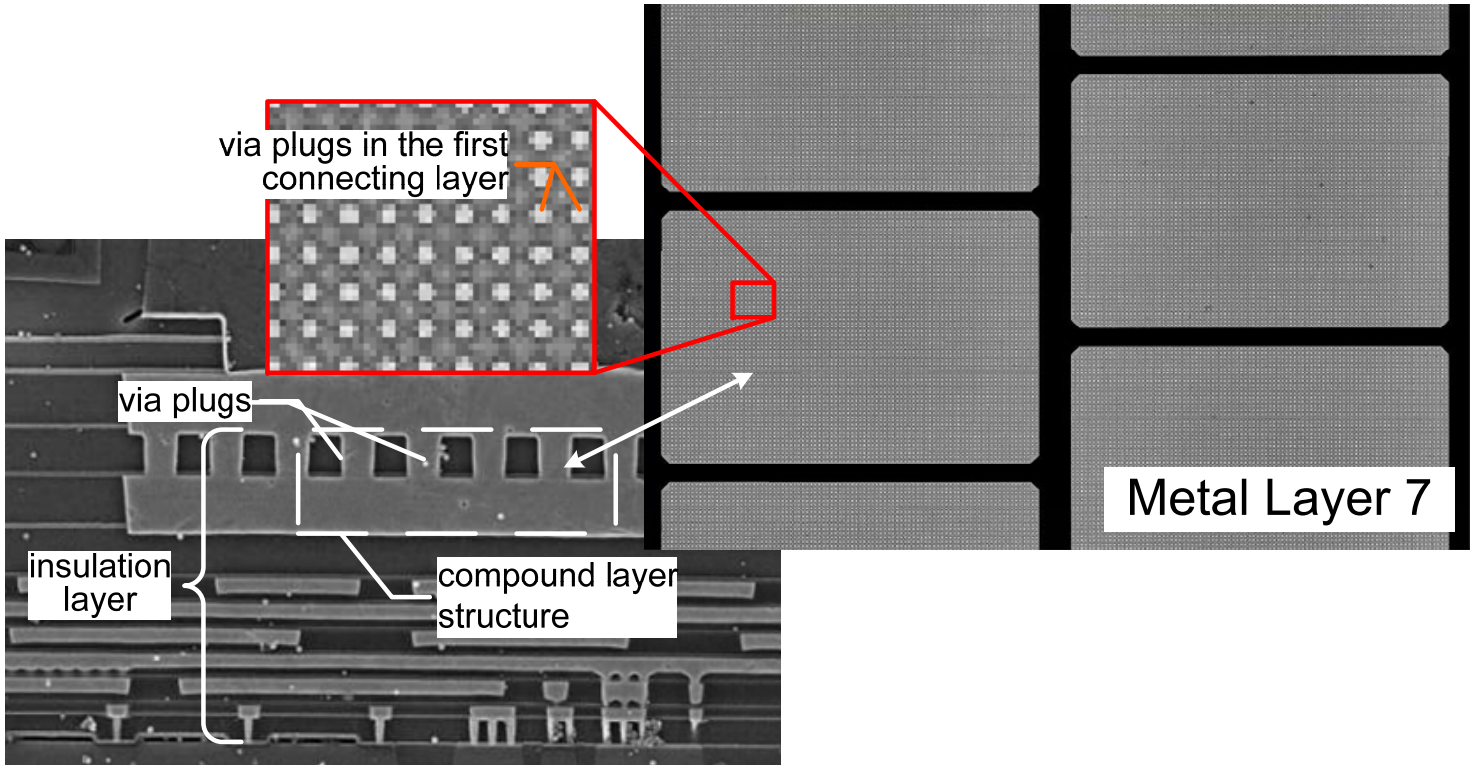
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The above image shows the layout of metal layer 5 of the LSI SF-2281VB1-SDC chip. The image includes a magnified portion outlined in red showing the lower electric-conduction layer in grey and via plugs that couple the lower electric-conduction layer to the third electric-conduction layer shown above in the image of metal layer 6.

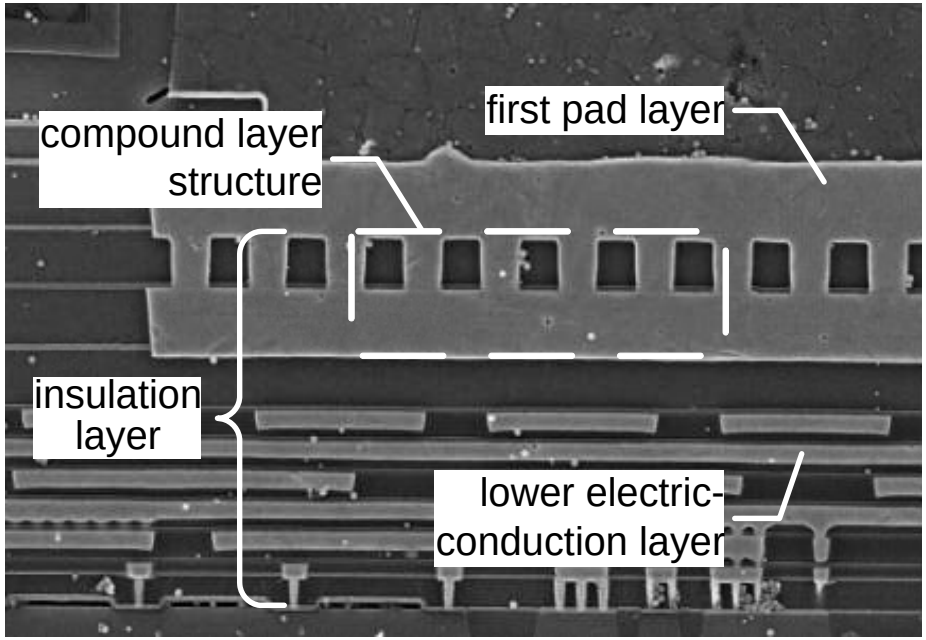
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
11. An integrated circuit (IC) device having a pad structure formed thereon, the IC device comprising:	 The LSI SandForce SF-2281VB1-SDC chip includes an integrated circuit having pad structures formed thereon. The above image of the SF-2281VB1-SDC chip illustrates both the integrated circuit and bond pad structures formed thereon.

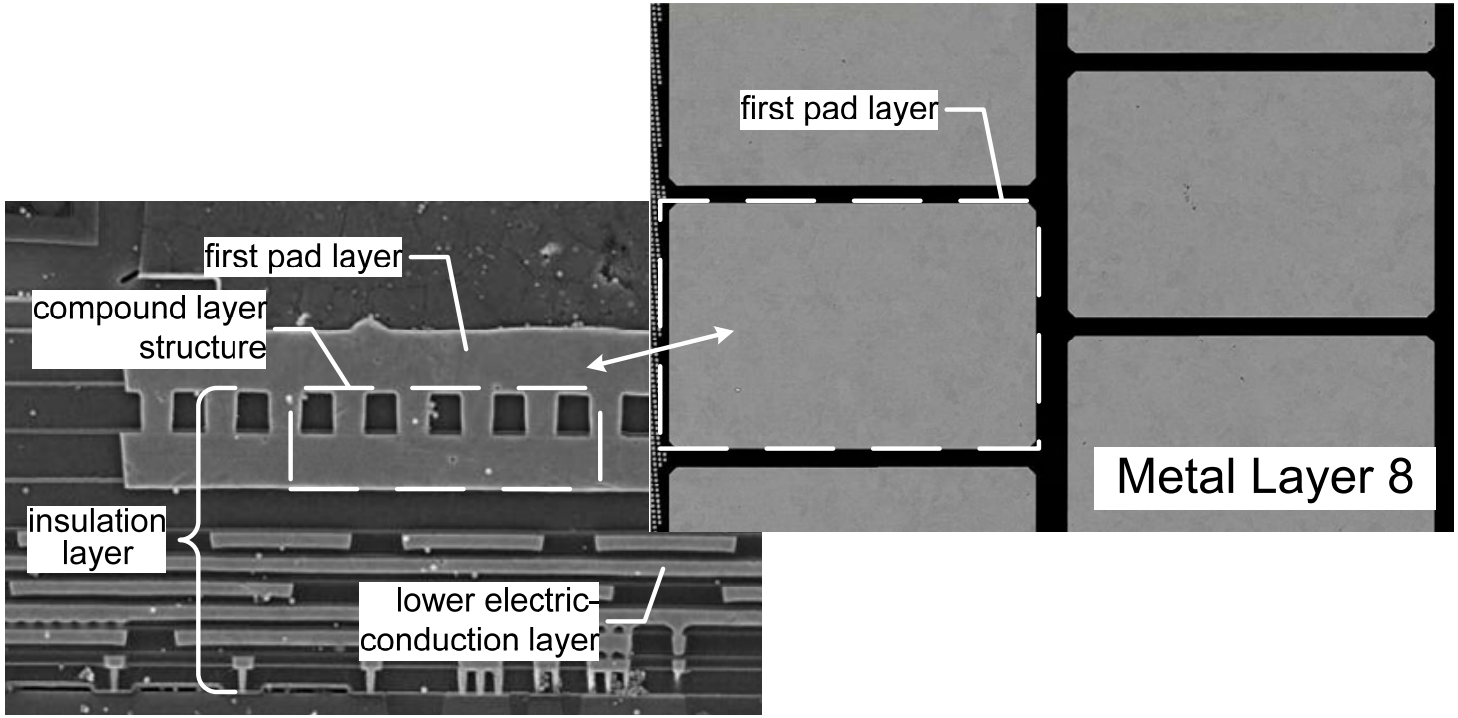
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
a) a substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. An annotation on the lower part of the image indicates the substrate.

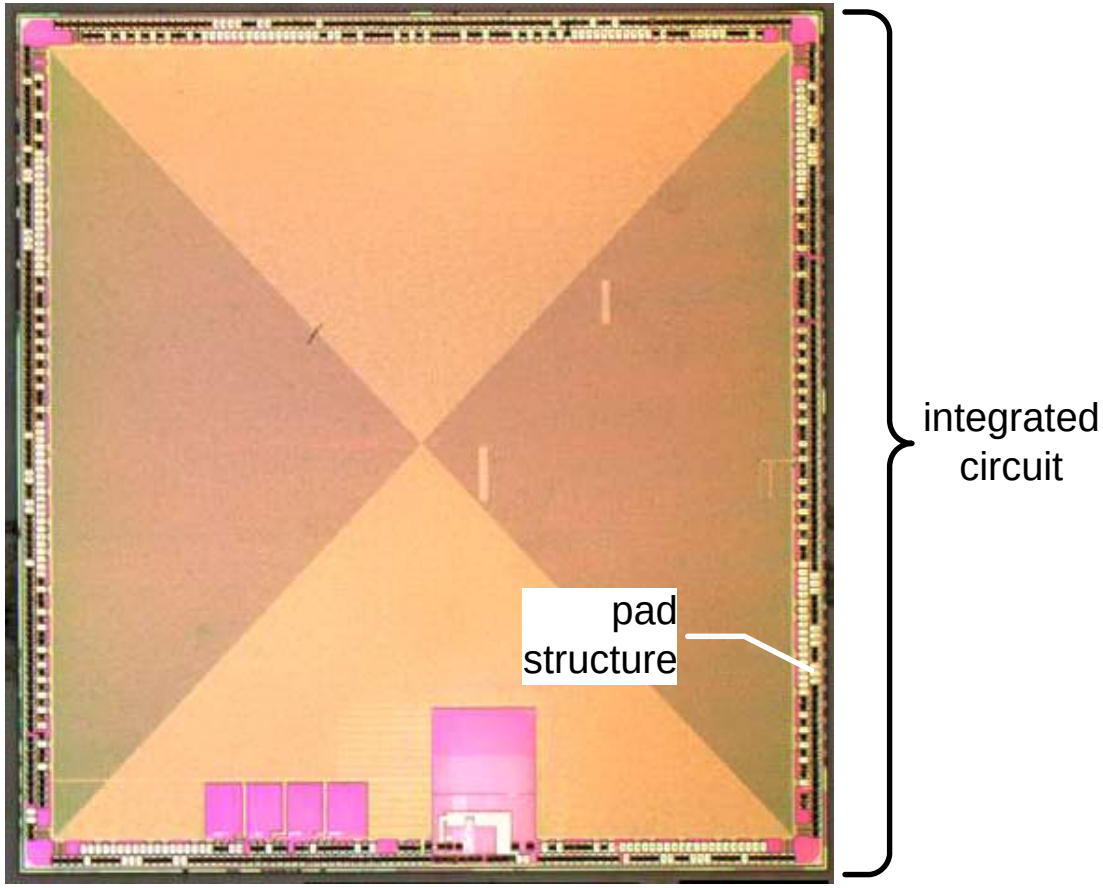
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
b) an insulation layer formed on the substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. The dark portions above the substrate illustrate the insulation layer formed on the substrate in which electric-conduction layers and via layers are formed.

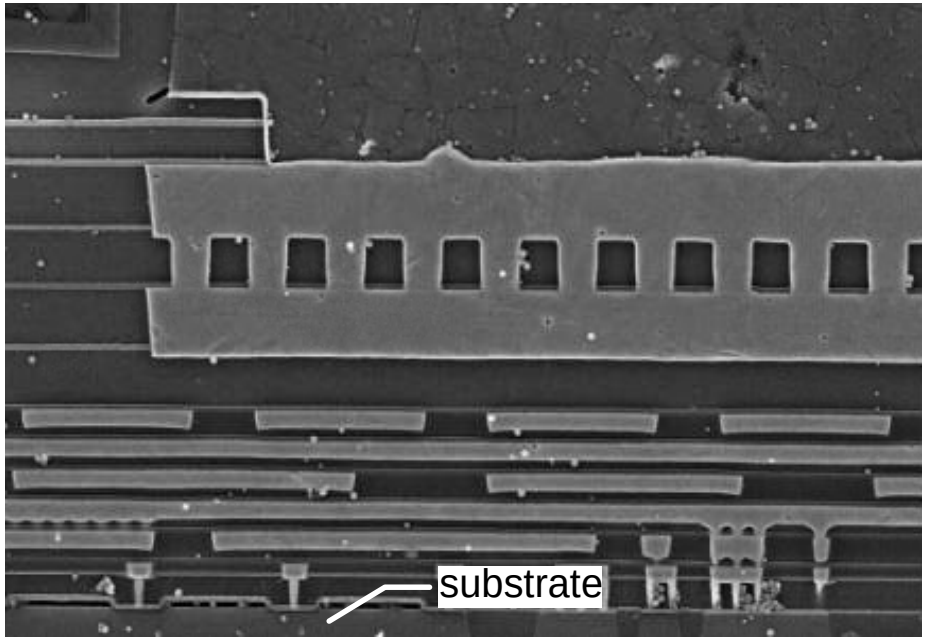
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
c) a lower electric-conduction layer formed in the insulation layer;	 The left side of the above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip with an annotation indicating a lower electric-conduction layer formed in the insulation layer. The right side of the above image shows the metal routing of metal layer 5 of the SF-2281VB1-SDC chip. The double-ended arrow maps the metal routing of layer 5 to the cross section image.

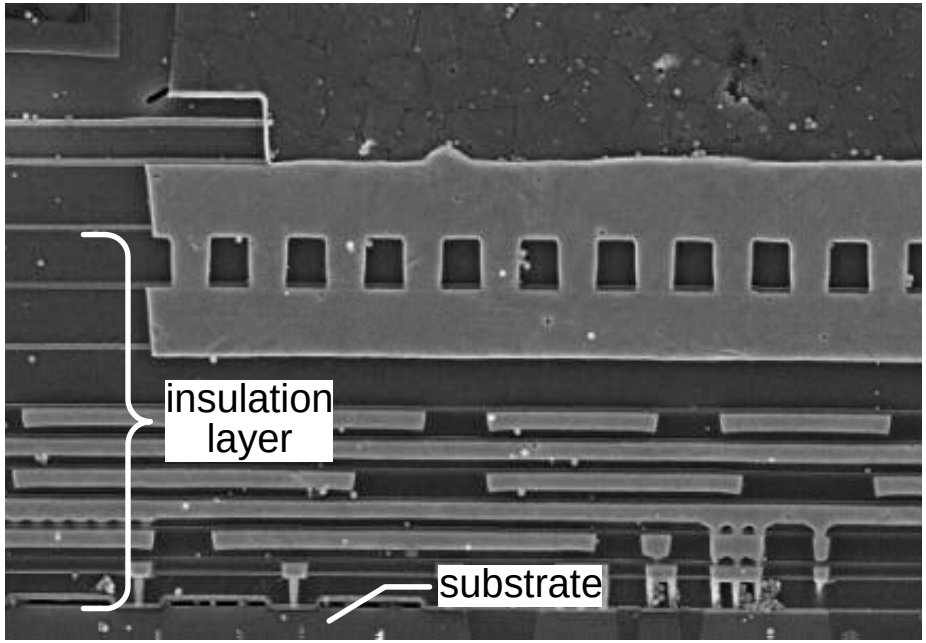
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
d) a compound layer structure formed in the insulation layer; and	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. An annotation on the cross section indicates the compound layer structure formed in the insulation layer. The compound layer structure includes both a first electric-conduction layer and a connecting layer including via plugs coupling the first electric-conduction layer to a first pad layer. The right side of the above image shows metal layer 7. The double-ended arrow maps a portion of metal layer 7 to the cross section image. The magnified portion outlined in red shows both the first electric-conduction layer in grey and the via plugs in the first connecting layer that couple the first electric-conduction layer to the first pad layer.

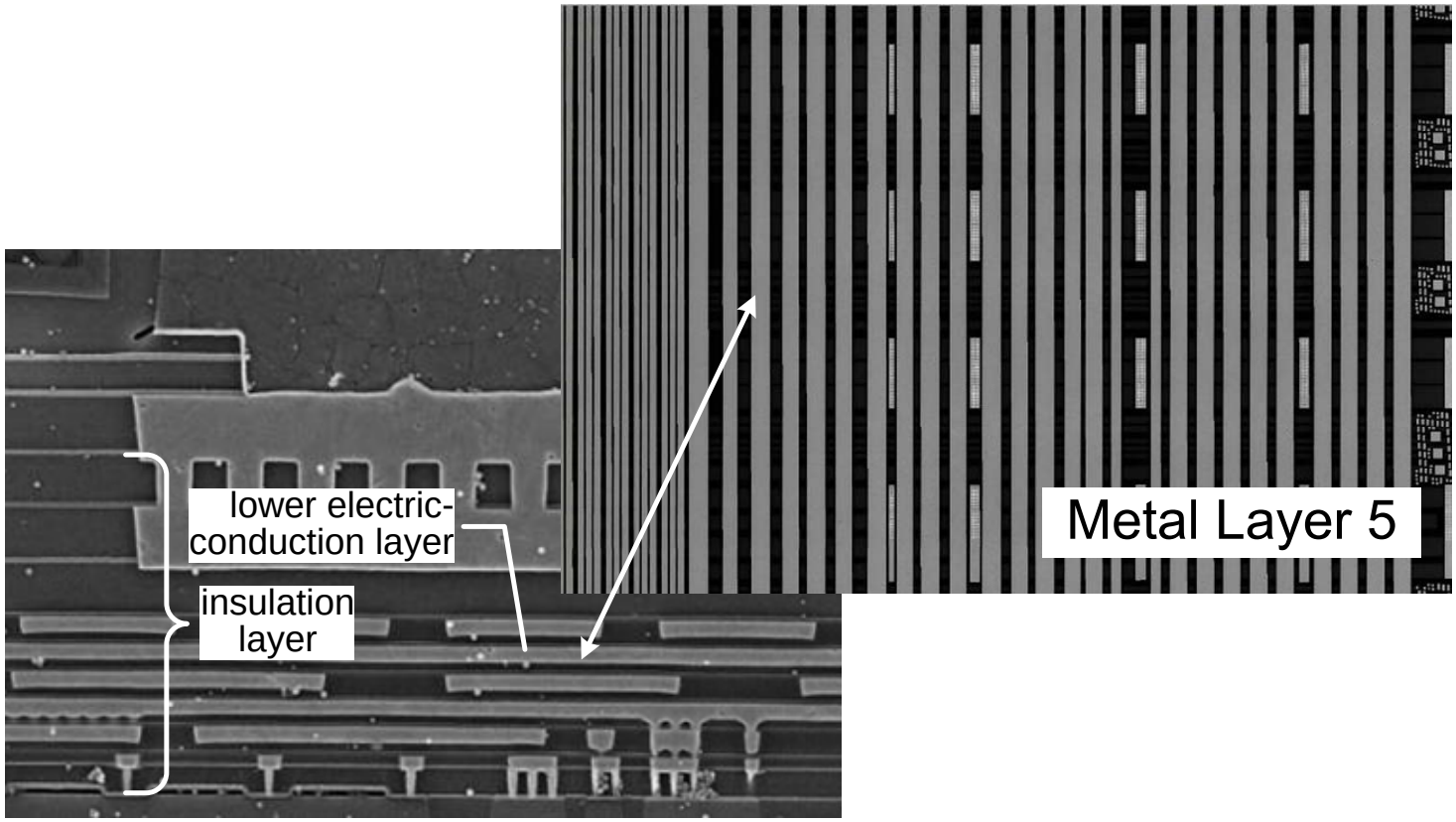
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
e) a first pad layer formed on the insulation layer and coupled to the compound layer structure, wherein the first pad layer and the compound layer structure are spaced apart from the lower electric-conduction layer.	 The above image shows a cross section of a bond pad on the SF-228CB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The first pad layer and the compound layer structure are shown to be spaced apart from the lower electric-conduction layer by a portion of the insulation layer.

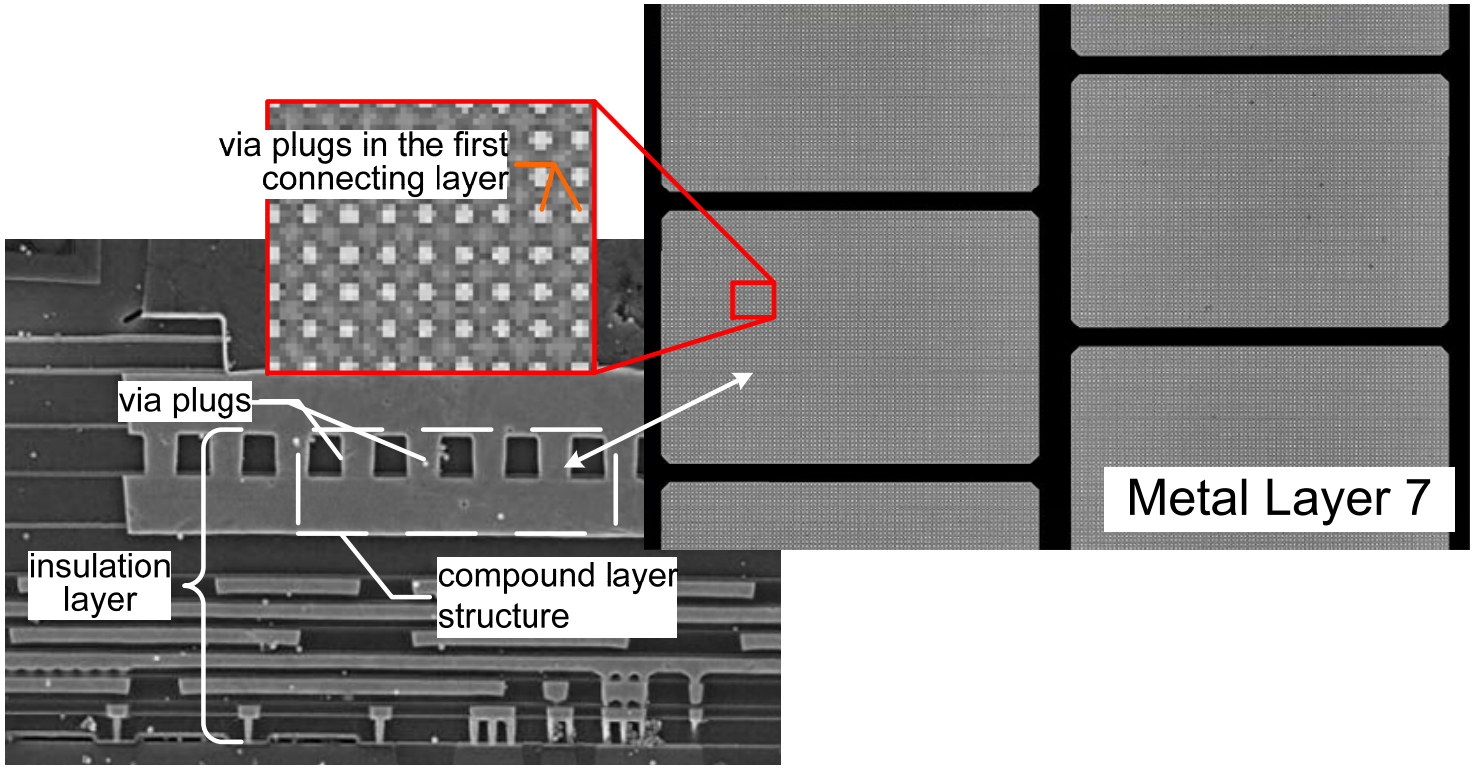
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The right side of the above image shows metal layer 8. The double-ended arrow maps a first pad layer of metal layer 8 to the first pad layer shown in the cross section image.

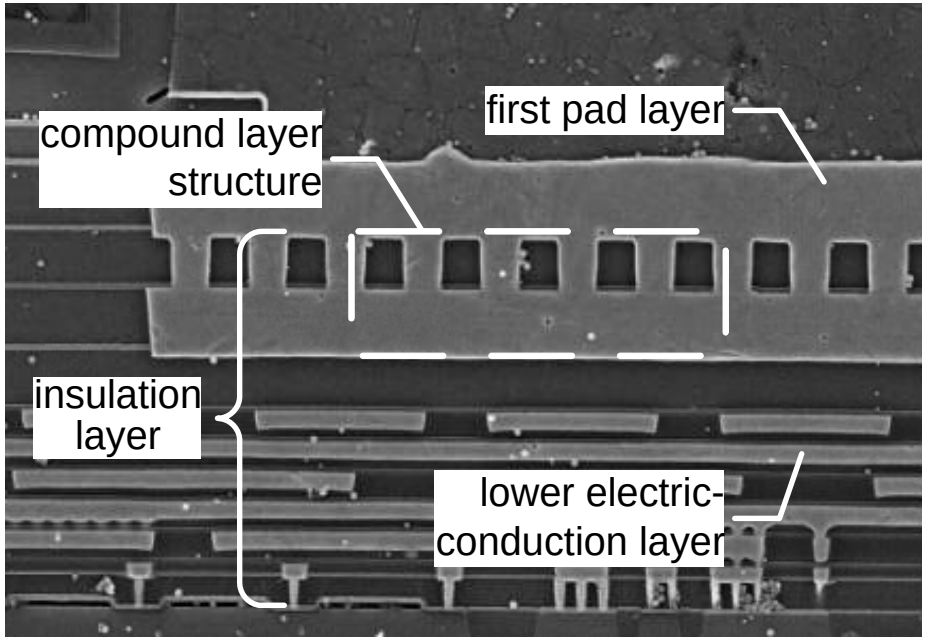
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
19. A method for fabricating an IC device having a pad structure formed thereon, the method comprising:	 The LSI SandForce SF-2281VB1-SDC chip includes an integrated circuit having pad structures formed thereon. The above image of the SF-2281VB1-SDC chip illustrates both the integrated circuit and bond pad structures formed thereon. The LSI B64002 chip is an article made or produced by LSI by means of this method of fabricating an IC device.

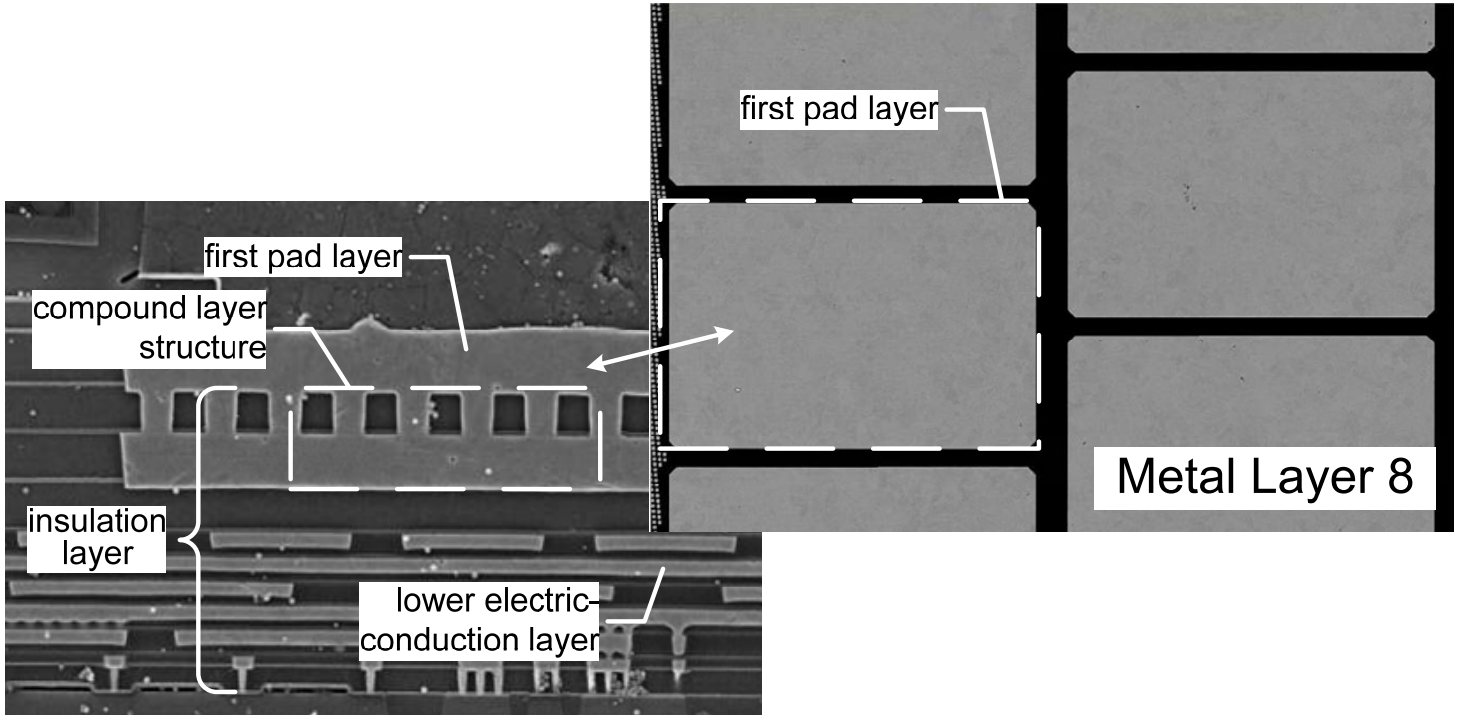
Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
a) providing a substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. An annotation on the lower part of the image indicates the substrate. LSI provides the substrate during the fabrication process.

Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
b) forming an insulation layer formed on the substrate;	 The above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip. The dark portions above the substrate illustrate the insulation layer formed on the substrate in which electric-conduction layers and via layers are formed. LSI forms the insulation layer on the substrate during the fabrication process.

Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
c) forming a lower electric-conduction layer formed in the insulation layer, at least a part of the lower electric-conduction layer being covered by the insulation layer;	 The left side of the above image shows a cross section of a bond pad on the LSI SF-2281VB1-SDC chip with an annotation indicating a lower electric-conduction layer formed in the insulation layer. The right side of the above image shows the metal routing of metal layer 5 of the SF-2281VB1-SDC chip. The double-ended arrow maps the metal routing of layer 5 to the cross section image. LSI forms the lower electric-conduction layer in the insulation layer during the fabrication process.

Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
d) forming a compound layer structure formed in the insulation layer, the compound layer structure being spaced apart from and not connected to the lower electric-conduction layer; and	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. An annotation on the cross section indicates the compound layer structure formed in the insulation layer. The compound layer structure includes both a first electric-conduction layer and a connecting layer including via plugs coupling the first electric-conduction layer to a first pad layer. The right side of the above image shows metal layer 7. The double-ended arrow maps a portion of metal layer 7 to the cross section image. The magnified portion outlined in red shows both the first electric-conduction layer in grey and the via plugs in the first connecting layer that couple the first electric-conduction layer to the first pad layer. LSI forms the compound layer structure in the insulation layer during the fabrication process.

Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
e) forming a first pad layer formed on the insulation layer, the first pad layer being coupled to the compound layer, wherein in the forming a first pad layer step e) the first pad layer and the compound layer are spaced apart from the lower electric-conduction layer.	 The above image shows a cross section of a bond pad on the SF-228CB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The first pad layer and the compound layer structure are shown to be spaced apart from the lower electric-conduction layer by a portion of the insulation layer. LSI forms the first pad layer on the insulation layer during the fabrication process.

Claims – US 6,787,928	Application of Claim Language to LSI SandForce SF-2281VB1-SDC
	 The left side of the above image shows a cross section of a bond pad on the SF-2281VB1-SDC chip. The image includes an annotation indicating the first pad layer formed on the insulation layer and coupled to the compound layer structure. The right side of the above image shows metal layer 8. The double-ended arrow maps a first pad layer of metal layer 8 to the first pad layer shown in the cross section image. LSI forms the first pad layer on the insulation layer during the fabrication process.