

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTELLECTUAL VENTURES MANAGEMENT, LLC
Petitioner

v.

XILINX, INC.
Patent Owner

Case IPR2012-00018
Patent 7,566,960 B1

Before SALLY C. MEDLEY, KARL D. EASTHOM, and
JUSTIN T. ARBES, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Petitioner Intellectual Ventures Management, LLC (“IVM”) filed a Petition (Paper 6) (“Pet.”) seeking *inter partes* review of claims 1-13 of Patent 7,566,960 B1 (“the ’960 patent”) pursuant to 35 U.S.C. §§ 311-319. On February 12, 2013, the Board granted the Petition and instituted an *inter partes* review of all claims on four grounds of unpatentability (Paper 13) (“Dec. on Inst.”).

Subsequent to institution, Patent Owner Xilinx, Inc. (“Xilinx”) filed a Patent Owner Response (Paper 17) (“PO Resp.”), and IVM filed a Reply (Paper 28) (“Pet. Reply”). Along with its Patent Owner Response, Xilinx filed a Motion to Amend. Paper 19. The motion was dismissed as defective, and Xilinx filed a Substitute Motion to Amend. *See* Papers 20, 22. After Xilinx filed its Substitute Motion, the Board entered a decision in *Idle Free Systems, Inc. v. Bergstrom, Inc.*, IPR2012-00027, Paper 26 (June 11, 2013) (“*Idle Free* Decision”) regarding motions to amend. Xilinx requested, and received authorization from the Board, to file a second substitute motion to amend to comply with that decision. Paper 24. Xilinx then filed its Second Substitute Motion to Amend (Paper 26) (“Second Subst. Mot. to Amend”), proposing substitute claims 14-21 if the Board determines claim 1 to be unpatentable, and substitute claims 22-26 if the Board determines claim 9 to be unpatentable. IVM filed an Opposition to the Second Substitute Motion to Amend (Paper 29) (“Opp.”), and Xilinx filed a Reply (Paper 31) (“PO Reply”). The parties did not seek an oral hearing. Paper 34.

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that IVM has shown by a preponderance of the evidence that claims 1-13 of the '960 patent are unpatentable, and we deny Xilinx's Second Substitute Motion to Amend.

A. The '960 Patent

The '960 patent relates to an “interposer disposed inside an integrated circuit package between a die and the package, wherein the interposer provides bypass capacitance, signal redistribution functionality and/or signal termination structures close to the semiconductor die.” Ex. 1001, col. 1, ll. 5-9. The '960 patent explains that it was known in the prior art to add a bypass capacitor to an integrated circuit (IC) device to reduce various power supply problems. *Id.* at col. 1, l. 49-col. 2, l. 30. According to the '960 patent, however, power supply problems often could not be anticipated during the initial design of an integrated circuit, and redesigning an integrated circuit to add bypass capacitance after it already has been designed and built “can be exceedingly expensive and slow.” *Id.* at col. 2, ll. 31-40. Also, the interconnections between the terminals on an integrated circuit and the signal traces on a printed circuit board (PCB) are sometimes incorrect, such that “[i]t would be desirable to be able to correct for this problem without having to redesign and refabricate the printed circuit.” *Id.* at col. 2, ll. 41-50. The '960 patent describes adding an extremely thin “capacitive interposer (caposer),” which provides the necessary bypass capacitance, between an integrated circuit die and an inside surface of an integrated circuit package (connected to a printed circuit board). *Id.* at col. 3, ll. 13-27; Fig. 1. The integrated circuit design then does not need to be

changed to solve power supply and interconnection problems that later arise. *Id.* at col. 3, ll. 41-44; col. 4, ll. 60-67.

The '960 patent describes various exemplary embodiments. Figure 10 is reproduced below.

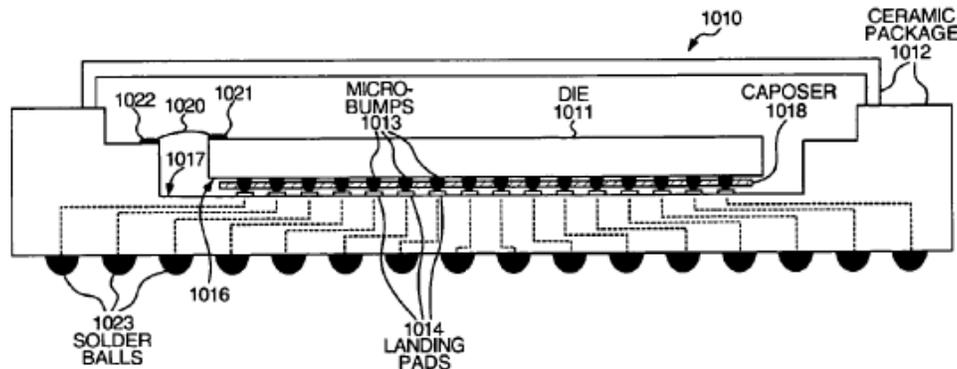


FIG. 10

Figure 10 depicts structure 1010 comprising (1) integrated circuit die 1011 having micro-bumps 1013 on planar surface 1016, (2) ceramic integrated circuit package 1012 having landing pads 1014 on inside upper surface 1017, and (3) through-hole caposer 1018¹ “disposed between inside upper surface 1017 of ceramic package 1012 and surface 1016 of die 1011.” *Id.* at col. 11, ll. 10-31. Integrated circuit package 1012 also has solder balls 1023 on its bottom surface for coupling to a printed circuit board (not shown). *Id.* at col. 11, ll. 33-37.

¹ The '960 patent explains that caposers may be either “through-hole” or “via.” Ex. 1001, col. 10, ll. 47-58. In a through-hole caposer, “an array of through holes passes through the caposer,” whereas in a via caposer, “conductive vias pass substantially orthogonally through the caposer.” *Id.*

Figure 24 depicts another embodiment and is reproduced below.

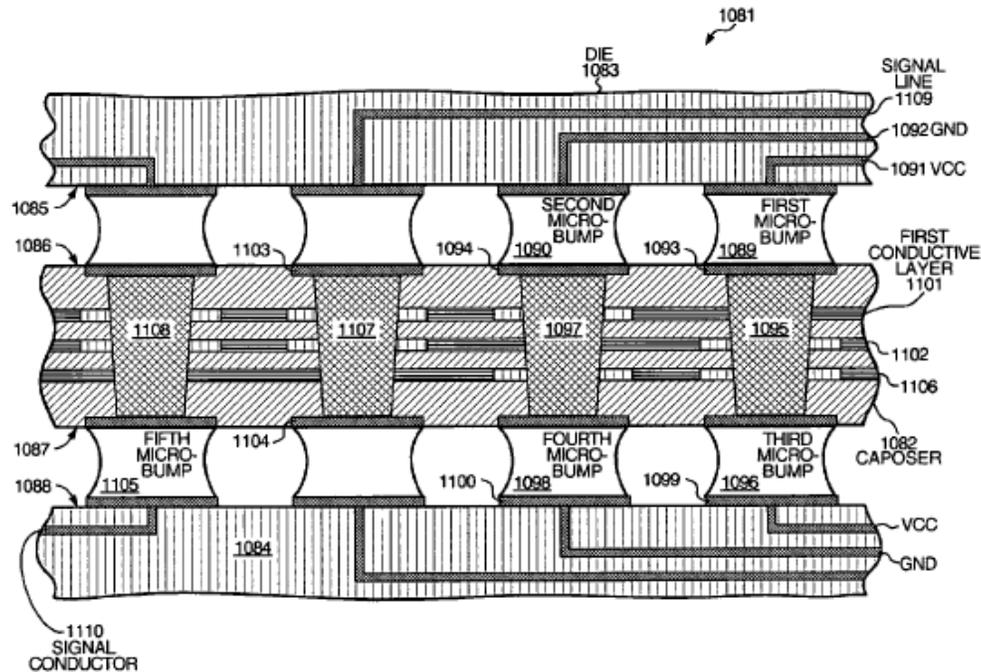


FIG. 24

As shown in Figure 24, caposer 1082 provides bypass capacitance and also “redistributes signals” through the use of multiple conductive layers 1101, 1102, and 1106. *Id.* at col. 18, l. 47-col. 19, l. 3. Signal line 1109 is coupled to landing pad 1103, and third conductive layer 1106 of caposer 1082 is coupled to vias 1107 and 1108. *Id.* This creates an electrically conductive path between the micro-bump above landing pad 1103 and two different landing pads on integrated circuit package 1084: (1) the landing pad below pad 1104 and the corresponding micro-bump, and (2) the landing pad below micro-bump 1105. *Id.* Caposer 1082, therefore, “can be used to redistribute signal inputs and outputs from array positions on die 1083 to different positions on ceramic package 1084.” *Id.* at col. 18, l. 67-col. 19, l. 3.

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