

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTELLECTUAL VENTURES MANAGEMENT, LLC  
Petitioner

v.

XILINX, INC.  
Patent Owner

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Case IPR2012-00020  
Patent 8,058,897

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Before SALLY C. MEDLEY, KARL D. EASTHOM, and  
JUSTIN T. ARBES, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

## I. INTRODUCTION

### A. *Background*

Petitioner, Intellectual Ventures Management, LLC (“IVM”), filed a Petition (Paper 5) (“Pet.”) requesting *inter partes* review of claims 1-9 and 12-14 of U.S. Patent No. 8,058,897 B1 (“the ’897 patent”) pursuant to 35 U.S.C. §§ 311-319. On February 12, 2013, the Board granted the Petition as to all claims challenged, and instituted trial for claims 1-9 and 12-14 on three grounds of unpatentability. Paper 14 (“Dec. on Inst.”).

Subsequent to institution, Patent Owner, Xilinx, Inc. (“Xilinx”) filed a Patent Owner Response (Paper 18; “PO Resp.”) and a Motion to Amend, requesting the cancellation of claim 1 (Paper 20; “Mot. to Amend”). IVM filed a Reply to the Patent Owner Response. Paper 23 (“Pet. Reply.”)

Oral hearing was held on November 7, 2013.<sup>1</sup>

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that IVM has shown by a preponderance of the evidence that claims 2-9 and 12-14 of the ’897 patent are unpatentable. Xilinx’s Motion to Amend, requesting the cancellation of claim 1, is *granted*.

### B. *The ’897 Patent*

The invention of the ’897 patent relates to the configuration of an integrated circuit (IC) that includes multiple dies, such as a master die and a slave die. A master die receives configuration data for both the master die

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<sup>1</sup> A transcript of the oral hearing is included in the record. Paper 32.

and the slave die. The master and slave segment of the configuration data is determined, and the slave segment of the configuration data is distributed to the IC's slave die. Ex. 1001, 2:5-15. Configuration data also may be sent from the master die of a first IC to a second IC. *Id.* at 7:45-60.

*C. Exemplary Claims*

Claim 1 and claim 8 are representative and reproduced here:

1. A method of configuring an integrated circuit (IC), the method comprising:

receiving configuration data within a master die of a first IC, wherein the first IC comprises the master die and a slave die;

determining a master segment and a slave segment of the configuration data, wherein the master segment specifies a master die circuit design to be implemented within the master die and the slave segment specifies a slave die circuit design to be implemented within the slave die;

distributing the slave segment of the configuration data to the slave die of the first IC,

determining, within the master die, whether configuration data comprises a segment of configuration data for a second IC; and

responsive to determining that the configuration data comprises a segment of configuration data for the second IC, sending the segment of the configuration data to the second IC.

8. An integrated circuit (IC) comprising:

an interposer comprising a configuration bus;

a first die on a surface of the interposer;

a second die on the surface of the interposer,

wherein the first die and the second die are coupled by the configuration bus,

wherein the first die is configured, responsive to receiving configuration data, to determine a first segment and a second segment of the configuration data and distribute the second segment of the configuration data to the second die through the configuration bus,

wherein the first die is configured to determine whether the configuration data comprises a segment of configuration data for an additional IC, and

wherein the first die comprises a configuration data output coupled to an output of the IC, and responsive to determining that the configuration data comprises a segment of configuration data for the additional IC, the first die is configured to send the segment of configuration data for the additional IC through the first die configuration data output.

*D. The Alleged Grounds of Unpatentability*

The prior art references as applied to claims 1-9 and 12-14 are:

Wennekamp	U.S. Patent 7,397,272	July 8, 2008 (Ex. 1009)
Miller	U.S. Patent 7,827,336	Nov. 2, 2010 (Ex. 1010)
Siniaguine	U.S. Patent 6,730,540	May 4, 2004 (Ex. 1013)

The Board instituted trial on the following grounds of unpatentability:

Reference[s]	Basis	Claims challenged
Wennekamp	§ 103	1-7
Wennekamp and Miller	§ 103	1, 8, and 12-14
Wennekamp, Miller, and Siniaguine	§ 103	9

## II. ANALYSIS

### A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

If a feature appearing in the specification is not necessary to interpret what the inventor means by a claim term, it would be “extraneous” and should not be read into the claim. *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988).

In the Decision on Institution, the Board determined the broadest reasonable construction for “[f]irst IC comprises the master die and a slave die” (claim 1) and “[a]n integrated circuit (IC) comprising” a “first die on a surface of the interposer” and “a second die on the surface of the interposer” (claim 8). Dec. on Inst. 6-7. For all other claim terms, the Board applied the plain and ordinary meaning that the term would have had to a person of ordinary skill in the art. *Id.* at 7.

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