UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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HEWLETT-PACKARD COMPANY,
Petitioner,

v.

MCM PORTFOLIO, LLC,
Patent Owner.

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Case IPR2013-00217
Patent 7,162,549

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Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK,
Administrative Patent Judges.

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Petitioner Hewlett-Packard Company ("HP") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 7, 11, 19, and 21 (the "challenged claims") of U.S. Patent No. 7,162,549 (Exhibit 1001, "the '549 patent") under 35 U.S.C. §§ 311-319. Patent Owner MCM Portfolio, LLC ("MCM") filed a Preliminary Response. Paper 9. On September 10, 2013, we instituted trial (Paper 10; "Decision"), concluding that Petitioner had demonstrated a reasonable likelihood of showing that the challenged claims are unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 6,199,122 (Ex. 1005) ("Kobayashi") combined with WO 98/03915 (Ex. 1007) ("Kikuchi"). Decision 3, 16.

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Petitioner has shown by a preponderance of evidence that claims 7, 11, 19, and 21 are *unpatentable*.

B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6, 1. On February 11, 2014, after a finding of No Violation of Section 337 in a concurrent proceeding at the International Trade Commission (No. 337-TA-841), a stay of the 6:12-cv-208 case was lifted and it was consolidated with *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 28, 2012). A

Markman Hearing is currently scheduled in that case for October 8, 2014. *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 14, 2014).

In addition, the '549 patent is the subject of a pending reissue proceeding, US Application 12/351,691. We ordered a stay of that examination pending the termination or completion of this proceeding. Paper 8.

C. The '549 Patent

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, 1:21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards were commonly used with digital cameras to allow for convenient transfer of images from a camera to a personal computer. *Id.* at 1:26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at 2:28-55. Each of the card formats required a different interface adapter to work with a personal computer. *Id.* at 3:9-25.

The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at 3:52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller and, if not, performing operations to manage error correction for the flash-memory card. *Id.* at 3:24-65.

D. Illustrative Claim

Claim 7, reproduced below, is illustrative of the claimed subject matter:

7. A method comprising:

> using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;

> determining whether the flash storage system includes a controller for error correction; and

> in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

II. ANALYSIS

A. Seventh Amendment

As a preliminary matter, MCM argues that *inter partes* review proceedings violate the Seventh Amendment. PO Resp. 2-13. The U.S. Court of Appeals for the Federal Circuit, however, has previously rejected this argument in the context of reexaminations. *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 603-05 (Fed. Cir. 1985) (holding that even when applied retroactively, the reexamination statute does not violate the jury trial guarantee of the Seventh Amendment); *see also Joy Techs., Inc. v. Manbeck*, 959 F.2d 226, 228-29 (Fed. Cir. 1992) (affirming the holding in *Patlex*), *other grounds superseded by statute*, 35 U.S.C. § 145, *as recognized in In re Teles AG Informationstechnologien*, 747 F.3d 1357 (Fed. Cir. 2014). *Inter partes* review proceedings continue the basic functions of the reexamination proceedings at issue in *Patlex*—authorizing the Office to reexamine the

validity of an issued patent and to cancel any claims the Office concludes should not have been issued. Patent Owner does not identify any constitutionally-significant distinction between reexamination proceedings and *inter partes* review proceedings. Thus, for the reasons articulated in *Patlex*, we conclude that *inter partes* reviews, like reexaminations, comply with the Seventh Amendment.

B. Claim Construction

We construe all terms, whether or not expressly discussed here, using the broadest reasonable construction in light of the '549 patent specification. 37 C.F.R. § 42.100(b). For the purposes of the decision to institute we expressly construed the following terms: (1) "flash adapter" and "flash adapter section" as "a section of the controller chip that enables communication with the flash storage system" and (2) "bad block mapping" as a type of error correction. Decision 5-6. In the post-institution briefs, the parties do not dispute these constructions. *See* Paper 23 ("PO Resp."); Paper 24 ("Reply"). For purposes of this decision, we continue to apply these constructions.

C. Overview of Kobayashi

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that are then used to control a storage medium (which can be a flash-memory card). Ex. 1005, 2:55-64, 3:63-65. This configuration is shown in Figure 1, which is reproduced below.

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