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Paper 29
Entered: May 4, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2014-00113
Patent 6,058,045

Before KEVIN F. TURNER, TREVOR M. JEFFERSON,
and DAVID C. McKONE, *Administrative Patent Judges.*

JEFFERSON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, "Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1 and 4 of U.S. Patent No. 6,058,045 (Ex. 1001, "the '045 patent"). *See* 35 U.S.C. § 311. Intellectual Ventures I LLC ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 13, "Dec.") we instituted this proceeding as to claims 1 and 4 of the '045 patent.

Patent Owner filed a Patent Owner Response (Paper 20, "PO Resp.") and Petitioner filed a Reply to the Patent Owner Response (Paper 21, "Reply"). An oral hearing in this matter was held on November 6, 2014 (Paper 28, "Tr.").

We have jurisdiction under 35 U.S.C. § 6(c). This is a final written decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of the challenged claims. For the reasons that follow, Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 4 of the '045 patent are unpatentable.

B. Related Matters

Patent Owner has sued Petitioner for infringement of the '045 patent in *Intellectual Ventures I LLC v. Toshiba Corp.*, No. 1:13-cv-00453 (D. Del.), filed on March 20, 2013. Pet. 1; Paper 7 (Patent Owner's Mandatory Notices).

C. The '045 Patent

The '045 patent, titled "Serial Flash Memory," issued on May 2, 2000, and claims the benefit of a provisional application dated September 9, 1996. Ex. 1001, at [45], [60], [62]. The '045 patent discloses a "scaleable flash memory cell structure and method of manufacture that improves data retention, increases capacitive coupling and speed of operation, and improves reliability." *Id*. at 2:39–42. "The flash cell of the ['045 patent] permits implementation of arrays of flash memory cells that allow the designer to program and/or erase individual bytes of memory as well as blocks of memory." *Id*. at 2:44–46. Figure 4 of the '045 patent, shown below, provides the exemplary memory array circuit disclosed.

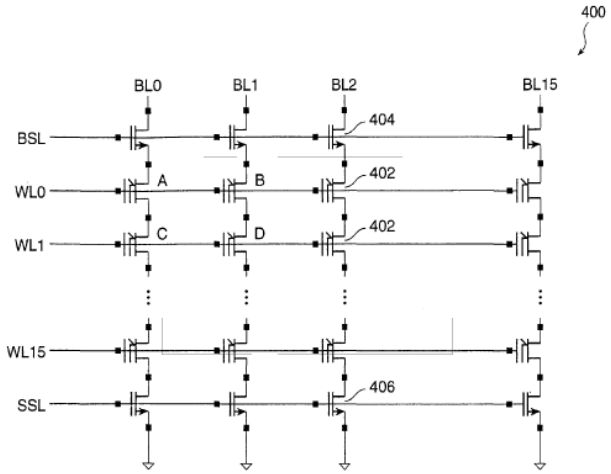

FIG. 4

Figure 4 depicts "a circuit schematic for an exemplary memory array made of flash cells." *Id*. at 3:25–26. The disclosed memory array 400 in Figure 4 includes columns of serially connected flash memory cells located at the intersection of bit lines (BL0–BL15) and word lines (WL0–WL15). *Id*. at 6:22–28. Bit select control line (BSL) controls gate terminals of bit select

transistors 404, which couple bit lines to memory cells. *Id*. at 6:30–31. Source select control line (SSL) controls gate terminals for source select transistors 406, which couple ground to memory cells. *Id*. at 6:31–32.

Table 1 of the'045 patent, reproduced below, provides a biasing scheme that discloses voltages that are applied to lines of the array to perform program, read, or erase operations for selected or unselected portions of the array.

TABLE I

Control Line	Erase	Program	Read	Condition
BSL	Vcc	Vcc	Vcc	Selected
SSL	Vss	Vss	Vcc	Selected
BLO	Vcc	Vss	1.0–1.4V	Selected
BL1	Vss	Vcc	0.5V	Unselected
WL0	Vcc	Vcc	Vcc	Unselected
WL1	−12 to −15V	15–20V	Vss	Selected

Id. at 6:37–45. Table 1 provides an example of a biasing scheme for an individual cell, showing voltages applied to various control lines (i.e., Vcc, Vss, etc.), and the desired function (erase, program, or read) for the selected or unselected portions of the array. *Id*. at 6:48–56.

D. Challenged Claims

Challenged claims 1 and 4 are reproduced below:

> 1. An array of flash memory cells comprising:
>
> a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
>
> a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line

select transistors having gate terminals coupled to a bit line select control line;

a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to from rows of memory cells with common gate terminals; and

a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having gate terminals coupled to a source select control line,

wherein, during programming:

a logic high voltage is applied to said bit line select control line to turn on bit line select transistors,

a logic low voltage is applied to source select control line to turn off source select transistors;

a logic low voltage is applied to a selected bit line while a logic high voltage is applied to unselected bit lines, and

a logic high voltage is applied to unselected word lines, while a boosted positive voltage is applied to a selected word line.

4. A method of operating a flash memory device wherein programming memory cells is accomplished by the steps of:

applying a logic high voltage to a bit line select control line to turn on bit line select transistors,

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