

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,  
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,  
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.  
Petitioner

v.

INTELLECTUAL VENTURES I LLC  
Patent Owner

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Case IPR2014-00113  
Patent 6,058,045

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Before KEVIN F. TURNER, TREVOR M. JEFFERSON,  
and DAVID C. McKONE, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## I. INTRODUCTION

### *A. Background*

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. Toshiba Corporation (collectively “Petitioner”) filed a Petition (Paper 1, “Pet.”) to institute an *inter partes* review of claims 1 and 4 of U.S. Patent No. 6,058,045 (Ex. 1001, “the ’045 patent”). See 35 U.S.C. § 311. Intellectual Ventures I LLC (“Patent Owner”) filed a Preliminary Response (Paper 10, “Prelim. Resp.”).

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

THRESHOLD.—The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Upon consideration of the Petition and the Preliminary Response, we conclude that Petitioner has established a reasonable likelihood that it would prevail with respect to claims 1 and 4 of the ’045 patent. Accordingly, we institute an *inter partes* review of claims 1 and 4 of the ’045 patent.

### *B. Related Matters*

Patent Owner has sued Petitioner for infringement of the ’045 patent in *Intellectual Ventures I LLC and Intellectual Ventures II LLC v. Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc.*, No. 1:13-cv-00453 (D.



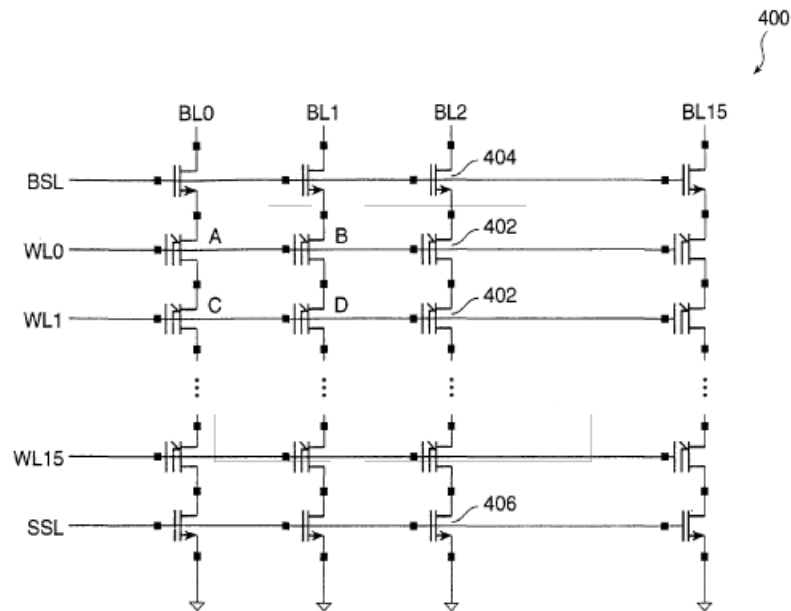


FIG. 4

Figure 4 depicts “a circuit schematic for an exemplary memory array made of flash cells.” *Id.* at 3:25-26. The disclosed memory array 400 in Figure 4 includes columns of serially connected flash memory cells located at the intersection of bit lines (BL0-BL15) and word lines (WL0-WL15). *Id.* at 6:22-28. Bit select control line (BSL) controls gate terminals of bit select transistors 404, which couple bit lines to memory cells. *Id.* at 30-31. Source select control line (SSL) controls gate terminals for source select transistors 406, which couple ground to memory cells. *Id.* at 31-32.

Table 1 of the '045 patent, reproduced below, provides a biasing scheme that discloses voltages that are applied to lines of the array to perform program, read, or erase operations for selected or unselected portions of the array.

TABLE I

Control Line	Erase	Program	Read	Condition
BSL	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	Selected
SSL	V <sub>ss</sub>	V <sub>ss</sub>	V <sub>cc</sub>	Selected
BLO	V <sub>cc</sub>	V <sub>ss</sub>	1.0–1.4V	Selected
BL1	V <sub>ss</sub>	V <sub>cc</sub>	0.5V	Unselected
WLD	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>	Unselected
WL1	-12 to -15V	15–20V	V <sub>ss</sub>	Selected

*Id.* at 6:37-45. Table 1 provides an example of a biasing scheme for an individual cell, showing voltages applied to various control lines (i.e, V<sub>cc</sub>, V<sub>ss</sub>, etc.), and the desired function (erase, program, or read) for the selected or unselected portions of the array. *Id.* at 6:48-56.

#### F. Claims

Challenged claims 1 and 4 are reproduced below:

1. An array of flash memory cells comprising:
  - a plurality of columns of serially connected flash memory cells, each memory cell having a gate terminal;
  - a plurality of bit lines respectively coupled to drain side of said plurality of columns of memory cells via a respective plurality of bit line select transistors, said plurality of bit line select transistors having gate terminals coupled to a bit line select control line;
  - a plurality of word lines, each one coupling to a gate terminal of one memory cell in each of said plurality of columns to form rows of memory cells with common gate terminals; and
  - a plurality of source select transistors respectively coupling a source side of said plurality of columns of memory cells to a logic low voltage, and having

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