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Tel: 571-272-7822 Entered: May 21, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION; TOSHIBA AMERICA, INC.; TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.; AND TOSHIBA AMERICA INFORMATION SYSTEMS, INC. Petitioner

v.

INTELLECTUAL VENTURES II LLC Patent Owner

Case IPR2014-00201 Patent 6,618,788

Before KEVIN F. TURNER, TREVOR M. JEFFERSON, and DAVID C. MCKONE, *Administrative Patent Judges*.

McKONE, Administrative Patent Judge.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108



I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively "Petitioner") filed a Corrected Petition (Paper 8, "Pet.") to institute an *inter partes* review of claims 1-27 of U.S. Patent No. 6,618,788 (Ex. 1001, "the '788 patent"). *See* 35 U.S.C. § 311. Intellectual Ventures II LLC ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp.").

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

THRESHOLD.—The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

We determine that the record before us does not demonstrate that there is a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim. We consequently deny the petition and decline to institute an *inter partes* review of the '788 patent.

B. Related Matters

Patent Owner has asserted the '788 patent against Petitioner in *Intellectual Ventures I LLC and Intellectual Ventures II LLC v. Toshiba Corporation et al.*, Case No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 4 at 2.



C. References Relied Upon

Petitioner relies upon the following prior art references:

Ex. 1003	Bastiani	US 6,609,167 B1	Aug. 19, 2003
			(filed Mar. 15, 2000)
Ex. 1005	McDonald	US 6,421,760 B1	July 16, 2002
			(filed Apr. 26, 2000)
Ex. 1006	Clay	US 5,465,338	Nov. 7, 1995

D. The Asserted Grounds

Petitioner contends that the challenged claims are unpatentable based on the following specific grounds (Pet. 7):

References	Basis	Claims challenged
Bastiani	§ 102(e)	1, 9, 10, 17-20, 22, 24
Bastiani	§ 103(a)	1-27
Bastiani and McDonald	§ 103(a)	7, 16, and 21
Bastiani and Clay	§ 103(a)	23

II. ANALYSIS

A. The '788 Patent

The '788 patent is directed to techniques for communicating over a serial communication connection, such as a universal serial bus ("USB"), between a computer host and a remote device that conforms to one or more of the Advanced Technology Attachment ("ATA") standards. Ex. 1001, Abstract. The ATA standards are promulgated by the American National Standards Institute ("ANSI") and define the physical, electrical, transport,



and command protocols for the attachment of devices to a computer host over an ATA bus. *Id.* at col. 1, ll. 11-22. An example of an ATA device is an internal hard drive of a personal computer. *Id.* at col. 1, ll. 17-19.

One embodiment of the invention of the '788 patent is shown in Figure 5, reproduced below:

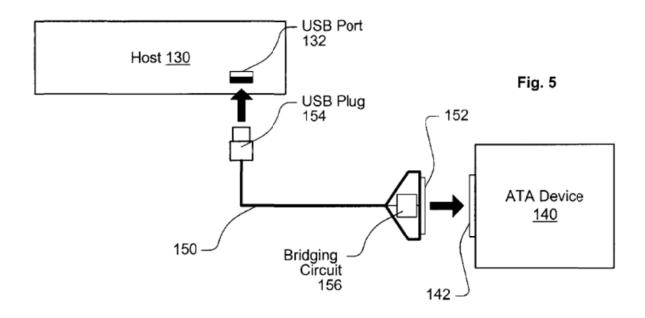


Figure 5 is a block diagram illustrating host 130 in communication with external ATA device 140. *Id.* at col. 4, ll. 63-65. The external ATA device can be, for example, an external hard drive. *Id.* at col. 3, ll. 55-57. Host 130 is connected to ATA Device 140 via smart cable 150 that plugs into USB port 132 on the host. *Id.* at col. 5, ll. 17-18, 21-22, 34-35. A connector 152 at the other end of the smart cable mates with socket 142 of ATA device 140. *Id.* at col. 5, ll. 34-35. Smart cable 150 includes bridging circuit 156 that converts data for communication between USB host 130 and ATA device 140. *Id.* at col. 5, ll. 39-43.



The host communicates with the ATA device by accessing, reading from, and writing to registers on the ATA device. *Id.*, col. 1, 1. 61-col. 2, 1. 23. For example, the ATA device executes register-driven commands from the host when those commands are written to the ATA device's "COMMAND" register. Id. at col. 2, 11. 1-9. The host includes a registerbased ATA host driver that formats ATA register accesses into ATA command blocks, which are packets. Id. at col. 4, ll. 11-14; col. 5, ll. 57-63; Fig. 7. The command blocks are sent from the host to the bridging circuit. *Id.* at col. 4, 11. 14-15; col. 5, 1. 64-col. 6, 1. 6; col. 6, 11. 26-34. At the bridging circuit, a controller receives an ATA command block, recognizes it as a command block, and parses it into a sequence of ATA register accesses. Id. at col. 6, 11. 7-14; Fig. 7. The controller then delivers the ATA register access sequence to an ATA register protocol adapter for execution. *Id.* at col. 6, ll. 14-15; Fig. 7. The ATA register protocol adapter contains the functionality for communicating asynchronously with the ATA device. *Id.* at col. 6, 11. 20-22.

When a given ATA register-delivered transaction requests the values stored in one or more of the ATA device's registers, the bridging circuit sends those values to the host in a packet format. *Id.* at col. 4, ll. 20-23.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A method of controlling an ATA device using packet-based communication between a host and a packet-to-ATA bridge, the method comprising

at the host:



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