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Paper 31
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MENTOR GRAPHICS CORPORATION,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-00287
Patent 6,836,420 B1

Before JENNIFER S. BISK, SCOTT A. DANIELS, and PHILIP J. HOFFMANN, *Administrative Patent Judges.*

DANIELS, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Mentor Graphics Corporation ("Petitioner") filed a Petition to institute an *inter partes* review of claims 1–3, 10–13, and 20 of U.S. Patent No. 6,836,420 B1 ("the '420 patent"). Paper 6 ("Pet.").[1] We instituted trial for claims 1–3, 10–13, and 20 of the '420 patent on certain grounds of unpatentability alleged in the Petition. Paper 9 ("Decision to Institute" or "Inst. Dec.").

After institution of trial, on September 17, 2014, Patent Owner, Synopsys, Inc., ("Patent Owner"), filed a Patent Owner Response ("PO Resp."), along with a Declaration by Patent Owner's Declarant, Dr. Brad Hutchings ("Hutchings Declaration"). Subsequently, Petitioner filed a Reply ("Reply") on December 12, 2014 and a Declaration in support of the Reply by Petitioner's Declarant, Mr. Edward Detjens ("Reply Declaration"). Paper 22.

A hearing for IPR2014-00287 was held on March 10, 2015. The transcript of the hearing has been entered into the record. Paper 30 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a).

Petitioner has shown by a preponderance of the evidence that claims 1–3, 10–13, and 20 of the '420 patent are unpatentable based on the combination of Vander Zanden and Shand. Petitioner has not shown that the challenged claims are unpatentable over any of the other proposed grounds.

[1] We refer to the corrected Petition filed January 15, 2014.

B. The '420 Patent

The '420 patent (Ex. 1001) generally relates to memory circuit design and specifically, a method and corresponding digital circuit design for resetable memory. Ex. 1001, 1:7–10. The '420 patent states, as a matter of background, that the circuitry for a conventional resetable memory unit is complicated and expensive because "each n wide storage cell is implemented with resetable flip-flops that are individually accessed via complicated multiplexing and control circuitry." *Id.* at 1:65–67. According to the patent, such a resetable memory unit is relatively slow and consumes more silicone surface area than a non-resetable memory unit. *Id.* at 2:3–6.

A solution to these challenges, proposed by the '420 patent, is designing resetable memory 220 as a combination of memory unit without reset 201, and memory unit with reset 205. *Id.* at 1:61–2:2, Fig. 2A. Figure 2A of the '420 patent, illustrating resetable memory 220, is reproduced below.

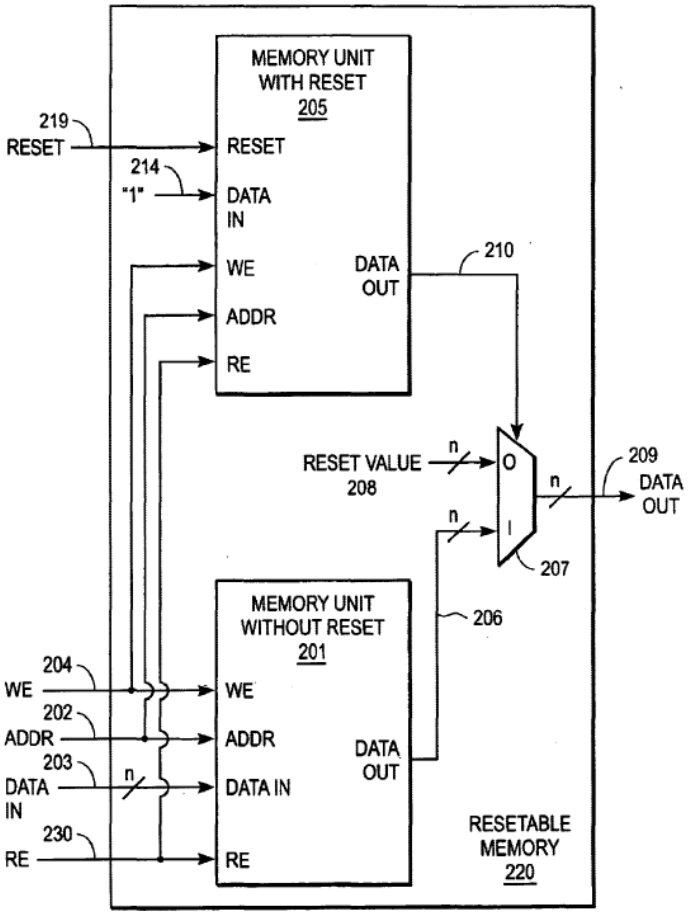

FIG. 2A

As depicted by Figure 2A, above, both memory unit without reset 201 and memory unit with reset 205 are connected to data out line 209 via multiplexor 207. Memory unit without reset 201 is larger in that it has a greater data width than memory unit with reset 205. *Id.* at 3:3–10. The '420 patent describes the smaller resetable memory having a cell word size less than the cell word size of the non-resetable memory. For example, the cell word size of the resetable memory is only one bit wide, so that the memory output from a cell is either a "1" or "0." *Id.* at 3:8–10. As explained below, the purpose of the combination is that the smaller memory with reset 205

"cost effectively disguises the inability of the larger memory 201 to reset its cells." *Id.* at 3:12–13.

Resetable memory 220 operates generally as follows: data is provided through data in line 203 to memory without reset 201, and is stored in a particular cell within the memory. *See id.*at Fig. 2A. The '420 patent refers to data called from memory without reset 201 as "actual memory unit data output 206." *Id.* at 3:26–30. Memory unit with reset 205 has a corresponding cell, in which a "1" from data in 214 is stored whenever write enable (WE) 204 of resetable memory 220 is activated. *Id.* at 4:1–3. The "1" from the memory unit with reset 205 instructs multiplexer 207 to output the actual memory unit data output 206 from memory 201 to data out line 209. *Id.* at 4:30–35. If memory unit with reset 205 is reset, a reset value, for example "0," is stored in memory unit 205, output to data out 210, and received by Multiplexer 207. In this circumstance, reset value 208 is output to data out line 209. *Id.* at 3:51–54. If no new data has been written to the particular cell in memory unit without reset 201 since its last reset, the multiplexer will continue to output the reset value "0,"[2] which remains in its storage cell until WE 204 line is activated again. *Id.* at 4:1–3. Accordingly, when a new value is written to the particular cell in memory unit without reset 201, the "0" will be over written with a "1" and the new value will be output by multiplexer 207 to data out line 209. *Id.* at 4:30–35. The '420 patent explains that "[i]n this manner, the circuit of FIG. 2[A] emulates the

[2] The reset may be a value besides "0," for instance FIG. 2B discloses an embodiment in which "a reset value function circuit 230 may be inserted between (and coupled to) the reset value 208 input of the multiplexer 207 and the address input 202 of the resetable memory 220." Ex. 1001, 4:67−5:3.

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