

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.;  
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.; and  
TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,  
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,  
Patent Owner.

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Case IPR2014-00310  
Patent 7,836,371

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Before KEVIN F. TURNER, TREVOR M. JEFFERSON,  
and DAVID C. MCKONE, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

## I. INTRODUCTION

### A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, “Petitioner”) filed a Corrected Petition (Paper 6, “Pet.”) to institute an *inter partes* review of claims 1–10 of U.S. Patent No. 7,836,371 (Ex. 1001, “the ’371 Patent”). *See* 35 U.S.C. § 311. Intellectual Ventures I LLC (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 12, “Dec.”), we instituted this proceeding as to claims 1–10.

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 19, “PO Resp.”) and Petitioner filed a Reply to the Patent Owner Response (Paper 21, “Reply”). An oral hearing (Paper 29, “Tr.”) was held on February 12, 2015.

### B. Related Cases

Patent Owner has asserted the ’371 Patent against Petitioner in *Intellectual Ventures I LLC and Intellectual Ventures II LLC v. Toshiba Corporation, Toshiba America Inc., Toshiba America Electrical Compenents, Inc. and Toshiba America Information Systems, Inc.* , Case No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 5, 2.

### C. References Relied Upon

Petitioner relies upon the following prior art references with respect to the instituted grounds:

Ex. 1004	Levine	US 5,802,273	Sept. 1, 1998
Ex. 1011	Whetsel	US 5,623,500	Apr. 22, 1997

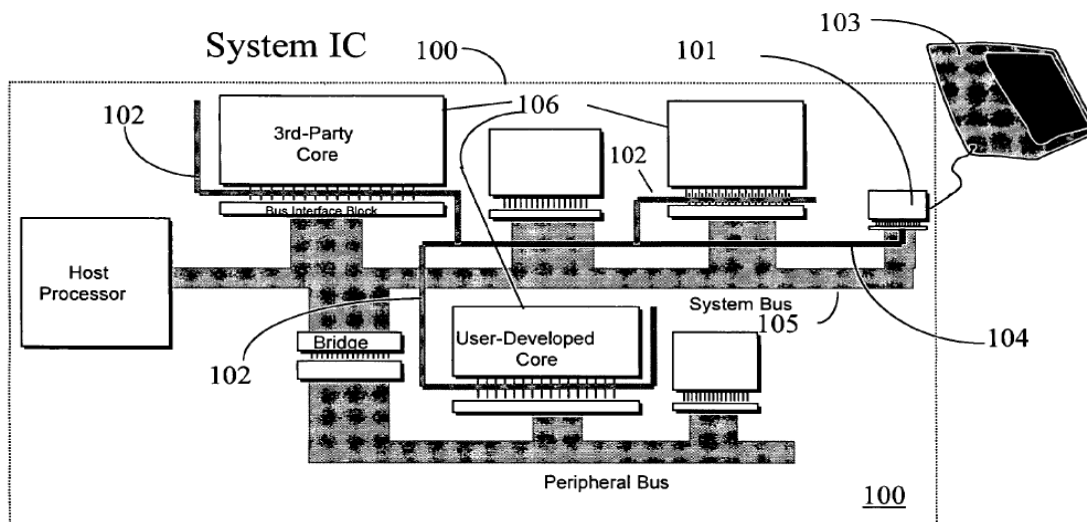
*D. The Instituted Grounds*

We instituted this proceeding based on the grounds of unpatentability set forth in the table below. Dec. 13.

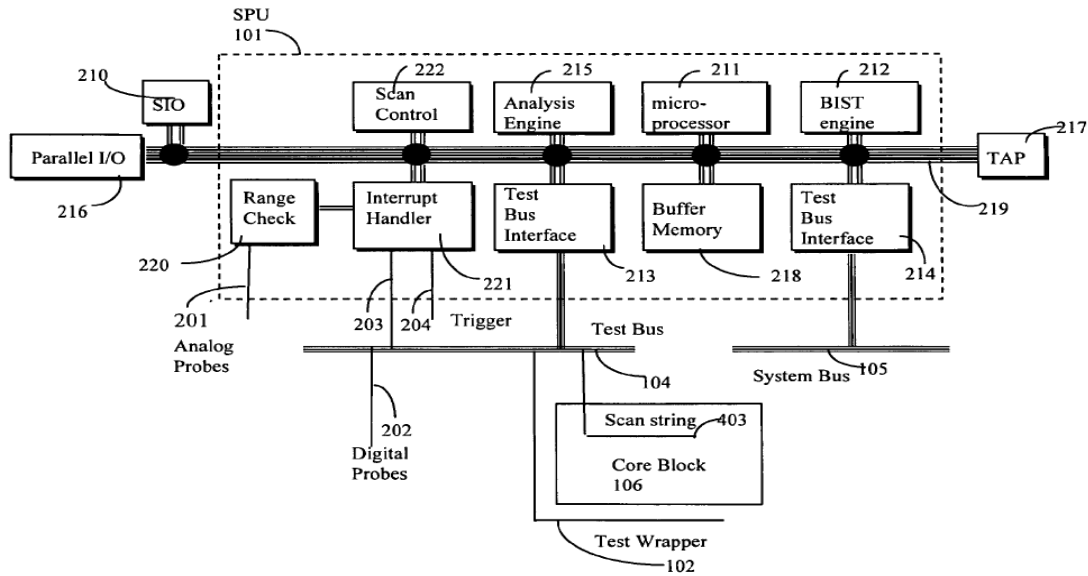
Reference(s)	Basis	Claim(s) Challenged
Levine	35 U.S.C. § 102	1–3 and 5–10
Levine and Whetsel	35 U.S.C. § 103	4

*E. The '371 Patent*

The '371 Patent is directed to on-chip circuits for the testing and diagnosis of problems in an integrated circuit, with the circuits used to observe the internal workings thereof. Ex. 1001, 1:24–27; 2:43–45. Figures 1b and 2, reproduced below, are illustrative:



*Figure 1b*



**Figure 2**

Figure 1b of the '371 Patent shows integrated circuit 100 having service processor unit (“SPU”) 101 and various circuit blocks connected by system bus 105. *Id.* at 6:15–27. SPU 101 is shown in greater detail in Figure 2 and includes a control unit (e.g., microprocessor 211), buffer memory unit 218, analysis engine 215, and processor bus 219. *Id.* at 6:23–40. Interfaces 210, 216, 217 provide communication between SPU 101 and the “external world” and interrupt handler 221 receives signals from trigger event lines 204 or test bus 104, which capture the signals. *Id.* at 6:40–59. Operation signals are captured by the SPU, and operation signals are analyzed, on-chip, by the SPU to determine whether a triggering event has occurred. *Id.* at 10:64–11:2, 11:55–59.

Claims 1, 2, and 7, reproduced below, are illustrative of the claimed subject matter:

1. An integrated circuit comprising:  
one or more logic blocks to generate one or more system-operation signals at one or more system-operation clock rates; and  
a service processor unit, said service processor unit comprising:  
a control unit;  
a buffer memory; and  
a multiplicity of selectable probes,  
wherein said service processor unit is adapted to perform capture and analysis of said system operation signals during normal system operation through said selectable probes.

2. The integrated circuit according to claim 1, further comprising at least one port selected from the group consisting of:  
a parallel I/O (PIO) port,  
a serial I/O (SIO) port, and  
a JTAG port;

wherein data and instructions are to be sent through at least one of said ports to said service processor unit from an external diagnostics console, and wherein result data is to be sent through at least one of said ports from said service processor unit to said external diagnostics console.

7. An integrated circuit comprising:  
one or more logic blocks to generate one or more system-operation signals at one or more system-operation clock rates;  
a system bus; and  
a service processor unit, said service processor unit comprising:  
a control unit;  
a buffer memory; and

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