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Paper 34
Entered: June 3, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

Case IPR2014-00317
Patent 5,687,132

Before KEVIN F. TURNER, TREVOR M. JEFFERSON, and DAVID C. MCKONE, *Administrative Patent Judges.*

MCKONE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, "Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–14 and 28–30 of U.S. Patent No. 5,687,132 (Ex. 1001, "the '132 patent"). *See* 35 U.S.C. § 311. Intellectual Ventures II LLC ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 11, "Dec."), we instituted this proceeding as to claims 1–14, 28, and 29.

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 20, "PO Resp.") and Petitioner filed a Reply to the Patent Owner Response (Paper 25, "Reply"). An oral hearing (Paper 33, "Tr.") was held on March 17, 2015.

B. Related Cases

Patent Owner has asserted the '132 patent against Petitioner in *Intellectual Ventures I LLC & Intellectual Ventures II LLC v. Toshiba Corp.*, Case No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 5, at 2. Patent Owner also has asserted the '132 patent in *Intellectual Ventures I LLC & Intellectual Ventures II LLC v. Hynix Semiconductor*, Case No. 2:11-cv-01145 (W.D. Wash.). Paper 5, at 2.

The '132 patent was under *ex parte* reexamination, Control Number 90/012,571 ("the '571 reexam"). Pet. 1. Prior to our Decision to Institute,

the Examiner in the '571 reexam mailed a Notice of Intent to Issue *Ex Parte* Reexamination Certificate ("NIRC") confirming claims 1, 2, 4, 6, 9, 10, 28, and 29.[1] Ex. 2001, at 3. Specifically, the Examiner concluded that each of the claims under reexamination includes a requirement of a single memory, rather than two separate memories, a limitation the Examiner found lacking in the cited prior art (which includes references that overlap with those raised in the Petition). *Id.* at 10–11. After our Decision to Institute, the Office issued an *Ex Parte* Reexamination Certificate, US 5,687,132 C1, confirming claims 1, 2, 4, 6, 9, 10, 28, and 29.

C. References Relied Upon

Petitioner relies upon the following prior art references:

Ex. 1004	Konishi	US 6,170,036 B1	Jan. 2, 2001 (filed Oct. 25, 1991)
Ex. 1005	Fujishima	US 5,353,427	Oct. 4, 1994

D. The Asserted Grounds

We instituted this proceeding based on the grounds of unpatentability set forth in the table below. Dec. 29.

References	Basis	Claims Challenged
Konishi	35 U.S.C. § 102(e)	1–14, 28, and 29
Fujishima	35 U.S.C. § 102(b)	1–12, 28, and 29

[1] The remaining claims of the '132 patent were not subject to reexamination. Ex. 2001, at 3.

E. The '132 Patent

The '132 patent is directed to multiple-bank computer memories. Ex. 1001, 1:6–8. In one example, a memory includes an array of memory cells divided into multiple subarrays. *Id.* at 3:4–9. The bitlines of the first subarray are coupled selectively to the bitlines of the second subarray by gating circuitry. *Id.* Figure 2A, reproduced below, is illustrative:

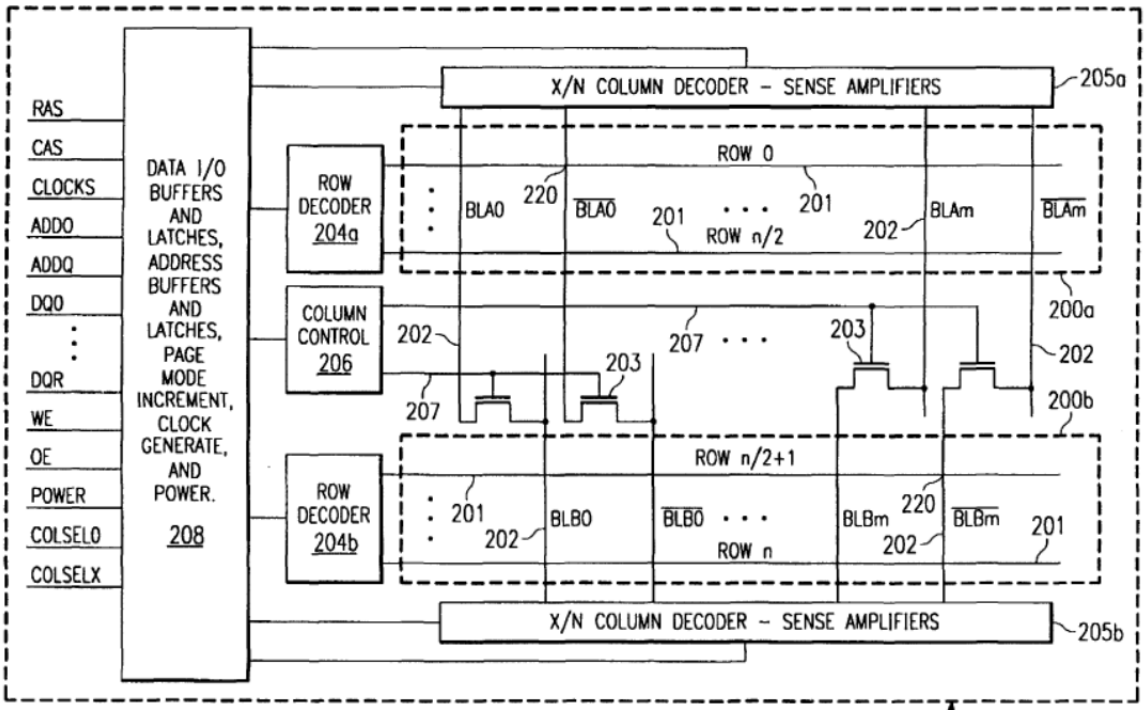

FIG. 2A

Figure 2A is a functional block diagram of memory 20. *Id.* at 7:5–6. Memory 20 includes a plurality of rows and columns of dynamic random access memory ("DRAM") cells partitioned into upper subarray 200a and lower subarray 200b. *Id.* at 7:10–16. Rows of cells are accessed using conductive wordlines (such as ROW 0 through ROW n/2 of upper subarray 200a and ROW n/2+1 through ROW n of lower subarray 200b) under the

control of row decoders (such as ROW DECODER 204a for upper subarray 200a and ROW DECODER 204b for lower subarray 200b). *Id.* at 7:39–46. Columns are arranged as pairs of bitlines (such as BLAm and $\overline{\text{BLAm}}$ for upper subarray 200a and BLBm and $\overline{\text{BLBm}}$ for lower subarray 200b). *Id.* at 7:47–59.

Bitlines in the upper subarray can be coupled to bitlines in the lower subarray using gates 203 under the control of column control circuitry 206. *Id.* at 8:45–47. For example, information in cells of upper subarray 200a can be transferred during a single gate delay to cells of lower subarray 200b by controlling gates 203 to couple bitlines BLAm and $\overline{\text{BLAm}}$ to BLBm and $\overline{\text{BLBm}}$. *Id.* at 8:47–51.

According to the '132 patent, the ability to transfer blocks of data between arrays of memory cells quickly is advantageous for computers driving multiple asynchronous display devices. *Id.* at 12:15–24.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory comprising:
>
> a first plurality of columns of memory cells each including at least one conductive bitline;
>
> a second plurality of columns of memory cells each including at least one conductive bitline; and
>
> a plurality of gates organized in independently controlled groups for selectively coupling said bitlines of a selected group of said first plurality of columns with a group of said bitlines of said second plurality of columns for transferring a at least one bit of data

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