

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., and
TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES II, LLC,
Patent Owner.

Case IPR 2014-00418
Patent 5,500,819

Held: May 6, 2015

BEFORE: JACQUELINE WRIGHT BONILLA, TREVOR M.
JEFFERSON, and DAVID C. McKONE, Administrative Patent
Judges.

The above-entitled matter came on for hearing on Wednesday, May 6,
2015, commencing at 1:15 p.m., at the U.S. Patent and Trademark
Office, 600 Dulany Street, Alexandria, Virginia.

Case IPR 2014-00418
Patent 5,500,819

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P R O C E E D I N G S

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JUDGE JEFFERSON: Good afternoon. We are here for IP2014-00418 in the matter of Toshiba, et al., versus Intellectual Ventures. I will quickly let you know that we have a new judge with us on panel, Jacqueline Wright Bonilla is here with us today. Judge Turner had a sudden illness and was unable to make the hearing, but we will certainly proceed and go forward on all the issues. If you give us a quick moment, I want to make sure I'm all up to speed here.

And the parties have an hour per side. You have been here before. And so if you will reserve your time, petitioner, at the end for rebuttal, please let us know and we'll let you know how close you are. And I'll say that the patent owner has an hour reserved as well. I will try to use the marker. If not, I will let you know. But I think we are ready to start when you are.

MR. HAMILTON: Good afternoon, Your Honors. Would you like a paper copy?

JUDGE JEFFERSON: I actually will take a paper copy.

MR. HAMILTON: May I approach?

JUDGE JEFFERSON: Yes, please.

MR. HAMILTON: Good afternoon. My name is Kevin Hamilton from DLA Piper on behalf of petitioner, Toshiba Corporation. With me is Gianni Minutoli, who is the lead counsel in this matter, and also with me is Gerald Sekimura, both from DLA

1 Piper. I would like to reserve 20 minutes of rebuttal time, if that's
2 okay.

3 JUDGE JEFFERSON: Okay. And you may begin.

4 MR. HAMILTON: So pulling up the slides here of the
5 petitioner's demonstratives and I want to look at slide number 2.
6 Slide 2 reminds us that the Board instituted this trial on the grounds
7 that the petitioner has a reasonable likelihood of showing claims 1
8 through 11 and 17 through 19 of the '819 patent are obvious over the
9 combination of three prior art references by the same inventor, the
10 Ogawa '577 reference, the Ogawa '045, and the Japanese Ogawa
11 application ending in '832.

12 Before I turn to slide 3, I want to give you an overview of
13 what I hope to do today. First, I would like to review the disclosure of
14 the '819 patent so that we all are talking about the same thing and to
15 briefly review some context building comments that were made
16 during the prosecution by the applicant. I would like to review the
17 claims of the patent, because as we all know, to determine the scope
18 of the patent, the court looks at the claims. I want to look at the patent
19 owner's argument which hinges completely upon convincing this
20 panel to read limitations of a preferred embodiment into the claim.
21 And finally, I would like to look at the Ogawa references to see how
22 their combination renders the challenged claims of the '819 patent
23 obvious.

24 Go ahead and turn to slide 3. Here in slide 3 we are looking
25 at a portion excerpts of the '819 patent specification. The '819 patent

1 discloses "circuit systems and methods for improving page access and
2 blocked transfers in a memory system." It's the title of the patent. It's
3 also the first sentence of the specification. The specification discloses
4 circuitry intended to improve page accesses and blocked transfers.

5 As shown in the underlying sections on the left-hand side of
6 slide 3, the specification discloses some well-known circuit elements
7 such as an array of memory cells, address to code circuitry, sense
8 amplifiers and even though it's not shown here, also control circuitry.

9 The background section of the specification confirms that
10 memory arrays, address decoding circuitry, sense amplifiers and
11 controllers were all well known in the art at the time the '819 patent
12 application was filed.

13 We turn to slide 4, in the underlying portion on the left-hand
14 side we have an excerpt from the '819 patent specification. The
15 underlying portion shows that the memory disclosed in the '819
16 specification also discloses -- also contains at least two sets of
17 latching circuitry that are coupled to the master sense amplifiers.
18 Each of the disclosed memory elements is shown in the embodiment
19 depicted in the Figure 2 of the '819 patent which is shown on slide 5.

20 Here on slide 5, we see Figure 2 from the '819 patent. We
21 see a conventional end-by-end array of memory cells, a conventional
22 row decoder 205 up on the top left, on the left of the memory array.
23 On the bottom we see a conventional column decoder labeled 213.
24 We see below the memory array are conventional sense amplifiers

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