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Paper 28
Entered: August 7, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

Case IPR2014-00418
Patent 5,500,819

Before JACQUELINE WRIGHT BONILLA, TREVOR M. JEFFERSON, and DAVID C. McKONE, *Administrative Patent Judges.*

JEFFERSON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, "Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–11 and 17–19 of U.S. Patent No. 5,500,819 (Ex. 1001, "the '819 patent"). *See* 35 U.S.C. § 311. Intellectual Ventures II LLC ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 7, "Dec."), we instituted this proceeding as to claims 1–11 and 17–19 of the '819 patent. Dec. 19.

Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp.") and Petitioner filed a Corrected Petitioner's Reply to Patent Owner's Response (Paper 23, "Reply"). An oral hearing in this matter was held on May 6, 2015 (Paper 27, "Tr.").

We have jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, Petitioner has demonstrated by a preponderance of the evidence that claims 1–11 and 17–19 of the '819 patent are unpatentable.

B. Related Matters

Patent Owner has sued Petitioner for infringement of the '819 patent in *Intellectual Ventures I LLC v. Toshiba Corp.*, No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 5 (Patent Owner's Mandatory Notices).

C. The '819 Patent

The '819 patent, titled "Circuits, Systems and Methods for Improving Page Accesses and Block Transfers In A Memory System," issued on March 19, 1996,

and addresses control circuitry that controls the exchange of data between read/write circuitry and first and second slave circuitry. Ex. 1001, Abstract. The '819 patent discloses circuits for improving page accesses and block transfers in memory. *Id*. at 1:7–10. The "invention provide[s] for the construction of a memory which includes an array of volatile memory cells, address decode circuitry for selecting rows and/or columns of cells in the memory array, and master sense amplifier circuitry for reading and writing data into those selected cells." *Id*. at 2:52–57. The invention also includes "[a]t least two sets of latching circuitry . . . coupled to the master sense amplifiers for temporarily storing data being exchanged with the master sense amplifiers during read and write operations to the array of memory cells." *Id*. at 2:57–61.

Figure 2 of the '819 patent, shown below, provides an exemplary block diagram of the memory system disclosed.

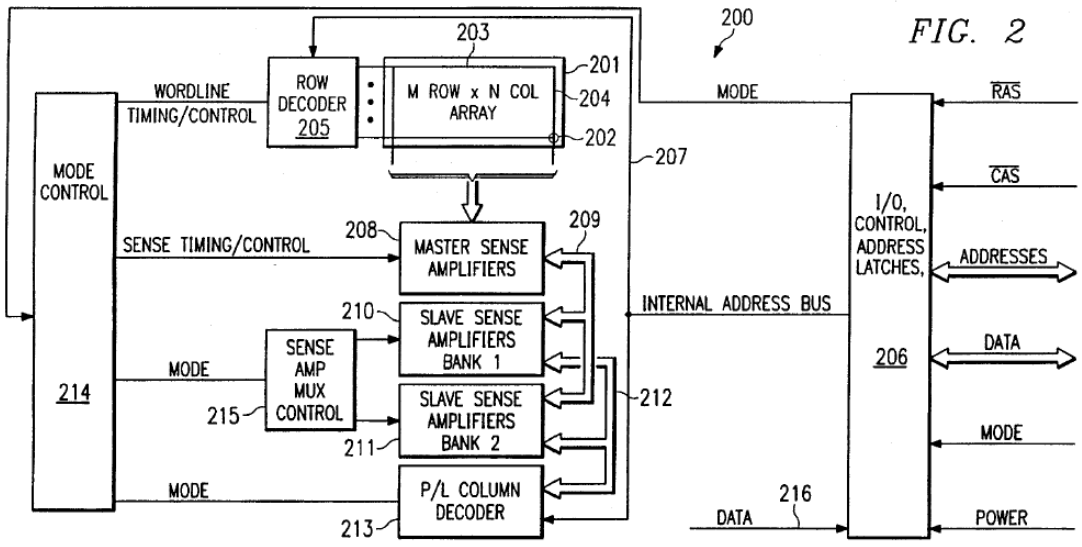

Figure 2 depicts a block diagram of memory system 200 with an M x N array of flash memory cells 201, with wordlines (rows) 203 and bitlines (columns) 204. *Id*. at 5:52–57, 3:25–26. Representative memory cell 202 is located at the

intersection of wordline 203 and bitline 204. *Id*. at 5:58–60. "[Bitlines] 204 of memory array 201 are coupled to a bank 208 of master sense amplifiers," which are coupled via "bus 209 to a first bank 210 (bank 1) of slave sense amplifiers and a second bank 211 (bank 2) of slave sense amplifiers." *Id*. at 6:8–12. "Slave sense amplifier banks 210 and 211 are further coupled by a local data I/O bus 212 to column decoder circuitry 213." *Id*. at 6:12–14. The challenged claims are directed to a memory that includes control circuitry that controls the sensing of data from cells via the master sense amplifiers, the temporary storage of those data in the first and second bank of slave sense amplifiers, and the rewriting of those data back in the memory array at the same or different locations.

D. Illustrative Claims

Illustrative independent claims 1, 7, and 17 (Ex. 1001, 8:20–44 (claim 1), 8:60–9:20 (claim 7), 11:8–12:3 (claim 17)) are reproduced below:

> 1. A memory comprising:
>
> an array of rows and columns of volatile memory cells;
>
> addressing circuitry for providing access to selected ones of said memory cells;
>
> master read/write circuitry for reading and writing data into said selected ones of said cells;
>
> first slave circuitry for storing data for exchange with said master read/write circuitry;
>
> second slave circuitry for storing data for exchange with said master read/write circuitry; and
>
> control circuitry for controlling exchange of data between said master read/write circuitry and said first and second slave circuitry, said control circuitry operable during a move operation to:

control sensing by said master read/write circuitry of data from a said row in said array selected by said addressing circuitry;

control transfer of said data from said master read/write circuitry to a selected one of said first and second slave circuitry; and

control writing of said data through said master read/write circuitry to a second said row in said array selected by said addressing circuitry.

7. A memory system comprising:

an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline;

a row decoder coupled to said wordlines;

a bank of master sense amplifiers coupled to said bitlines;

a plurality of banks of slave sense amplifiers coupled to said master sense amplifiers;

a column decoder coupled to each of the plurality of banks of slave sense amplifiers; and

control circuitry coupled to said row decoder, said bank of master sense amplifiers and said banks of slave sense amplifiers, said control circuitry including mode control circuitry coupled to said row decoder and said master sense amplifiers and multiplexer control circuitry coupled to said mode control circuitry and said plurality of banks of slave sense amplifiers, said control circuitry operable during a move operation to:

control sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

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