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Paper 55
Entered: November 30, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MARVELL SEMICONDUCTOR, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2014-00548
Patent 5,712,870

Before THOMAS L. GIANNETTI, JAMES A. TARTAL, and PATRICK M. BOUCHER, *Administrative Patent Judges*.

TARTAL, *Administrative Patent Judge.*

FINAL WRITTEN DECISION

35 U.S.C. § 318(a) and *37 C.F.R. § 42.73*

Petitioner, Marvell Semiconductor, Inc., filed a substitute corrected Petition requesting an *inter partes* review of claims 1–20 of U.S. Patent No. 5,712,870 ("the '870 patent"). Paper 12 ("Pet."). Based on the information provided in the Petition, we instituted a trial pursuant to 35 U.S.C. § 314(a) of: (1) claims 1, 2, 4–6, 8, 10, 11, 13, 14, and 16–20 as obvious over Fischer[1] and Nakamura[2] under 35 U.S.C. § 103(a); and, (2) claims 9 and 15 as obvious over Fischer, Nakamura, and Tsuda.[3] Paper 16 ("Institution Decision" or "Inst. Dec."). We did not institute trial on claims 3, 7, or 12. *Id*. Additionally, in a separate order, we vacated our decision to institute trial on claims 8 and 9, which depend from claim 7, and dismissed *inter partes* review of those claims. Paper 54.

After institution of trial, Patent Owner, Intellectual Ventures I LLC, filed a Patent Owner's Response (Paper 30, "Response" or "PO Resp.") and Petitioner filed a Corrected Reply (Paper 53, "Reply"). The Petition is supported by a Declaration (Exhibit 1003) and a Reply Declaration (Exhibit 1013) of Prof. Zhi Ding. Patent Owner filed observations on the cross-examination of Prof. Ding (Paper 43), and Petitioner filed a response to Patent Owner's observations (Paper 46). Patent Owner also filed a Motion to Exclude (Paper 44) portions of Prof. Ding's Reply Declaration (Exhibit 1013), to which Petitioner filed an opposition (Paper 47) and Patent Owner further filed a reply (Paper 48). The Patent Owner Response is supported by a Declaration of Dr. Ghobad Heidari (Ex. 2006).

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[1] U.S. Patent No. 5,371,734, issued Dec. 6, 1994 (Ex. 1004, "Fischer")
[2] U.S. Patent No. 4,856,027, issued Aug. 8, 1989 (Ex. 1005, "Nakamura")
[3] U.S. Patent No. 5,619,507, issued Apr. 8, 1997 (Ex. 1009, "Tsuda") from U.S. Application Number 08/268,454 filed June 30, 1994.

A transcript of the Oral Hearing conducted on September 11, 2015, is entered as Paper 50 ("Tr.").

We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, Petitioner has shown by a preponderance of the evidence that claims 1, 4–6, 10, and 13–20 of the '870 patent are unpatentable.

I. BACKGROUND

A. The '870 patent (Ex. 1001)

The '870 patent issued January 27, 1998, from U.S. Application No. 08/508,462, filed July 31, 1995. Ex. 1001. The '870 patent, titled "Packet Header Generation and Detection Circuitry," describes a device for receiving and transmitting direct sequence spread spectrum ("DSSS") signals using a single integrated device for converting and demodulating an RF signal into a serial data signal. *Id*. at Abstract. In particular, according to the '870 patent, "[c]ritical timing relationships during the acquisition and demodulation of the received signal are satisfied by the use of an integrated circuit specially designed to perform all operations needed to convert the physical signal to a[] media access circuit level data signal." *Id*.

According to the '870 patent, standards for the communication of signals in a wireless Local Area Network ("LAN") system typically utilize a message format consisting of a fixed length preamble having fields for power ramping, synchronization, a signal field, a descrambling seed, and a unique word identifier, followed by the data, and then a Cyclical Redundancy Check ("CRC") field. *Id*. at 4:41–49. The preamble may be modulated onto the carrier signal using digital Binary Phase Shift Keyed

("BPSK") modulation, and the data and CRC signals may be modulated using either BPSK or Quaternary Phase Shift Keyed ("QPSK") modulation. *Id*. at 4:49–56. As explained by Patent Owner, the '870 patent "is directed to circuitry for demodulating a header portion of a signal that has been BPSK modulated and for demodulating a data portion of the signal that has been QPSK modulated." PO Resp. 6.

Figure 2 of the '870 patent is reproduced below.

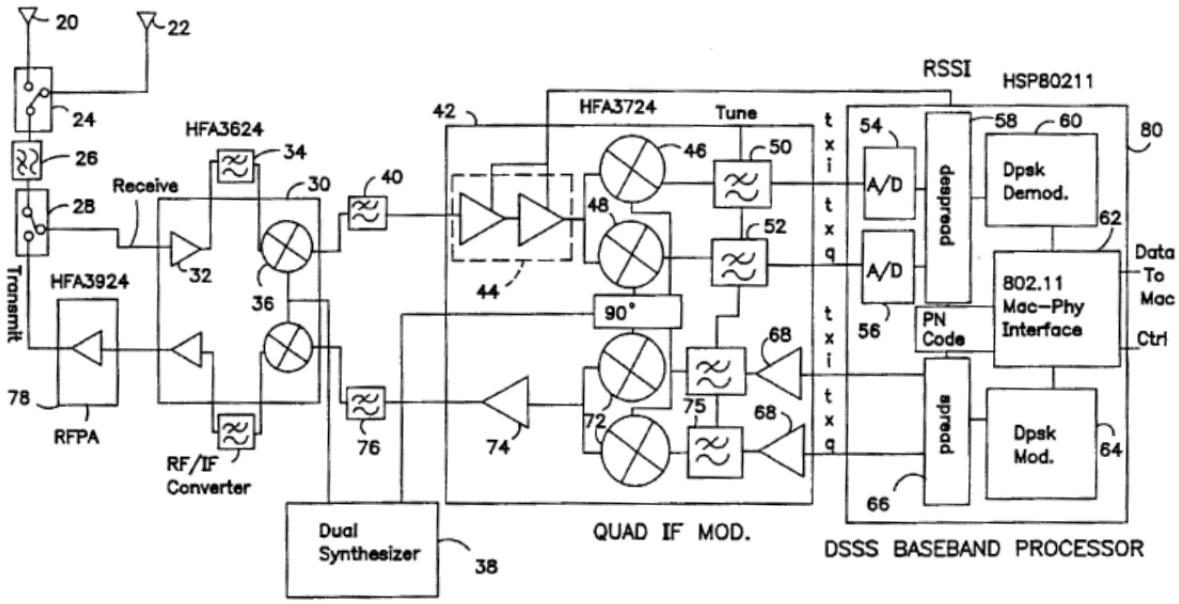

FIG. 2

Figure 2 illustrates a functional block diagram of a communications transceiver, including antennae 20, 22 and selector switch 28 that connects antenna coupler 26 to either a transmit circuit or a receive circuit. Ex. 1001, 4:59–66. In the receive circuit, the incoming signal is first amplified by RF/IF converter 30, and then further amplified by quadrature Intermediate Frequency ("IF") modulator/demodulator 42. The amplified signal may be

split into I and Q (in-phase (real) and quadrature (imaginary)) components. *Id*. at 5:5–15. The I and Q component signals may be provided to a baseband processor that converts the analog signals to digital signals at A/D converters 54, 56, and then despreads the spread spectrum signal through despreader 58. *Id*. at 5:24–28. The despread signal may be demodulated by Differential Phase Shift Keyed ("DPSK") demodulator 60 to provide a digital data signal to be passed to an application system through interface circuit 62. Data to be transmitted may follow a similar return path, passing through modulator 64, data spreader 66, and modulator/demodulator 42; after which it is upconverted to RF by RF/IF converter 30 and then provided to one of the antennae, as selected by switch 24.

Figure 3 of the '870 patent is reproduced below.

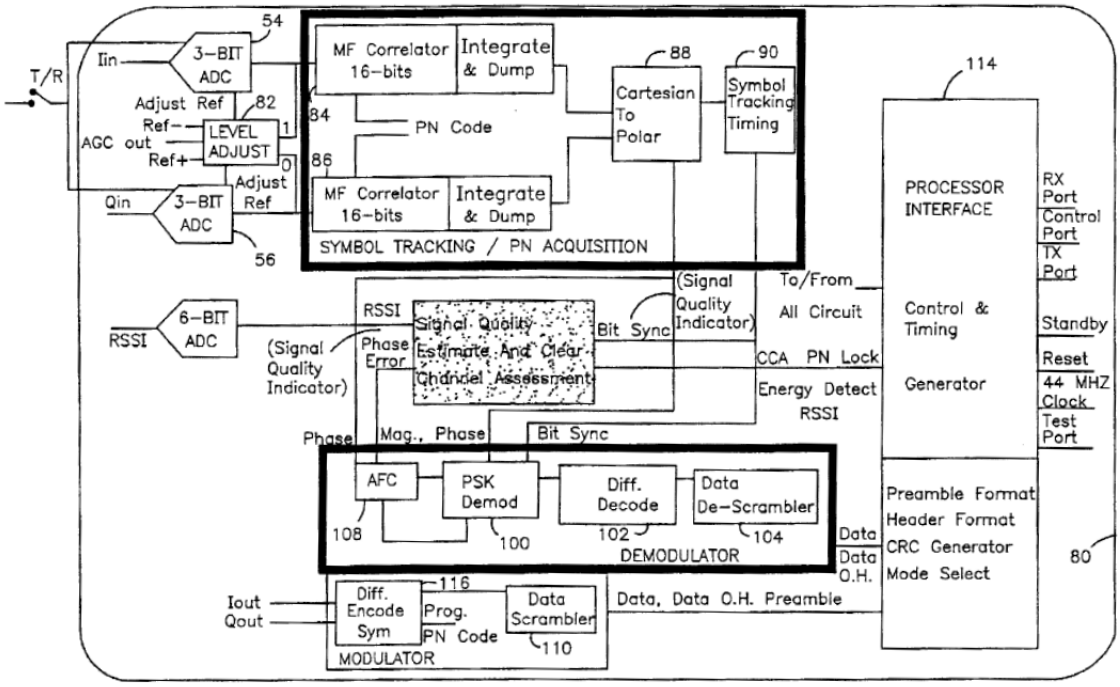

FIG. 3

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