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Paper No. 12
Filed: September 29, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORP., SONY ELECTRONICS INC.,
SONY MOBILE COMMUNICATIONS AB,
SONY MOBILE COMMUNICATIONS (USA) INC.,
LG ELECTRONICS, INC., LG ELECTRONICS USA, INC., and
LG ELECTRONICS MOBILECOMM USA, INC.,
Petitioner,

v.

MEMORY INTEGRITY, LLC,
Patent Owner.

Case IPR2015-01376
Patent 7,296,121 B2

Before JENNIFER S. BISK, NEIL T. POWELL, and KERRY BEGLEY, *Administrative Patent Judges*.

BEGLEY, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review, Motion for Joinder
35 U.S.C. § 315(c); 37 C.F.R. §§ 42.108, 42.122

Sony Corp., Sony Electronics Inc., Sony Mobile Communications AB, Sony Mobile Communications (USA) Inc. (collectively, "Sony"), LG Electronics, Inc., LG Electronics USA, Inc., and LG Electronics Mobilecomm USA, Inc. (collectively, "LG") filed a Petition requesting *inter partes* review of claims 1–3, 8, 11, 12, and 15–25 of U.S. Patent No. 7,296,121 B2 (Ex. 1001, "the '121 patent"). Paper 3 ("Pet."). Along with the Petition, Sony and LG filed a motion for joinder with IPR2015-00159, *Apple Inc. v. Memory Integrity, LLC*, a pending *inter partes* review involving the '121 patent. Paper 4 ("Mot.").[1]

Memory Integrity, LLC ("Patent Owner"), with prior authorization from the Board, filed a notice that it seeks to rely on its Preliminary Response filed in IPR2015-00159. Paper 10. We treat Patent Owner's Preliminary Response in IPR2015-00159 as having been filed in this case. *See* IPR2015-00159, Paper 11 ("Prelim. Resp.").

Patent Owner has not filed an opposition to the Motion for Joinder. Sony and LG represent in the Motion that the petitioners in IPR2015-00159 have no objection to the requested joinder. *See* Mot. 7.

For the reasons set forth below, we conclude that Sony and LG have shown that the Petition warrants institution of *inter partes* review of claims 1–3, 8, 11, and 15–25 of the '121 patent, but does not warrant

[1] We note that the one-year time bar of 35 U.S.C. § 315(b) and 37 C.F.R. § 42.101(b) does not apply to Sony and LG's request for joinder with IPR2015-00159. *See* Mot. 3; 35 U.S.C. § 315(b) ("The time limitation set forth in the preceding sentence shall not apply to a request for joinder under subsection (c)."); 37 C.F.R. §§ 42.101(b), 42.122(b) ("The time period set forth in § 42.101(b) shall not apply when the petition is accompanied by a request for joinder.").

institution of review of claim 12. This conclusion is consistent with our institution decision in IPR2015-00159. We exercise our discretion to join Sony and LG as petitioners in IPR2015-00159.

I. BACKGROUND

A. RELATED PROCEEDINGS

Sony and LG indicate that Patent Owner has asserted the '121 patent in numerous cases filed in the U.S. District Court for the District of Delaware. Pet. 2–3. In addition, the '121 patent is the subject of pending *inter partes* review proceedings, including IPR2015-00159 as well as IPR2015-00158 and IPR2015-00163. *Id.* at 3. The '121 patent also was the subject of IPR2015-00161 and IPR2015-00172, in which *inter partes* review was not instituted. *Id.*

In IPR2015-00159, filed by Apple Inc., HTC Corporation, HTC America, Inc., Samsung Electronics Co. Ltd., Samsung Electronics America, Inc., and Amazon.com, Inc. (collectively, "IPR2015-00159 Petitioners"), we instituted *inter partes* review of claims 1–3, 8, 11, and 15–25 of the '121 patent on the grounds of unpatentability asserted in the present Petition. *Apple Inc. v. Memory Integrity, LLC*, Case IPR2015-00159 (PTAB May 11, 2015) (Paper 12) ("IPR2015-00159 Inst. Dec.").

B. THE '121 PATENT

The '121 patent relates to techniques to reduce memory transaction traffic and to improve data access and cache coherency in systems with multiple processors connected using point-to-point links. Ex. 1001, 1:22–25, 2:39–47. The '121 patent explains that cache coherency problems can arise in a system with multiple processors, each with an individual cache

memory, because the system may contain multiple copies of the same data. *Id.* at 1:26–38. For example, if the caches of two different processors have a copy of the same data block and both processors "attempt to write new values into the data block at the same time," then the two caches may have different data values and the system may be "unable to determine what value to write through to system memory." *Id.* at 1:37–45.

The '121 patent discloses a computer system with processing nodes, each with a cache memory, connected by a point-to-point architecture. *Id.* at [57], 2:48–62. The system also includes a "probe filtering unit" that can receive a probe from a processing node. *Id.* at [57], 2:52–65, 5:45–47. The '121 patent defines a probe as "[a] mechanism for eliciting a response from a node to maintain cache coherency in a system." *Id.* at 5:45–47.

The probe filtering unit then can evaluate the probe based on probe filtering information and transmit the probe to selected processing nodes. *Id.* at [57], 2:52–3:5, 14:50–52; *see id.* at 28:29–58, 29:43–46. The '121 patent explains that probe filtering information is "[a]ny criterion that can be used to reduce the number of clusters or nodes probed." *Id.* at 14:50–52.

The probe filtering unit also may be operable to accumulate responses from the selected processing nodes and to respond to the node from which the probe originated. *Id.* at 3:5–8, 28:59–67, 29:46–51. Figure 18 of the patent is reproduced below.

Figure 18

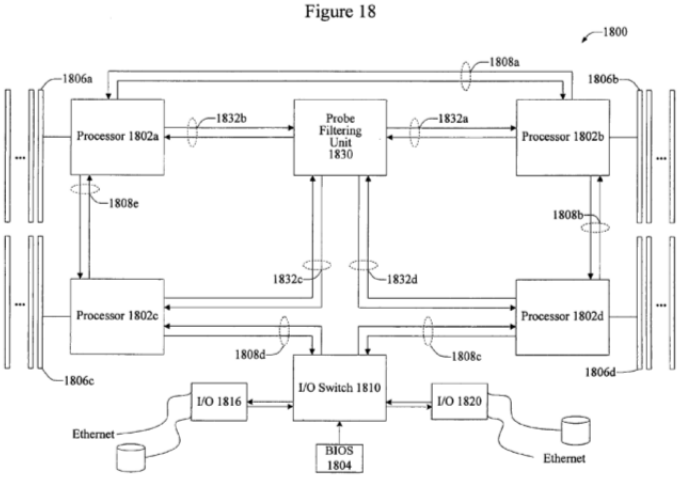

Figure 18 is a diagrammatic representation of a multiple processor system with a probe filtering unit. *Id.* at 3:61–63, 26:58–27:20, Fig. 18. Specifically, Figure 18 depicts multiple processor system 1800 with processing nodes 1802a–d interconnected by point-to-point communication links 1808a–e. *Id.* at 26:58–27:1. System 1800 also includes probe filtering unit 1830 as well as I/O switch 1810, one or more Basic I/O systems ("BIOS") 1804, I/O adapters 1816, 1820, and a memory subsystem with memory banks 1806a–d. *Id.* at 3:61–63, 26:58–27:20, Fig. 18.

Claims 1, 16, and 25 of the '121 patent are independent claims. Claim 1 is illustrative of the claimed subject matter and recites:

> 1. A computer system comprising a plurality of processing nodes interconnected by a first point-to-point architecture,
>
> each processing node having a cache memory associated therewith,
>
> the computer system further comprising a probe filtering unit which is operable to receive probes corresponding to memory lines from the processing nodes and to transmit the probes only to selected ones of the processing nodes with reference to probe filtering information representative of states associated with selected ones of the cache memories.

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