

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Conley:

U.S. Pat. No. 8,316,177

Issued: November 20, 2012

Title: PARTIAL BLOCK DATA
PROGRAMMING AND READING
OPERATIONS IN A NON-VOLATILE
MEMORY

Petition for *Inter Partes* Review

Attorney Docket No.:
337722-70.177

Customer No.: 26379

Petitioner: Apple Inc.
Real Party-in-Interest: Apple Inc.

PETITION FOR *INTER PARTES* REVIEW

Mail Stop Patent Board
Patent Trial and Appeal Board
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the provisions of 35 U.S.C. §§ 311-319, Apple Inc. (hereinafter “Petitioner”) hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-9 of United States Patent No. 8,316,177 (“the ’177 patent”)

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EXHIBITS

- Ex. 1001 U.S. Patent No. 8,316,177 (“the ’177 patent”)
- Ex. 1002 File History for the ’177 patent
- Ex. 1003 U.S. Patent No. 5,457,658 (“Niijima”)
- Ex. 1004 Flash Memories, edited by Cappelletti, et al (1999)
 (“Cappelletti”)
- Ex. 1005 U.S. Patent No. 5,627,783 (“Miyauchi”)
- Ex. 1006 PC Card Standard, Volumes 1 and 3 (1999) (“PC Card
 Standard”)
- Ex. 1007 Declaration of Dr. Vivek Subramanian
- Ex. 1008 CV of Dr. Vivek Subramanian
- Ex. 1009 Excerpt from Microsoft Computer Dictionary, 4th edition
 1999, “controller”

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