Trials@uspto.gov
571-272-7822

Paper 44
Entered: December 6, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00320
Patent 6,169,503 B1

Before KARL D. EASTHOM, JAMES B. ARPIN, and
KEVIN W. CHERRY, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* EASTHOM.

Opinion Concurring by *Administrative Patent Judge* ARPIN.

EASTHOM, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
AFTER REHEARING
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1 and 8–10 of U.S. Patent No. 6,169,503 B1 ("the '503 patent," Ex. 1001). Pet. 1. Innovative Memory Systems, Inc. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp.").

We instituted trial for claims 1 and 8–10 (the "challenged claims"). Paper 10 ("Institution Decision" or "Inst. Dec."). Patent Owner then disclaimed claim 1 and filed a Response. Paper 23 ("PO Resp."), 2 n.1. Petitioner followed with a Reply. Paper 25 ("Pet. Reply"). The record includes a transcript of the Oral Hearing. Paper 39 ("Tr.").

We issued a First Final Written Decision. Paper 40 ("1st FWD"). Subsequently, Patent Owner filed a Request for Rehearing. Paper 41 ("Rehearing Request" or "Reh'g Req."). Based on the Rehearing Request, the Board withdrew the First Final Written Decision as set forth in the Decision on Rehearing. Paper 42 (Withdrawal of Final Written Decision and Authorization of Sur-Reply) ("Rehearing Decision" or "Reh'g Dec."). As set forth in the Rehearing Decision, we granted Patent Owner's request for additional briefing in the form of a Sur-Reply (Paper 43). *See* Reh'g Dec. 5–6; Sur-Reply.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision After Rehearing issues pursuant to 35 U.S.C. § 318(a). After reconsidering the record in light of Patent Owner's Sur-Reply and Rehearing Request, we determine Petitioner has shown by a preponderance of the evidence that claims 8–10 of the '503 patent are unpatentable.

A. Related Matters

According to the parties, a co-pending lawsuit involves the '503 patent and other patents owned by Patent Owner: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del. 2014). *See* Pet. 2; Paper 6, 1.

Petitioner filed petitions challenging the patentability of certain subsets of claims in patents involved in the Delaware litigation: (1) U.S. Patent No. 7,045,849 (Case IPR2016-00322); (2) U.S. Patent No. 7,495,953 B2 (Case IPR2016-00323); (3) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324) (institution denied); (4) U.S. Patent No. 7,000,063 B2 (Case IPR2016-00325) (institution denied); (5) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326) (terminated, adverse judgment requested by patent owner); (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327) (terminated, adverse judgment requested by patent owner); and (7) U.S. Patent No. 6,901,498 B2 (Case IPR2016-00330). *See* Pet. 2–3; Paper 6, 1.

B. The '503 Patent

The '503 patent describes analog-to-digital converters ("ADCs"). Ex. 1001, Abstract. An ADC converts an analog signal, such as a voltage, to a digital value. *Id.* at 1:14–17. For example, an analog audio or image signal may be converted into digital form by quantizing digital samples of the signal as represented by a number of bits. *See id.* at 1:14–42.

Instead of using comparators, in order to obtain relatively higher speed, lower power, and smaller circuit areas, the '503 patent describes using a plurality of transistors having different threshold voltages (referred to alternatively as memory or reference cells) that conduct at such different threshold voltages in response to an analog input voltage. *Id.* at 2:24–63.

These threshold voltages may be within read only memories (ROMs) or within programmable transistors. *See id.* at 2:60–63, 3:6–16.

The ROMs or transistors may be arranged in different types of arrays. *Id.* at 2:60–3:23. For example, "transistors having programmable threshold voltages . . . may be in an array including multiple rows and columns of memory cells." *Id.* at 3:14–16. However, "[o]ther array configurations are possible." *Id.* at 4:39–40. In one embodiment, "ADC 300 uses a row of reference cells." *Id.* at 4:37.

Figure 5B, reproduced below, depicts a disclosed embodiment having multiple rows of memory cells or programmable transistors in ADC 500:

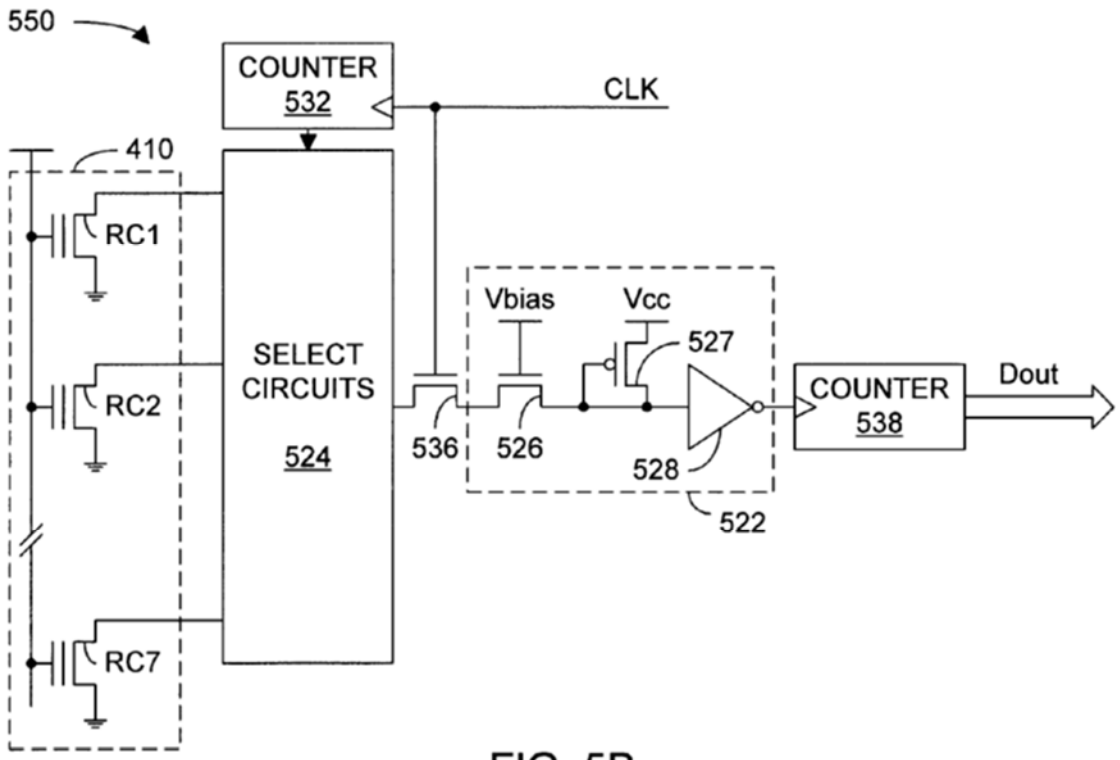

FIG. 5B

With respect to Figure 5B, to convert an analog signal Ain into a signal in digital format Dout, "sense circuit 522 generates a pulse for each

reference cell RC1 to RC7 that conducts. Counter 538 counts pulses from sense circuit 522 and outputs the resulting count as signal Dout." Ex. 1001, 7:5–8.

Figures 5A and 5B show that Ain connects to all of the rows, such that embodiments represented by those figures use all the rows simultaneously in a specific digital conversion. The Specification also describes modifying embodiments including those represented by Figures 5A and 5B, such that "[i]nstead of simultaneously applying analog input voltage Ain to all of the reference cells associate with a conversion, the ADC applies signal Ain only to [sic] reference cell (or one row of reference cells) at a time." *See id.* at 7:11–14. At least one such embodiment includes a row decoder to select successive rows. *See id.* at 7:14–16. In an embodiment that selects successive rows, "signal CSEL initially has a value that selects one of the rows associated with the desired conversion, and circuit 740 determines the conductivity states of the reference cells in the current row. . . . The control circuit continues to change signal CSEL until a row is found in which some reference cells conduct and others don't conduct." *Id.* at 10:14–23 (discussing Figure 7A and AADAC 700).[1]

[1] AADAC refers to a dual converter (which uses the same reference cells) for both an analog to digital and digital to analog conversion. *See* Ex. 1001, 9:32–51.

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