

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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ARM, Ltd.  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1  
Patent Owner.

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Case IPR2016-00825  
Patent RE43, 729

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Before TRENTON A. WARD, GEORGIANNA W. BRADEN, and  
MONICA S. ULLAGADDI, *Administrative Patent Judges*.

ULLAGADDI, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
37 C.F.R. § 42.108

## I. INTRODUCTION

### A. Background

ARM, Ltd. and ARM, Inc. (collectively, “Petitioner”)<sup>1</sup> filed a Petition (Paper 1, “Pet.”) for *inter partes* review of claims 21 and 22 of U.S. Patent No. RE43,729 (Ex. 1001, “the ’729 patent”). Godo Kaisha IP Bridge 1 (“Patent Owner”)<sup>2</sup> timely filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Thereafter, on September 7, 2016, a conference call was held among the parties and the Board.<sup>3</sup>

Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Upon consideration of the Petition, the Petitioner’s supporting evidence, as well as Patent Owner’s Preliminary Response and supporting evidence, and for the purposes of this decision, we are persuaded Petitioner has established a reasonable likelihood it would prevail with respect to at least one of the challenged claims. Accordingly, for the reasons that follow, we institute an *inter partes* review of the ’729 patent as to challenged claims 21 and 22.

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<sup>1</sup> Petitioner identifies ARM, Ltd. and ARM, Inc. as the real parties-in-interest. Pet. 57–58.

<sup>2</sup> In its Mandatory Notices, Patent Owner identifies “IP Bridge” as the real party in interest (Paper 5, 1) and patent owner (Paper 7, 1).

<sup>3</sup> During the conference call, Petitioner requested leave to file a reply to Patent Owner’s Preliminary Response, as well as a certified English translation of JP 8-320423, the Japanese patent application designated as “Foreign Application Priority Data” on the face of the ’729 patent. (Paper 11, 2). We denied both requests. *Id.* at 4.

*B. Related Proceedings*

Patent Owner informs us that the '729 patent is at issue in the following proceeding: *Godo Kaisha IP Bridge 1 v. Broadcom Limited et al.*, Case No. 2-16-cv-00134 (E.D. Tex.), filed February 15, 2016. Paper 5, 2.

*C. The '729 Patent*

The '729 patent is a reissue of U.S. Patent No. 6,237,084 (“the '084 patent”). Ex. 1001, [64]. The '729 patent discloses a positive conversion saturation calculation circuit that operates on a sum-product result of matrix multiplication. *Id.* at 13:23–40. The value of the sum-product result is stored in a sum-product result register. *Id.* at 14:8–10. Figure 4, reproduced below, shows positive conversion saturation calculation circuit 3 that operates on the value stored in sum-product result register 6 and includes constant generator 21, comparator 22, polarity judging unit 23, multiplexer 24, and zero generator 25. *Id.* at 13:46–49.

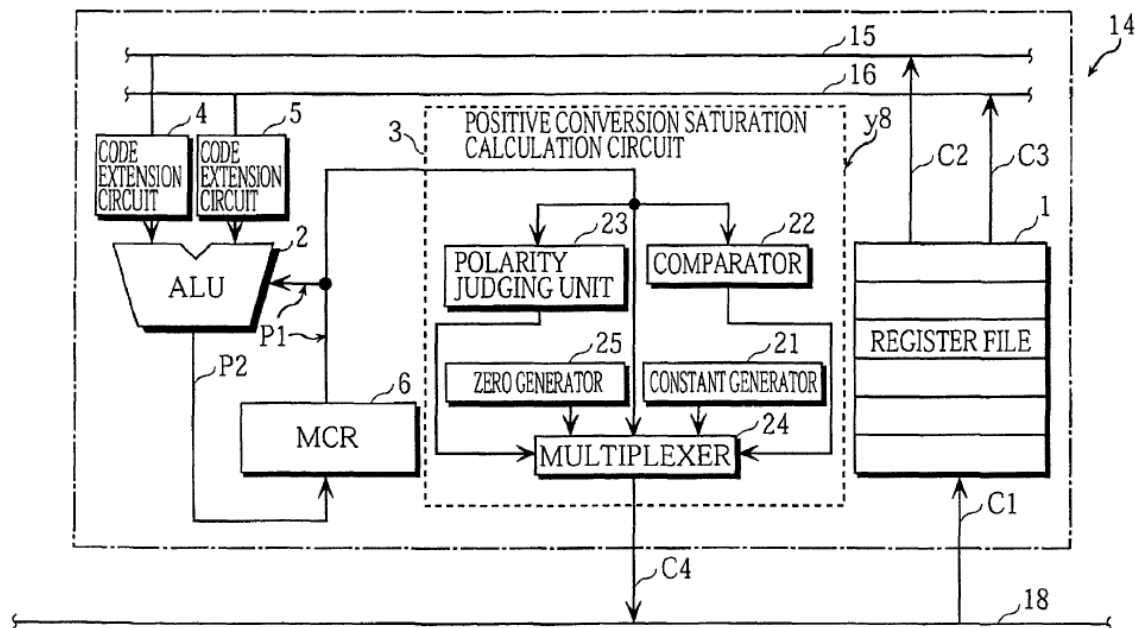


Figure 4 of the '729 patent

When a positive conversion saturation calculation instruction (MCSST) is fetched and decoded, “the constant generator 21 generates a maximum positive value” (e.g., 0x0000\_00FF) that is uncoded and has a width specified by a width field of the instruction, and zero generator 25 generates the integer 0x0000\_0000. *See* Ex. 1001, 13:35–14:7, 15:4–6.

Comparator 22 compares the magnitude of the sum-product value stored by sum-product result register 6 with the maximum positive value output by constant generator 21 and outputs “1” to multiplexer 24 when the sum-product value exceeds the maximum positive value and outputs “0” in all other cases. *Id.* at 14:29–35. Polarity judging unit 23 outputs “1” to multiplexer 24 when it determines the sum-product value is negative and outputs “0” in all other cases. *Id.* at 14:60–15:3.

In accordance with the values shown in Figure 9, reproduced below, based on the inputs received from comparator 22 and polarity judging unit 23 (respectively, logic values x and y in Figure 9), multiplexer 24 selects one of the 0x0000\_0000 value generated by zero generator 25, the maximum positive value 0x0000\_00FF generated by constant generator 21, and the sum-product value stored by sum-product result register 6. Ex. 1001, 15:14–37.

LOGIC VALUE X	LOGIC VALUE Y	SELECTED INPUT VALUE
1	0	0x0000_00FF
1	1	0x0000_0000
0	1	0x0000_0000
0	0	STORED VALUE OF SUM-PRODUCT RESULT REGISTER

Figure 9 of '729 patent

Figure 12B, reproduced below, depicts pipelined execution of a matrix multiplication subroutine including the positive saturation conversion instruction, MCSST.

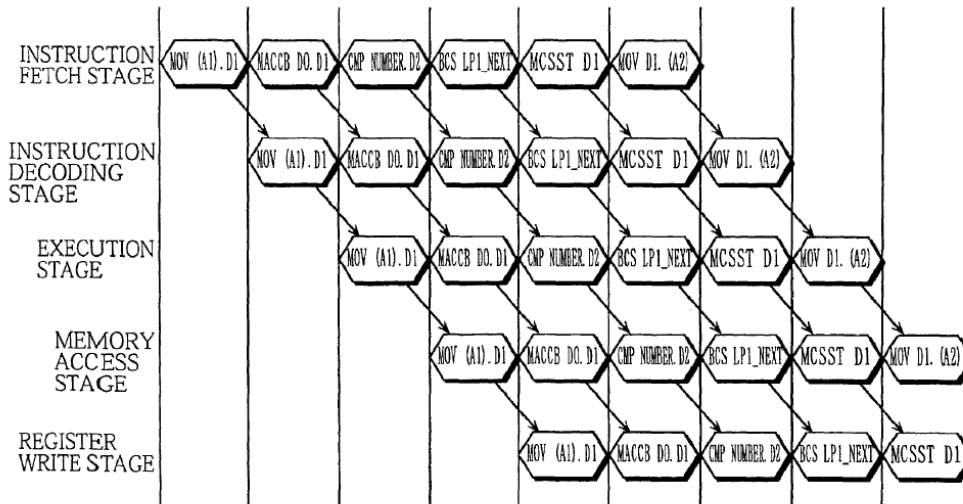


Figure 12B of the '729 patent

Figure 12B was cited by Patent Owner during prosecution of applications in the priority chain<sup>4</sup> leading to the '729 patent. During prosecution of the '920 priority chain application (now “the '145 patent”), the Examiner issued rejections under 35 U.S.C. §§ 112, 251 of claims specifying that the plural arithmetic operations executed by the positive conversion saturation calculation circuit (discussed above) are performed “within one cycle” or “in a single cycle.” Ex. 1013, Response to Non-Final Office Action dated December 8, 2009, 20–21. According to Patent

<sup>4</sup>Application No. 09/399,577 (“the '577 application”), the application underlying the '084 patent, is a divisional application of Application No. 11/016,920 (“the '920 application”), which was filed on Dec. 21, 2004 and is now U.S. Patent No. RE43,145 (“the '145 patent”), which is a divisional application of Application No. 10/366,502 (“the '502 application”), which was filed on Feb. 13, 2003 and is now U.S. Patent No. RE39,121 (“the '121 patent”), which is a divisional application of Application No. 08/980,676 (“the '676 application”), which was filed on Dec. 1, 1997 and is now U.S. Patent No. 5,974,540 (“the '540 patent”).

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