UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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EMC CORPORATION,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

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Case IPR2016-01106
Patent 6,516,442 B1

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Before JUSTIN T. ARBES, BRIAN J. McNAMARA, and MINN CHUNG,
Administrative Patent Judges.

CHUNG, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, EMC Corporation ("Petitioner") challenges the patentability of claims 1, 5, 9, 10, 12, 24, 28, 32, 33, and 34 (the "challenged claims") of U.S. Patent No. 6,516,442 B1 (Ex. 1001, "the '442 patent"), owned by Intellectual Ventures II LLC ("Patent Owner"). The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 5, 9, 10, 12, 24, 28, 32, 33, and 34 of the '442 patent are unpatentable.

II. BACKGROUND

A. *Procedural History*

On May 27, 2016, Petitioner filed a Petition (Paper 3, "Pet.") requesting an *inter partes* review of claims 1, 2, 5, 9, 10, 12, 24, 25, 28, 32, 33, and 34 of the '442 patent. Patent Owner filed a Preliminary Response (Paper 7, "Prelim. Resp."). On November 30, 2016, we instituted an *inter partes* review of claims 1, 5, 9, 10, 12, 24, 28, 32, 33, and 34 of the '442 patent. Paper 9 ("Dec. on Inst."), 50.

After institution, Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp."), to which Petitioner filed a Reply (Paper 18, "Pet. Reply"). In addition, Patent Owner filed a Motion for Observations on certain cross-examination testimony of Douglas W. Clark, Ph.D. (Paper 26, "Obs."), to which Petitioner filed Responses (Paper 28, "Obs. Resp."). An oral

hearing was held on September 7, 2017. A transcript of the hearing is included in the record as Paper 35 ("Tr."). After the hearing, upon our authorization, Patent Owner filed a Patent Owner Sur-Reply (Paper 33, "PO Sur-Reply"), in response to which Petitioner filed a Sur-Sur-Reply (Paper 34, "Pet. Sur-Sur-Reply").

B. Related Proceedings

According to the parties, the '442 patent has been asserted in the following patent infringement cases: *Intellectual Ventures I LLC v. HCC Insurance Holdings, Inc.*, No. 6:15-cv-660 (E.D. Tex.); *Intellectual Ventures II LLC v. Kemper Corp.*, No. 6:16-cv-81 (E.D. Tex.); *Intellectual Ventures I LLC v. Lenovo Group Ltd.*, No. 1:16-cv-10860 (D. Mass.); and *Intellectual Ventures I LLC v. NetApp, Inc.*, No. 1:16-cv-10868 (D. Mass.). Pet. 2–3; Paper 6, 1.

C. The '442 Patent

1. Background

As background, the '442 patent describes that, in conventional symmetric multiprocessor (SMP) systems, a shared system bus is used for memory access by the processors. Ex. 1001, col. 1, ll. 18–21. In such systems, transactions between the processors and the memory take place one at a time over the shared bus. *Id.* at col. 1, ll. 30–32. According to the '442 patent, the serial availability of the shared bus ensures that the transactions are performed in a well-defined order. *Id.* at col. 1, ll. 32–33. Such strong transaction ordering also is necessary to support cache coherency, i.e., coherent state management of the caches associated with each processor. *Id.* at col. 1, ll. 21–24, 33–35.

According to the '442 patent, a shortcoming of the traditional SMP system is that, as more processors are added to the traditional SMP system, the serial or sequential nature of the transactions leads to saturation of the shared system bus, limiting the performance and scalability of the system. *Id.* at col. 1, ll. 36–40. Hence, the '442 patent identifies a need for an SMP system architecture that provides greater scalability and increased transaction throughputs by permitting concurrent use of multiple buses, while still providing a system serialization point to maintain strong transaction ordering and cache coherency. *Id.* at col. 1, ll. 41–46.

2. *Described Invention*

The '442 patent describes a symmetric multiprocessor system that includes a switched fabric, such as a switch matrix, which provides multiple concurrent buses for transferring data between processors and shared memory. *Id.* at col. 1, ll. 49–53, Abstract.

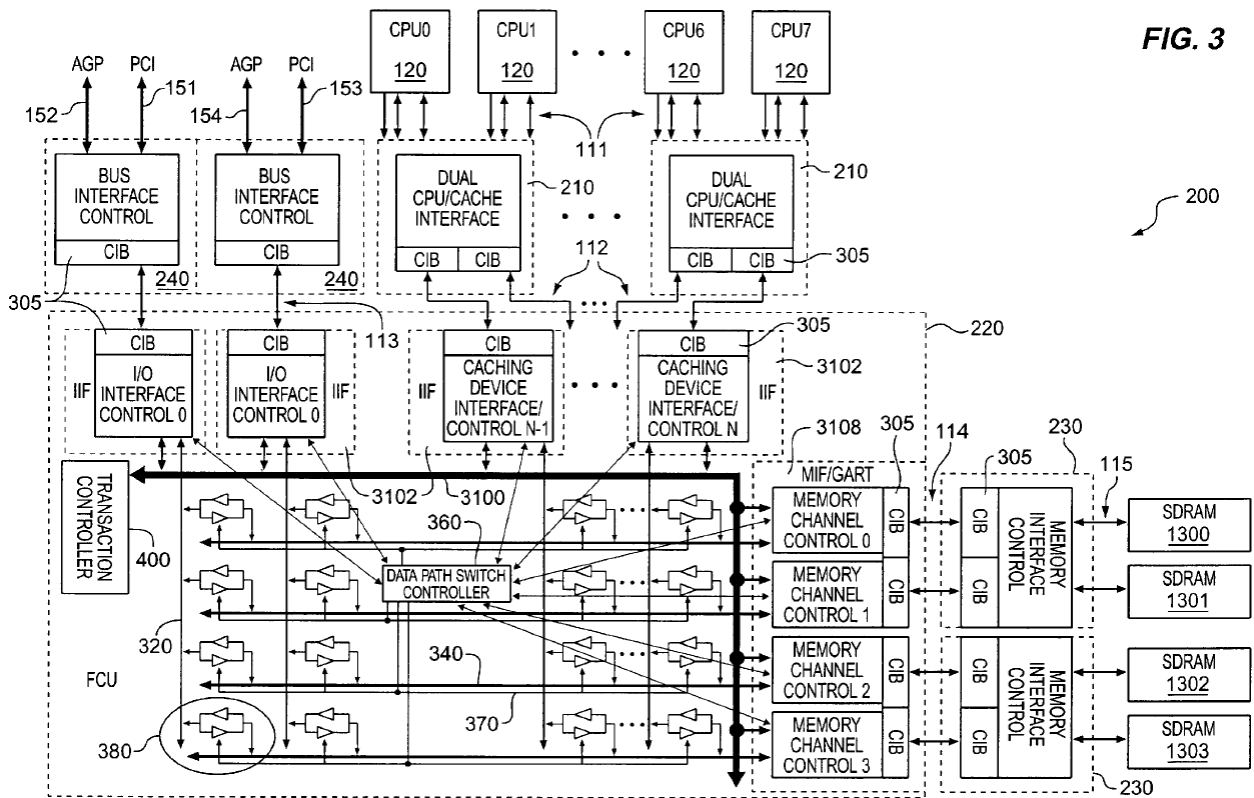Figure 3 of the '442 patent is reproduced below.

FIG. 3

Figure 3 illustrates an embodiment of a symmetric multiprocessor system using a Flow-Control Unit (FCU) based on a switched fabric data path architecture. *Id.* at col. 2, ll. 1–9. Figure 3 describes internal detail of the components of the multiprocessor system depicted in Figure 2 (not reproduced herein). *Id.* As shown in Figure 3, FCU 220 includes a Data Switch, which is also referred to as a Simultaneous Switched Matrix (SSM) or switched fabric data path. *Id.* at col. 3, ll. 6–9. The Data Switch provides for parallel routing of data between multiple initiators and multiple targets (or destinations), such as CPUs and memory devices. *Id.* at col. 4, ll. 30–37.

The multiple, simultaneous data transfers over the Data Switch take place via a series of interfaces between the initiators and the targets. As

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