Filed on behalf of: Unified Patents Inc.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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UNIFIED PATENTS, INC.,
Petitioner
v.

INTELLECTUAL VENTURES II, LLC
Patent Owner

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U.S. Patent No. 6,968,459
IPR2016-01404

COMPUTING ENVIRONMENT HAVING SECURE STORAGE DEVICE
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DECLARATION OF DR. PAUL FRANZON

Contents

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I, Dr. Paul Franzon, declare as follows:

I. INTRODUCTION

I have been retained by Unified Patents Inc. ("Unified" or "Petitioner") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office. Although I am being compensated at my usual rate of $500 per hour for the time I spend on this matter, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

II. QUALIFICATIONS

1. I am a currently a Distinguished Professor in the Department of Electrical and Computer Engineering at North Carolina State University ("NCSU") in Raleigh, North Carolina. I have been affiliated with NCSU in various roles since 1989.

2. I obtained my Ph.D. in Electrical and Electronic Engineering in 1989 from the University of Adelaide in Australia. I obtained two additional degrees from the University of Adelaide, a Bachelor of Engineering in Electrical and Electronic Engineering (1984) and a Bachelor of Science in Physics and Mathematics (1983).

3. I have over 20 years of experience with memory hierarchies and security in electronic hardware. My experience in these areas started in the early-mid 1990s.

4.   From 1989 to 1996, I taught a graduate level course on Computer Design that included sections on memory hierarchies, including caching and disk storage.

5.   As part of a DARPA funded project that ran from 1993 to 1997, I led a group in building an encryption processor that implemented the Data Encryption Standard (DES). This was built as 3-chip module, on what would today be called an interposer.

6.   From 2007 to 2009, I collaborated with Irvine Sensors on a DARPA funded project in which we used a cryptographic technique, a one way hash function, to obfuscate the design of digital systems.

7.   Since 2011, I have been the lead author and editor of the chapter on Emerging Research Architectures for the International Roadmap for Semiconductors (ITRS). One subsection of this has been on "Storage Class Memories" (SCM), with a partial focus on solid state mass storage. I have helped run ITRS workshops on this topic, and co-wrote a book chapter on SCMs.

8.   Since 2015, I have been the Principal Investigator of a project funded by the Air Force Research Laboratories on interfacing a secure processor to a 3D memory chip stack.

9.   Since 2015, I have been leading a DARPA funded project in 3D methods to obfuscate the design of secure chips.

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