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Paper 10
Entered: February 22, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
(d/b/a ON SEMICONDUCTOR),
Petitioner,

v.

POWER INTEGRATIONS, INC.,
Patent Owner.

Case IPR2016-01599
Patent 6,107,851

Before THOMAS L. GIANNETTI, BRIAN J. McNAMARA, and LYNNE E. PETTIGREW, *Administrative Patent Judges*.

PETTIGREW, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, Semiconductor Components Industries, LLC, d/b/a ON Semiconductor, filed a Petition for *inter partes* review of claims 2, 3, 7, 8,

10, and 19 of U.S. Patent No. 6,107,851 (Ex. 1001, "the '851 patent").[1] Paper 1 ("Pet."). Patent Owner, Power Integrations, Inc., filed a Preliminary Response. Paper 9 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any of the challenged claims of the '851 patent.

A. Related Matters

Petitioner identifies as related matters the following two district court proceedings: *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, No. 1:04-cv-01371 (D. Del.), and *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, No. 1:08-cv-00309 (D. Del.). Pet. 2. The United States Court of Appeals for the Federal Circuit reviewed district court decisions in those two cases in *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348 (Fed. Cir. 2013), and *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 843 F.3d 1315 (Fed. Cir. 2016). *See* Pet. 2.

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[1] Of the claims challenged in the Petition, claims 2, 7, 10, and 19 were introduced or amended during reexamination of the '851 patent (*see* Reexamination Application No. 90/008,324) and appear in Ex Parte Reexamination Certificate US 6,107,851 C1. Ex. 1002. Thus, all references to those claims of the '851 patent are to the claims as issued in the Reexamination Certificate.

Petitioner also identifies as a related matter the reexamination of the '851 patent. *Id.* In addition, Petitioner concurrently filed a petition (IPR2016-01598) for *inter partes* review of claims 12, 16, 18, and 20 of the '851 patent. *Id.* at 2–3.

B. The '851 Patent

The '851 patent relates to switch mode power supplies, which convert, for example, an AC voltage at a wall socket to a DC voltage used to power an electronic device. Ex. 1001, 1:5–21. A switch mode power supply may incorporate a pulse width modulated (PWM) switch to maintain a steady DC voltage. *Id.* The PWM switch uses an oscillator and related circuitry to vary the frequency of the switch. *Id.*

According to the '851 patent, a common problem with switch mode power supplies is the electromagnetic interference (EMI) generated at the switching frequency of the switch. *Id.* at 1:22–40. The '851 patent explains that, at the time of the invention, it was known that EMI could be reduced by varying, or jittering, the frequency of the oscillator contained in the PWM switch controller. *Id.* at 3:9–30. Jittering allows the switching frequency of the switch to be spread over a larger bandwidth, which minimizes the peak value of the EMI generated by the power supply at each frequency. *Id.* at 3:22–25.

Figure 1 of the '851 patent illustrates a known power supply using a PWM switch and frequency jitter circuitry external to the PWM switch for varying the switch frequency. *Id.* at 3:12–17, 4:37–39, Fig. 1 (labeled "PRIOR ART"). The '851 patent describes shortcomings of the EMI reduction scheme shown in Figure 1. For example, the amount of frequency

jitter itself will vary due to variations in the line voltage and output load. *Id.* at 3:31–34, 6:13–17.

The '851 patent purports to overcome shortcomings of external frequency jitter circuitry by including a frequency variation circuit that is internal to the PWM switch itself. According to the '851 patent, an internal frequency variation signal has an advantage over the frequency jitter operation of Figure 1 "in that the frequency range of the presently preferred pulse width modulated switch is known and fixed, and is not subject to the line voltage or load magnitude variations." *Id.* at 6:13–17 (reference numeral omitted). Moreover, the '851 patent continues, a power supply containing a PWM switch with an internally generated frequency variation signal will have a reduced size and overall cost as compared to the prior art power supply shown in Figure 1 with an externally generated frequency variation signal. *Id.* at 6:21–24.

C. Challenged Claims

Of the challenged claims, only claim 19 is independent. Claim 19 was added as a new claim during reexamination of the '851 patent to replace independent claim 1, which was cancelled. Ex. 1002, 1:19, 2:1–22; Ex. 1016, 2, 6, 8 (Second Amendment and Response After Final, May 9, 2009). Challenged claims 2, 7, and 10 were amended during reexamination to depend from claim 19. Ex. 1002, 1:29–42. Claims 3 and 8 were not reexamined and continue to depend from cancelled claim 1. Ex. 1001, 12:40–45, 12:66–13:4.

Claim 19 is illustrative of the claimed subject matter and reads:

> 19. A pulse width modulated switch comprising:
>
> a first terminal;
>
> a second terminal;
>
> a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;
>
> a frequency variation circuit that provides a frequency variation signal, wherein the frequency variation signal is an internally controlled signal within the pulse width modulated switch;
>
> an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and
>
> a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and a magnitude of said oscillation signal is below a variable threshold level.

Ex. 1002, 2:1–22.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 2, 3, 7, 8, 10, and 19 of the ’851 patent are unpatentable based on the following grounds:

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