Trials@uspto.gov
571.272.7822

Paper 6
Filed: April 11, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-00038
Patent 6,195,302 B1

Before JAMESON LEE, KEVIN F. TURNER, and JOHN A. HUDALLA, *Administrative Patent Judges.*

TURNER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Petitioner, Samsung Electronics Co., Ltd. ("Petitioner"), filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–6 and 10–12 of U.S. Patent No. 6,195,302 B1 (Ex. 1001, "the '302 Patent"). Patent Owner, ProMOS Technologies, Inc. ("Patent Owner"), did not file a Preliminary Response.

To institute an *inter partes* review, we must determine that the information presented in the Petition shows "that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Having considered the Petition, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing the unpatentability of each of claims 1–6 and 10–12 of the '302 Patent.

B. Related Matters

Petitioner and Patent Owner indicate that the '302 Patent has been asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 1:15-cv-898-SLR-SRF (D. Del.). Pet. 1; Paper 5, 1. The '302 Patent is also the subject of another petition, also filed by Petitioner, seeking *inter partes* review of claims 1–6 and 10–18 under different grounds of unpatentability, IPR2017-00039, being considered concurrently.

Petitioner and Patent Owner indicate that these patents are related to the '302 patent: U.S. Patent Nos. 5,761,112; 6,849,897; 6,020,259; 6,088,270; and 6,699,789. *Id.* Patent Owner identifies these *inter partes* review proceedings for the related patents: IPR2017-00032 (Patent No.

6,849,897); IPR2017-00033 and IPR2017-00035 (Patent No. 6,020,259); IPR2017-00036 (Patent No. 6,088,270); IPR2017-00037 (Patent No. 6,699,789); and IPR2017-00040 (Patent No. 5,761,112). Paper 5, 1.

C. The ’302 Patent

The ’302 patent is directed to a random access memory and the operations within a random access memory for reading or refreshing memory cells, specifically applied to sense amplifiers. Ex. 1001, 1:8–10. The ’302 Patent discloses a memory device with sense amplifiers, as illustrated in Figure 1, reproduced below:

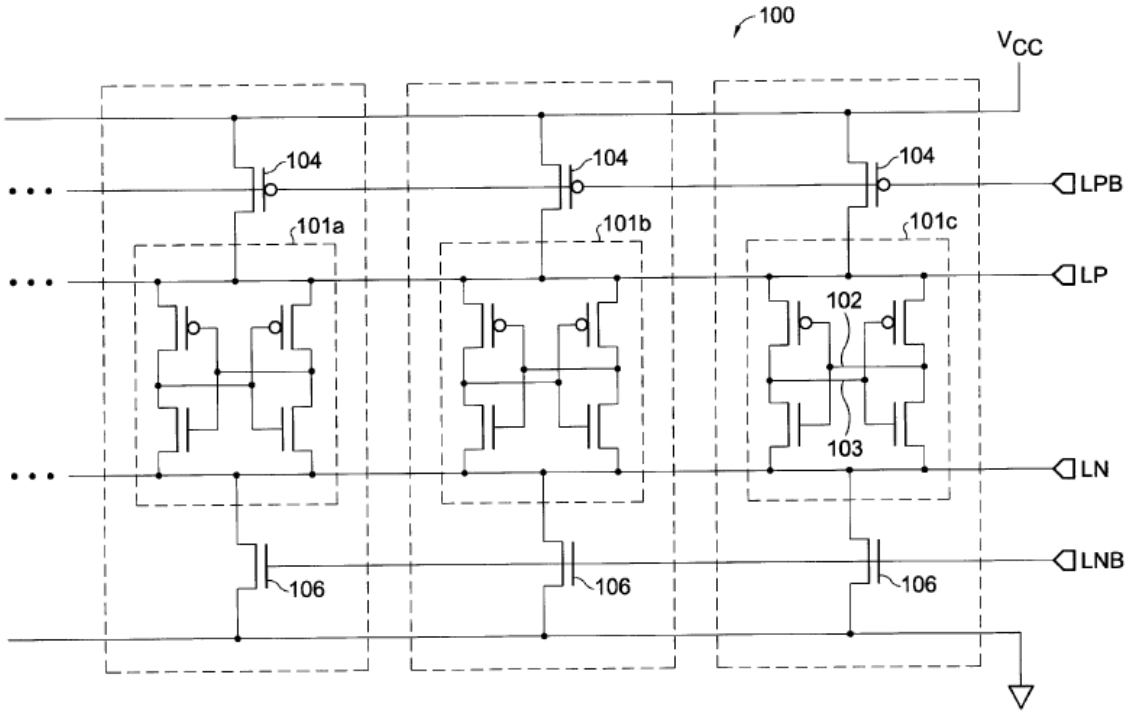

FIG. 1

Figure 1 illustrates a memory device according to an embodiment of the ’302 Patent.

Sense amplifiers 101a–101c are coupled to high voltage line Vcc and ground via driver transistors 104 and 106, respectively. *Id.* at 4:40–5:4.

Driver transistors 104, which are PMOS pull-up transistors, and driver transistors 106, which are NMOS pull-down transistors, are controlled by control signals LPB and LNB, respectively. *Id.* The '302 Patent illustrates the functionalities of the sense amplifiers with respect to Figure 2, reproduced below:

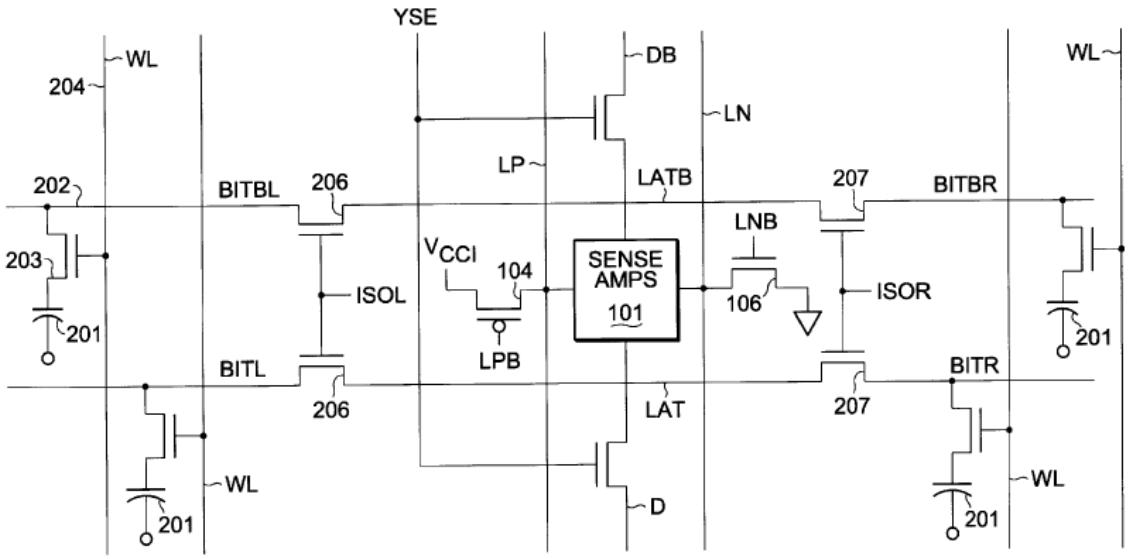

FIG. 2

Figure 2 illustrates a portion of a memory device according to an embodiment of the '302 Patent.

The '302 Patent discloses that storage capacitors 201 are selectively coupled to bit lines 202 through access switches 203 in response to address signals supplied to word lines 204. *Id.* at 5:5–9. Prior to a read operation, a pair of bit lines 202 are "equalized at some voltage between a logic high and a logic low signal," and a word line (WL) signal is activated. *Id.* at 5:18–21, 5:35–37. After the WL signal is activated, "the LPB signal is driven to a logic low[,] coupling VCCI to sense amp 101 through drive transistor 104

[and] [s]imilarly, the LNB signal is driven high to couple sense amp 101 to ground or V_{SS} through drive transistor 106." *Id.* at 5:38–42. The '302 Patent also provides that "LNB and LPB are generated by a circuit such as that shown in FIG. 3 that generates LNB and LBP both as dual slope signals." *Id.* at 5:45–47. Figure 3 of the '302 Patent is reproduced below:

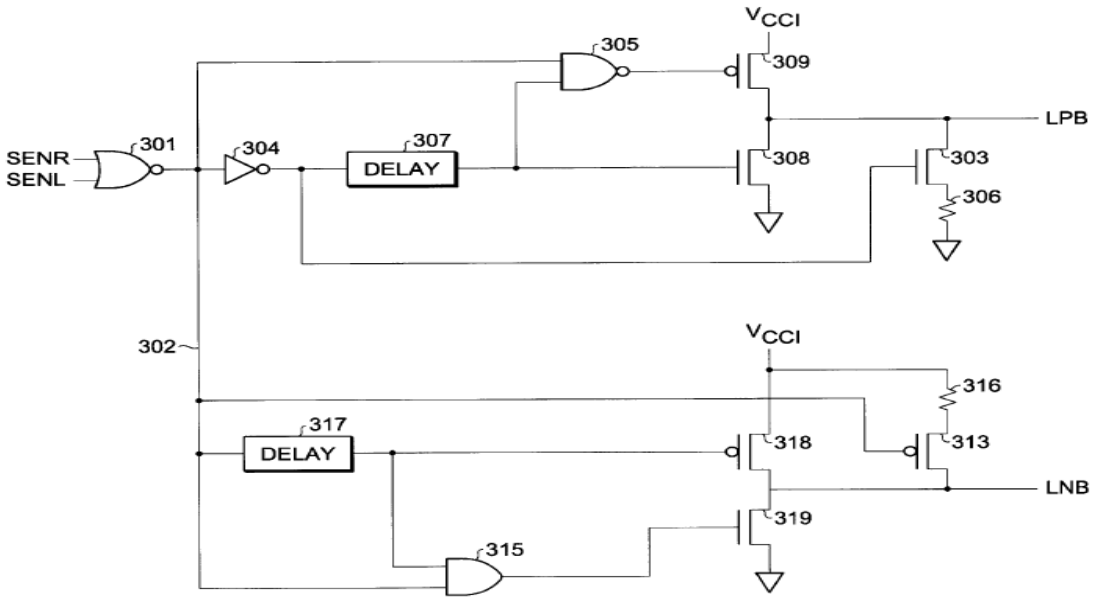

FIG. 3

Figure 3 illustrates a timer circuit according to an embodiment of the '302 Patent.

The '302 Patent discloses that when sensing is to begin, "one of the input signals SENR or SENL will go to a logic high," which causes signal 302 to transition to a logic low because of NOR gate 301 and inverter 304. *Id.* at 5:66–6:6. Signal LPB is disclosed as being generated as follows:

> [S]hortly after either SENR or SENL goes high, transistor 303 is turned on pulling the LPB signal low through resist[o]r 306. . . . Resistor 316 controls the rate of change or dv/dt of LNB while resistor 306 controls the dv/dt of LPB. After a delay determined by delay element 307, transistor 308 will be turned on pulling

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