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United States Patent [19]

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Seo

[45] Date of Patent: **Aug. 18, 1992**

[54] **SENSE AMPLIFIER DRIVER FOR MEMORY DEVICE HAVING REDUCED POWER DISSIPATION**

0178796 8/1986 Japan 365/205
0226111 9/1988 Japan 307/603
0275223 11/1988 Japan 307/481

[75] Inventor: **Seung-mo Seo, Seoul, Rep. of Korea**

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[73] Assignee: **Samsung Electronics Co., Ltd., Rep. of Korea**

IBM Tech. Disc. Bult.; Chakravarti et al.; High Gain Sense Amplifier; Dec. 1977; p. 206.
Wong et al.; Memory Techniques—A 45ns Fully Static 16K MOS ROM; Feb. 19, 1981; p. 150.

[21] Appl. No.: **358,679**

[22] Filed: **May 30, 1989**

Primary Examiner—Stanley D. Miller
Assistant Examiner—Terry D. Cunningham
Attorney, Agent, or Firm—Morgan & Finnegan

[30] **Foreign Application Priority Data**

Jul. 11, 1988 [KR] Rep. of Korea 88-8607

[51] Int. Cl.⁵ **G11C 7/00**

[52] U.S. Cl. **307/530; 307/263; 307/592; 307/601; 365/205; 365/233**

[58] Field of Search 307/263, 530, 592, 601, 307/603, 481; 365/194, 205, 233

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[57] ABSTRACT

An improved sense amplifier driver for sensing and restoring data in memory cells is disclosed. Pull-up means in the form of p-channel MOS transistors are respectively provided for forcibly pulling up the gate voltage of delayable p-channel MOS transistors within the first inverter of the sensing clock driver and the second inverter of the restore clock driver in the trailing transient periods of the sensing and restoring clock signals. The formation of a DC current path between the power line and the ground line in any one of the delayable p-channel MOS transistors is prevented, thereby making it possible to avoid the unnecessary power dissipation. Further, delaying resistances are installed respectively in the first inverter of the sensing clock driver and in the second inverter of the restoring clock driver to make the slope of the leading edges of the sensing and restoring clocks less steep, thereby making it possible to exclude the occurrence of noise.

3 Claims, 5 Drawing Sheets

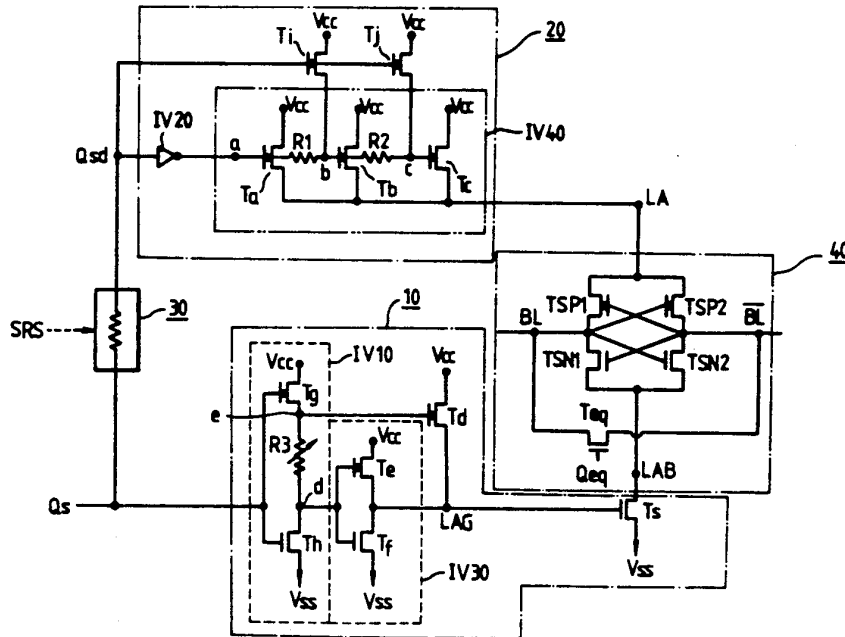


FIG. 1 (Prior Art)

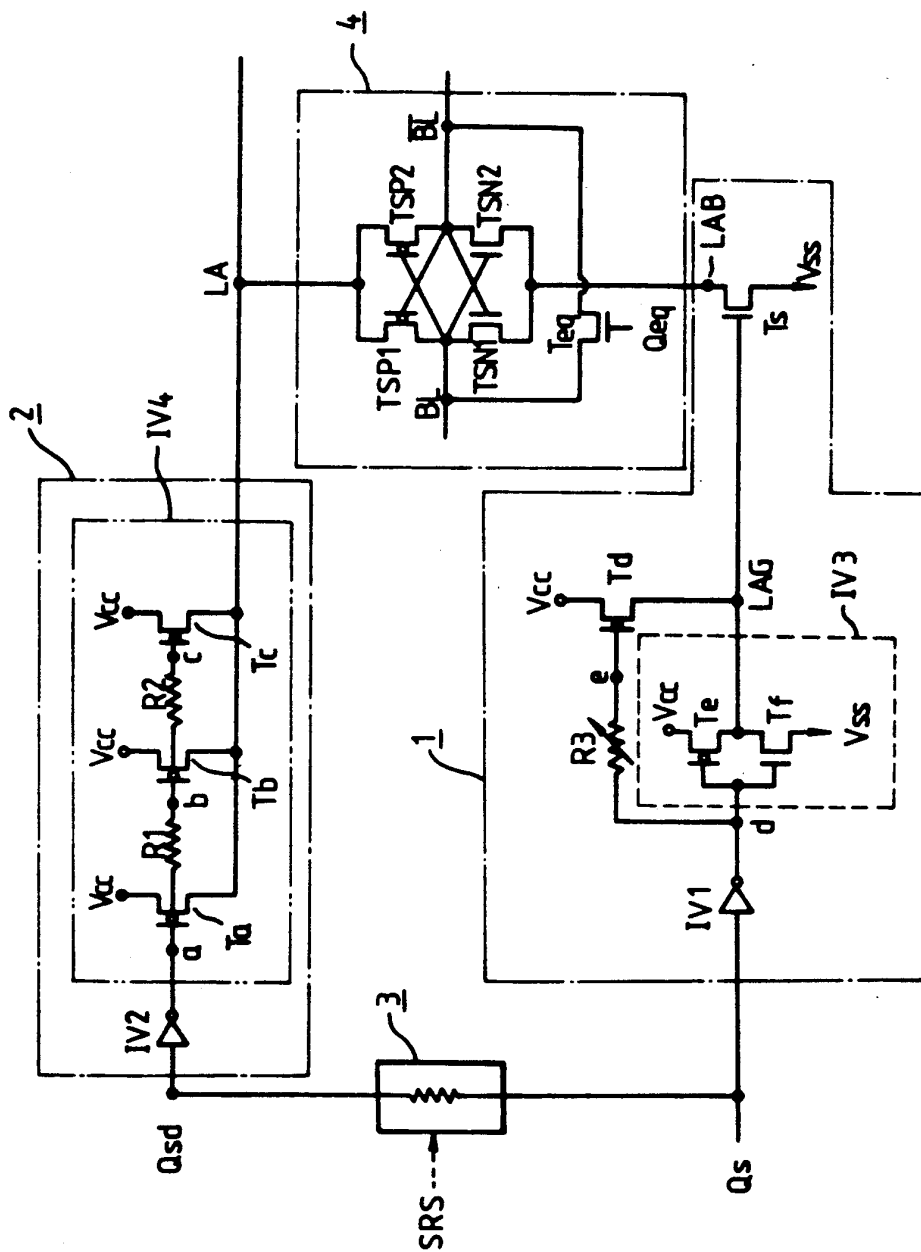


FIG. 2 (Prior Art)

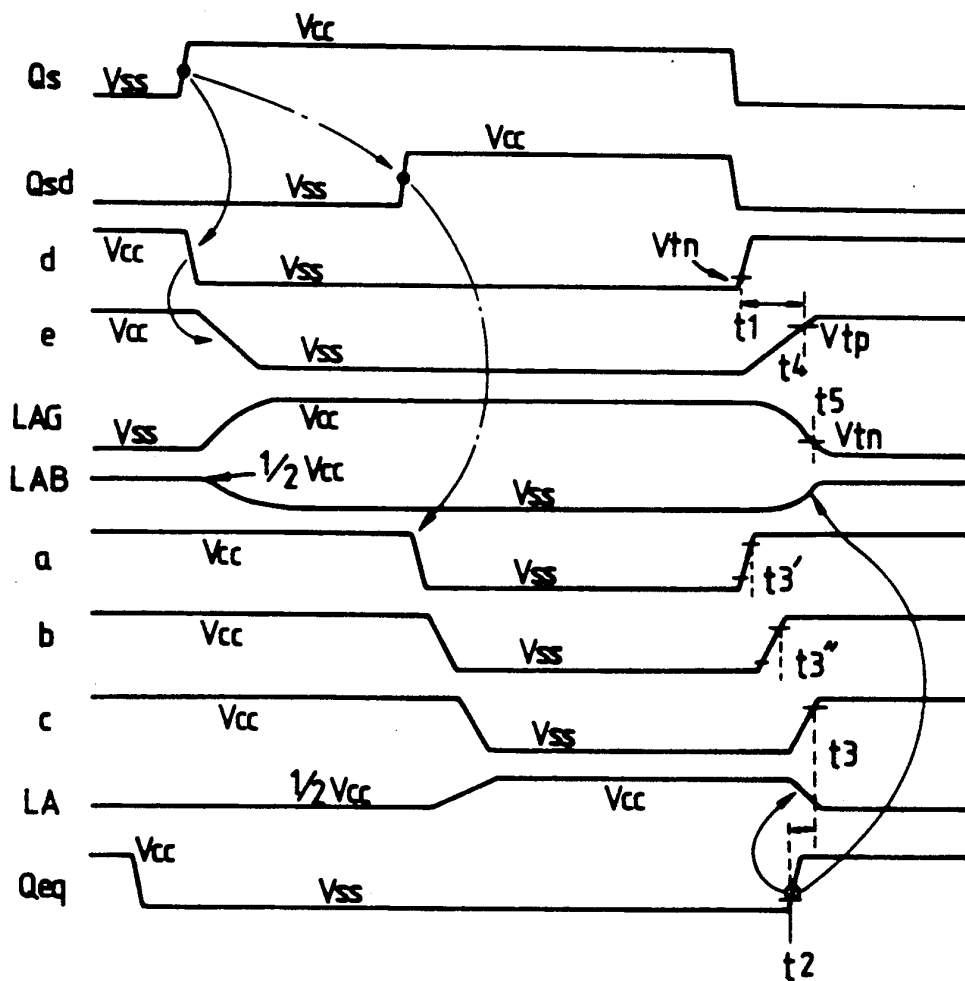


FIG. 3 (Prior Art)

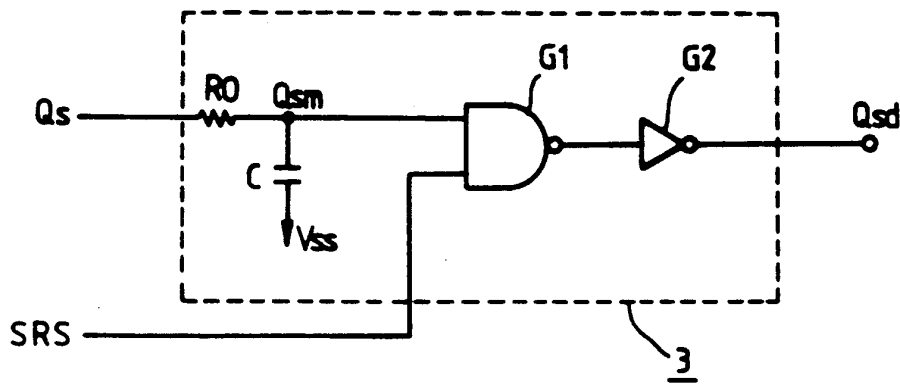
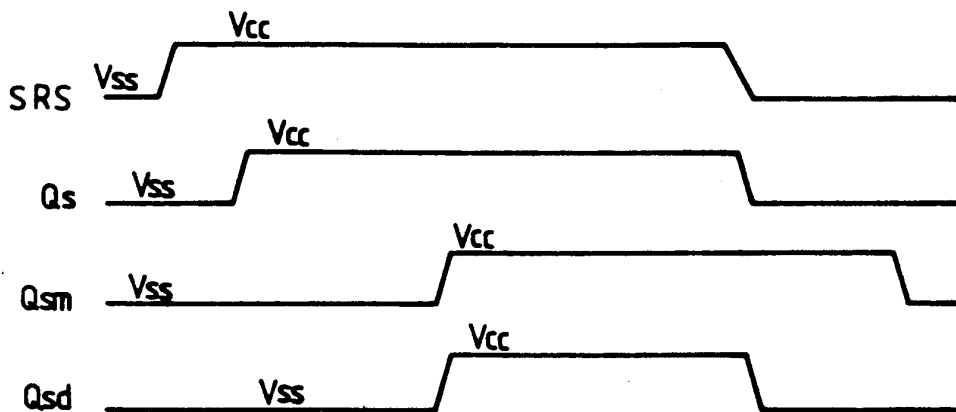
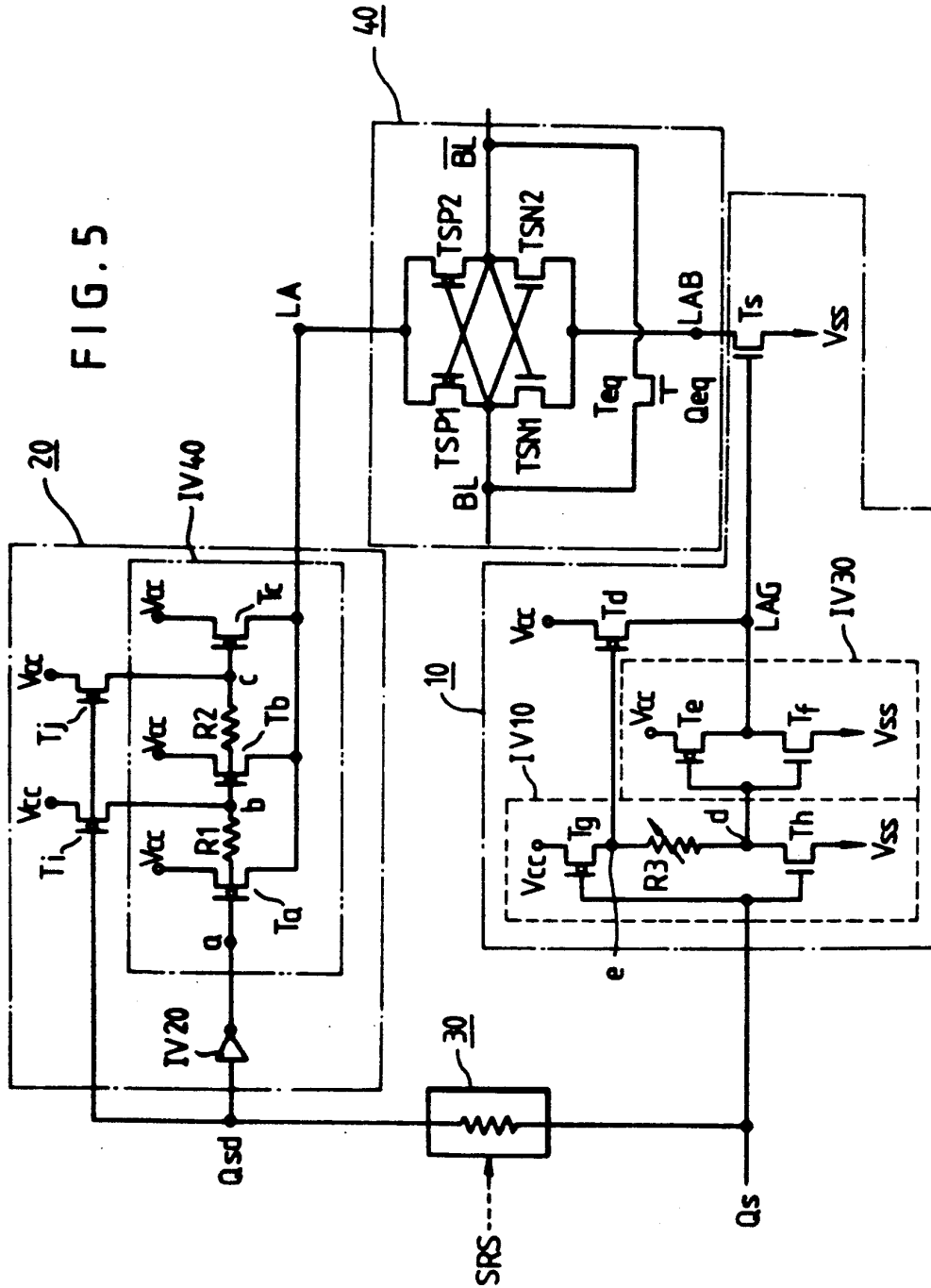


FIG. 4 (Prior Art)





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