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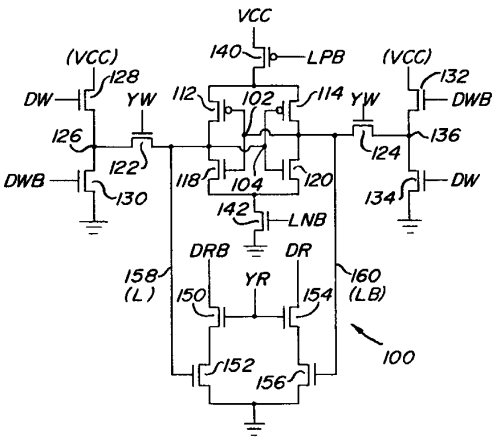
(54) **Sense amplifier with local write drivers.**

(57) A sense amplifier for a very high density integrated circuit memory using CMOS technology is described. Each sense amplifier includes first and second local sense amplifier drive transistors, one (140) connecting the P channel transistors (112, 114) to VCC; the other (142) connecting the N channel transistors (142) to VSS. A read amplifier circuit (150-156) is provided within each sense amplifier and is operated by read control signals (DR, DRB, YR). Internal nodes of the latch of the sense amplifier are coupled by pass transistors (122, 124) that are responsive to column write control signals (YW). Local data write driver transistors (128, 130, 132, 134) are also provided to selectively couple the pass transistors to VCC-Vt or VSS in response to further data write control signals (DW, DWB). A relatively wider power line (184) is coupled to the drive transistors (140) to provide VCC thereto, and a narrower line (181) is used to control those first sense amplifier drive transistors (140). Corresponding wide and narrow lines (190, 186) are used for the second local sense amplifier drive transistors which couple the N channel transistors to ground. Each sense amplifier may be shared between first and second pairs of bit lines (220, 222; 224, 226) through the use of isolation transistors 232, 234, 238, 240) and a corresponding isolation signal (ISOL, ISOR).

FIG. 5



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The present invention relates to integrated circuit memories and particularly relates to sense amplifiers for use therein.

Integrated circuit memories include a large number of memory cells which are usually set forth in an array. The memory cells may be volatile or non-volatile. If they are volatile, they may be static RAM cells or dynamic RAM cells. There may be one large array, or a given memory chip may have several sub-arrays which may be arranged in blocks. Typically, the memory device comprises a large number of bit lines extending in one direction. The bit lines may be paired or non paired. Where they are paired, they are often referred to as complementary bit lines, or paired bit lines. Complementary bit lines are used for both static RAM and dynamic RAM applications. The bit lines generally extend in a first direction, and a plurality of word lines extend in a second direction which is perpendicular to the first direction. Typically, a memory cell is located at or near the crossing of a bit line with a word line.

Often, a memory array is divided into subarrays, and each subarray may further be divided into blocks. Each subarray will often have its own "peripheral circuitry" such as decoders.

The memory array or subarray is usually said to be organized into rows and columns. Generally, a row indicates the memory cells located along (coupled to) a word line. A column is therefore ordinarily perpendicular to a row and generally indicates a collection of memory cells along (coupled to) a bit line or a bit line pair. Generally, each column is connected to a respective sense amplifier. One job of the sense amplifier is to sense the effect that the memory cell has on the bit line(s) and to amplify that signal for outputting in a read operation. Conversely, the sense amplifier may also drive or control the bit line(s) when the memory is writing data into a memory cell.

CMOS technology is prevalent today. Figure 1 illustrates a prior art configuration and shows a sense amplifier 10 using CMOS technology. The operation and configuration of such a sense amplifier 10 is well known and will not be explained except briefly herein. Amplifier 10 contains P channel transistors 12 and 14 having source electrodes commonly coupled to a line 16 which carries from time to time a signal LP also called LATCHP. The sense amplifier also comprises a pair of N channel transistors 18, 20 having source electrodes commonly coupled to a line 22 which sometimes carries a signal which may be called LN or LATCHN. A pair of internal nodes A, B are connected to gate electrodes. In particular, node A is coupled to the gate electrodes of transistors 12 and 18, while node B is coupled to the gate electrodes of transistors 14 and 20. These transistors form a latch. A first bit line BL1 on the left side of sense amplifier 10 is coupled to node B which is also coupled between the drain electrode of P channel transistor 12 and the drain electrode of N channel transistor 18. Likewise, a complementary bit line BL1 BAR is connected to node A which is also coupled between the drain electrode of P channel transistor 14 and N channel transistor 20. Transistors 12 and 14 are referred to as "pull-up" transistors whereas transistors 18 and 20 are referred to as "pull-down" transistors. When a transistor 24 is turned on, it couples VCC through its source-drain path to line 16, thereby providing the LATCHP signal. Sense amplifier 10 forms a flip-flop so that either transistor 12 or 14 but not both will be turned on and will pull the voltage at its corresponding node toward VCC. At or near the same time, one of the transistors 18 or 20 will pull down the voltage at the other node toward VSS which will be connected to line 22 via a transistor 26 being turned on. In this way, one of the two nodes is pulled high and the other is pulled low, and the sense amplifier latches into a stable state.

In any large memory, such as a 16 megabit DRAM, there will be thousands of columns and thousands of rows. This is represented in Figure 1 which shows a second sense amplifier 30 connected to corresponding bit line pair BL2 and BL2 BAR, and an N-th sense amplifier 32 coupled to bit lines BLN and BLN BAR. It should be appreciated that N may be on the order of 1000 or more. The LATCHP signal is applied to all N of these sense amplifiers via line 16, and the LATCHN signal is applied to them via the line 22. It will be seen in Figure 1 that a plurality of resistances 34 are illustrated. These are not discrete resistance devices but rather indicate the parasitic resistance of the lines 16 and 22, which, even though they are formed of conductive materials such as metal or the like, nevertheless over great distances will have some resistance value. Over each resistance, there will be a voltage drop from the voltage applied via transistor 24 or 26, as the case may be. Accordingly, the voltage that eventually reaches sense amplifier 32 may be appreciably diminished from VCC or VSS, and that sense amplifier will work inefficiently or slowly. It will also be appreciated that because of this problem, sense amplifier 10 does not activate at the same time as sense amplifier 32 and the resulting skew prolongs access time. Additionally, some prior art designs can be unstable if the selected sense amplifier is connected to the data line (the bit lines) too early.

Thus, as power supply (VSS) line 22 is trying to pull down to 0v, transistors start to turn on in the sense amplifiers. A current flows to the right on line 22, and there exists a voltage drop due to the resistance of line 22. Practical limitations prevent

the solution of greatly widening line 22 to reduce its resistance -- the chip area is jealously allocated. Hence, in the illustrated architecture, the right-most sense amplifier 10 turns on first, and sense amplifier 32 will turn on thereafter.

Generally, one desires to pull down line 22 at a controlled rate. The far end (most remote from transistor 26) of line 22 will drop in voltage slower than the near end. This slows the memory, which is undesirable, but if circuitry drove the near end too fast, then the corresponding near sense amplifiers would become unreliable.

Another problem occurs when the near sense amplifiers latch logic "1's" and the far amplifier latches a logic "0." There is a pattern sensitivity because when the bit lines are precharged to ½VCC, the memory cell moves only one of the bit lines lower or higher.

Sensing a "1" occurs before sensing a "0" because LN needs to drop only 1 Vt below a voltage level corresponding to a "1." However, to sense a "0" LN must be 1Vt below the "0" level, and this occurs later. Large current flows when "1's" are read. Because of the large currents, the decline in voltage at the far end of line 22 slows to an uncontrolled rate. This effectively can add 7 nsec. to the sensing process -- a substantial and undesirable increase.

One approach that has been proposed for addressing this problem is depicted in Figure 2. It shows the same sense amplifiers 10,30, and 32, and has the same signals LATCHP and LATCHN provided by transistors 24 and 26 respectively. However, further N channel transistors have been added beneath the sense amplifiers and a modification has been made so that LATCHN is carried by two distinct lines. One of these lines 40 is constructed relatively wide to carry most of the current, and the other line 42 is relatively narrower because it will carry current for just a single selected sense amplifier. Line 40 is coupled to the sources of a plurality of transistors 44, each sense amplifier having a respective transistor 44. Each transistor 44 has its gate electrode coupled to VCC and is therefore generally on. Transistors 44 are relatively small in size so that they do not carry much current to any single sense amplifier.

The narrower line or rail 42 is coupled to the several sense amplifiers by source-drain paths of respective transistors 46, which are shown also as N channel transistors. Transistors 46 are decoded and this is indicated by a low to high transition signal YR 47 shown beside the gate electrode of transistor 46 for sense amplifier 32 at the far left side of Figure 2. The other transistors 46 also are coupled to their YR signals, which are shown illustratively at 0v, i.e. they are not selected columns. Thus, the column which has been selected decodes its YR signal to apply to the gate electrode of the transistor 46 thereby to couple the narrow LATCHN line 42 to the sense amplifier. See also Okamura et al., "Decoded-Source Sense Amplifier for High-Density DRAMs", IEEE J. Solid State Circuits, Vol. 25, No. 1 (Feb 1990), pp 18-23. This solution does reduce the sensing skew since the current flowing through line 40 is reduced due to the weak transistors 44 in the current path. Therefore, the voltage drop down line 40 is reduced. Disadvantages of this approach are that the large transistors 46 must be added and that the capacitive loading on the column select signal YR is increased since it must drive the gates of transistors 46. There is poor control over the current draw and extra loading to the YR line because it is driving an extra transistor per sense amplifier.

Chin et al., "An Experimental 16-Mbit DRAM with Reduced Peak-Current Noise," IEEE J. Solid State Circuits, vol. 24, no. 5 (Oct. 1989) at p. 1191 et seq. and particularly in Figure 4 adds both p-channel and n-channel transistors between sense amplifiers and power supply lines. However, it does not use one connection to the VCC line and one connection to the VSS line *per sense amplifier*. It does not drive these power lines from one end only, but rather from several connections that are distributed in the array. Signals SAP and SAN bar may correspond to LP and LN respectively. Thus, in the architecture disclosed that article, there are several sense amplifiers connected together, and there will still be some pattern sensitivity.

Figure 3 illustrates further transistors that have been used in the past or are used in current generations (16 Meg) of very large capacity integrated circuit memories. Thus, sense amplifier 10 is coupled between LATCHP and LATCHN signals which are generally VCC and VSS. The data signals coming from the data lines are illustrated as D and its complement D BAR. However, the source-drain paths of further pass transistors 48 and 50 couple the data signal D to the sense amplifier, and an identical arrangement is provided for the complementary data signal. Transistor 48 is responsively coupled to a global column select signal Y which is applied to the gate electrode thereof. Most 16 meg DRAMs have such global Y select signals. Additionally, very large scale memories, as mentioned above, include one or more blocks, and transistors 50 are illustrated to show a block enable signal controlling the operation of transistor 50. In this, the complementary data signals must be high, near VCC, during reading and the pass transistors must be small compared to the LATCH transistors to avoid instability.

Figure 4 shows some of the problems of circuitry styled along the lines of Figure 3. In Figure 4, three identically constructed sense amplifiers 10

are illustrated, and for ease of reference they will be referred to in this drawing as 10A, 10B and 10C. For ease of illustration, the LATCHP line 16 and LATCHN line 22 are not shown. The column select signal Y is a global select signal and is therefore shown as having a voltage of VCC. The block enable signals are separately provided so that the pass transistors 50 for sense amplifier 10A have their gate electrodes coupled to a line 52A which carries a first block select signal. Similarly, pass transistors 50 for sense amplifier 10B have their gate electrodes coupled to a second block select line 52B which carries a second block select signal, and a block select signal line 52C similarly corresponds to sense amplifier 10C.

Sense amplifier 10A is illustratively in an inactive block, for sake of explanation. "Inactive" means herein that LN and LP are at ½VCC and the latch is inactive. Its block has not been enabled so the block enable signal on line 52A is low at zero volts. Thus, pass transistors 50A are off, and regardless of whether transistors 48A may be on, sense amplifier 10A is generally isolated from data. However, to prevent it from latching, LATCHP and LATCHN must both be kept at ½VCC, and the data write signal DW and its complement DWB are held at VCC.

Sense amplifier 10B is in an active block with LN at 0v and LP at VCC. However, with the block select at 0v, no write will occur even with the global column select Yw at VCC.

Since amplifier 10C is in an active block and a write operation is to occur through amplifier 10C. The block select signal on line 52C is high, at VCC. The column select signal Y is high. With the data signal DW high at VCC and its complement DWB low at zero volts (or vice-versa if different data is being written), the pass transistors 48C, 50C on at least one side of sense amplifier 10C will turn on, and the sense amplifier will latch the data state and drive the bit lines so that the data state will be written into the memory cell or cells along the column (usually at the active word line).

An object of the present invention is to improve the sense amplifiers to overcome or reduce the aforementioned problems.

The present invention provides a CMOS sense amplifier with local write driver transistors to eliminate the pattern sensitivities and delays of the prior art. Also, each sense amplifier has its own respective drive transistors. Third, each sense amplifier includes a column read amplifier which eliminates the instability problem because the latch nodes are never connected to the data lines. Further, the local write drivers solve the problems associated with global columns selects. Prefer embodiments of the present invention will use column read YR and column write YW signals.

In one of its aspects, while the prior art used narrow and wide lines or rails each carrying a LATCHN signal, the present invention uses narrow and wide lines in connection with the LATCHN signal but connects them differently. Additionally, the present invention in one of its aspects includes narrow and wide lines or rails for the LATCHP supply signal. Thus, in the preferred embodiment, each sense amplifier has a respective N channel transistor having its source-drain path coupled to VSS or a signal LATCHN via the wide line. The gate electrodes of those N channel drive transistors are gated by the narrow drive line which preferably carries the complement LNB of the LATCHN signal.

Correspondingly, in another aspect of the invention, each sense amplifier includes a respective P channel drive transistor, the source-drain path of which couples the P channel transistors of the sense amplifier latch to the high voltage such as VCC or LATCHP. That high voltage is carried by one of the wide drive lines. The narrower of the drive lines associated with LATCHP is coupled to the gate electrodes of these P channel drive transistors and carries a complement LPB of the LATCHP signal.

Preferably the sense amplifier is shared by a column on each side thereof.

Three aspects of present invention therefore are:

(1) the connection of each sense amplifier via transistors or other switching devices to the power supply lines without directly connecting together power supply lines for multiple sense amplifiers;

(2) the use of local read amplifiers; and

(3) the use of local write circuitry.

Further aspects of the invention exist, and these three are mentioned as salient points. While it may not be necessary to employ all three in combination to embody the present invention, the use of all three features is most beneficial.

In describing the prior art and the present invention, reference has been made and will be made to accompanying drawings wherein:

Figure 1 shows a typical CMOS sense amplifier group;

Figure 2 shows the same group of sense amplifiers connected according to one prior art modification;

Figure 3 shows the same prior art sense amplifier with pass transistors for a global column select and for block enable features;

Figure 4 shows three such prior art sense amplifiers having column select and block enable capabilities and illustrating the voltages applied from time to time depending on the current state of the sense amplifier;

Figure 5 illustrates a sense amplifier constructed according to a preferred embodiment of the present invention;

Figure 6 shows a simplified form of the sense amplifier of the present invention collected into a group of such sense amplifiers according to a further aspect of the invention;

Figure 7 shows how the sense amplifier of the present invention may operate in various modes; and

Figure 8 shows how the preferred sense amplifier may be connected selectively to two pairs of bit lines.

Figure 5 illustrates a preferred sense amplifier 100 according to various aspects of the present invention. Amplifier 100 includes internal nodes 102 and 104 in a latch formed by transistors 112, 114, 118 and 120. Node 102 is coupled to the gate electrodes of P channel transistor 112 and N channel transistor 118, whereas node 104 is coupled to the gate electrodes of P channel transistor 114 and N channel transistor 120. The configuration of the flip-flop itself within the sense amplifier is the same as that of sense amplifier 10.

A column write select signal Y_w is coupled to the gate electrodes of pass transistors 122, 124. Preferably, the column write signal YW and a column read signal YR describe below are decoded for each four columns, so that each four columns has a unique YW and YR. However, this is unnecessary to embody the principles of the invention. In one configuration, each subarray may be fairly large -- 4Meg illustratively -- and may have a respective column decoder that will generate column select signals for that whole subarray. It is desired to be able to write to just one block within the subarray. That will be an "active block" wherein the sense amplifiers are active. An "inactive block" is one where the sense amplifiers are in precharge.

Returning to the description of Fig. 5, however, the source-drain path of pass transistor 122 is coupled to node 104, and the source-drain path of transistor 124 is coupled to node 102.

Transistor 122 is also coupled to a node 126 between the source electrode of a local data write driver transistor 128 and the drain of another local data write driver transistor 130. Transistors 128 and 130 are N channel devices having their source-drain paths coupled in series. The drain of transistor 128 is coupled to VCC and the source of transistor 130 is coupled to ground. A data write signal DW is coupled to the gate electrode of transistor 128 and its complement DWB is coupled to the gate electrode of transistor 130. A similar configuration exists on the right side of sense amplifier 100 where transistors 132 and 134 are coupled between VCC and ground and have a node 136 therebetween which is coupled to transistor 124. Note, however, that the data write signal DW is coupled to control transistor 134 whereas its complement DWB is coupled to the gate electrode of transistor 132. That is to say, the data write signal DW turns on a pull-up transistor 128 on the left side of the sense amplifier 100, but turns on a pull down transistor 134 on the right side of sense amplifier 100. Its complementary signal DWB likewise has reciprocal effects on the left and right sides.

The source electrodes of P channel transistors 112 and 114 within amplifier 100 are coupled to a further P channel transistor 140, the source electrode of which is coupled to VCC (or LATCHP). The gate electrode of this P channel device 140 is coupled to receive a signal LPB which is the logical complement of LATCHP. FET 140 is referred to as a local sense amplifier drive transistor. Similarly, the source electrodes of the N channel transistors 118 and 120 within amplifier 100 are coupled to ground through the source-drain path of a further local sense amplifier drive transistor 142. The gate electrode of transistor 142 is coupled to receive signal LNB which is the logical complement of LATCHN.

The lower portion of Figure 5 includes a local column read amplifier which includes four N channel transistors 150, 152, 154, and 156. The source-drain paths of transistors 150 and 152 are coupled in series. The drain electrode of transistor 150 receives a signal DRB which is a logical complement of a data read signal DR. The source electrode of transistor 152 is coupled to ground. Node 104 is coupled via a conductive line 158 to the gate electrode of transistor 152. The gate electrode of transistor 150 is coupled to a column read signal Y_R. The source-drain path of transistors 154 and 156 are coupled in series between the data read signal DR and ground. The gate electrode of transistor 154 is coupled to the gate electrode of transistor 150, and accordingly is coupled to the column read signal Y_R. The gate electrode of transistor 156 is coupled to internal node 102 via a conductive line 160.

Hence, the circuit of Figure 5 includes data read circuitry formed by transistors 150 through 156. Transistors 128, 130, 132 and 134 comprise local data write transistors. Transistors 140 and 142 comprise local sense amplifier drive transistors. It will be understood that there are thousands of such circuits 100 in a large integrated circuit memory. The signals LPB and LNB connected to the local sense amplifier drive transistors, the data write signal DW and its complement DWB coupled to the local data write driver transistors, and the data read signals DR and DRB are shared among or applied to many sense amplifiers on the memory

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