
R. JACOB (JAKE) BAKER, PH.D., P.E.

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EDUCATION

Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*

M.S. and B.S. in Electrical Engineering; May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, and the AFRL.
- Current research and development interests are:
 - Circuit design for the control, use, and storage of renewable energy using thermoelectric generators
 - Design of electrical/biological circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories and digital systems
 - Analog and mixed-signal circuit design for communication systems, synchronization, energy storage, data conversion, and interfaces

- The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
- Reconfigurable electronics design using nascent memory technologies
- Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
- Power electronics circuit design for consumers and consumer electronics
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

- 2013 - present:** Working with Freedom Photonics and Attollo Engineering in the Santa Barbara area on the integration of optoelectronics with CMOS integrated circuits.
- 2013 - present:** Working with National Security Technologies, LLC,) on the Design of Integrated electrical/photonic application specific integrated circuit (ASIC) design.
- 2013 - 2015:** Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.
- 2010 - 2013:** Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.
- 2013:** Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.
- 2012:** Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.
- 2010 - 2012:** Working with Aeries Photonics (and then FLIR Inc. when Aeries was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.
- 2009 - 2010:** Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.
- 2009 - 2010:** Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.
- 1994 - 2008:** Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for

MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory using the MTJ memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1998: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)

Member of the honor societies Eta Kappa Nu and Tau Beta Pi

Licensed Professional Engineer

HONORS AND AWARDS

- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013 - 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007

- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2017) for the *IEEE Solid-State Circuits Magazine*, as a Distinguished Lecturer for the SSCS (2012-2015), and as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015.

ARMED FORCES

6 years United States Marine Corps reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge, October 23, 1987

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition" *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) **Over 50,000 copies of this book's three editions in print.**

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 978-0-470-18475-2

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0-7803-6014-1

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, CRC Press, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICySSS keynote, IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING (last 5 years only)

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2016-2017) "Testing and development of BiCMOS photodetectors and diagnostic instrumentation," Department of Energy, National Security Technologies, LLC, \$181,605
- Baker, R. Jacob, (2016-2017) "Dual-Mode, Extended Near Infrared, Focal Plane Arrays fabricated with a Commercial SiGe BiCMOS Process," DARPA, \$41,892
- Baker, R. Jacob, (2016-2018) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665
- Baker, R. Jacob, (2015-2016) "Photodetectors and high-speed electronics using Silicon Germanium (SiGe) Bipolar/CMOS (BiCMOS) integrated circuits," Department of Energy, National Security Technologies, LLC, \$100,000
- Baker, R. Jacob, (2015-2016) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$45,000
- Baker, R. Jacob, (2015) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$45,000

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