

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,  
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,  
Patent Owner.

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Case IPR2017-00039  
Patent 6,195,302 B1

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Before JAMESON LEE, KEVIN F. TURNER, and  
JOHN A. HUDALLA, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*Inter Partes* Review  
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

Petitioner, Samsung Electronics Co., Ltd. (“Petitioner”), filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–6, 10–12, and 14–18 of U.S. Patent No. 6,195,302 B1 (Ex. 1001, “the ’302 Patent”) pursuant to 35 U.S.C. §§ 311–319. Patent Owner, ProMOS Technologies, Inc. (“Patent Owner”), did not file a Preliminary Response. We determined that the information presented in the Petition established that there is a reasonable likelihood that Petitioner would prevail in challenging claims 1–6, 10–12, and 14–18 of the ’302 Patent under 35 U.S.C. § 103(a). Pursuant to 35 U.S.C. § 314, we instituted this proceeding on April 11, 2017, as to the challenged claims of the ’302 Patent. Paper 6 (“Institution Decision” or “Dec. on Inst.”).

During the course of trial, Patent Owner filed a Patent Owner Response (Paper 10, “PO Resp.”), and Petitioner filed a Reply to the Patent Owner Response (Paper 12, “Reply”). The parties filed a “Joint Stipulation Regarding Scheduling Order” (Paper 13) in which “the parties waive[d] oral argument in this proceeding,” so no oral hearing was held. *See* Paper 14.

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–6, 10–12, and 14–18 of the ’302 Patent. For the reasons discussed below, Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable.

## I. BACKGROUND

### A. *Related Proceedings*

Petitioner and Patent Owner indicate that the ’302 Patent has been asserted by Patent Owner in *ProMOS Technologies, Inc. v. Samsung*

IPR2017-00039  
Patent 6,195,302 B1

*Electronics Co., Ltd., et al.*, No. 1:15-cv-898-SLR-SRF (D. Del.). Pet. 1; Paper 5, 1. The '302 Patent is also the subject of another petition, also filed by Petitioner, seeking *inter partes* review of claims 1–6 and 10–12 under different grounds of unpatentability, IPR2017-00038, where a trial was instituted in that proceeding as well.

Petitioner and Patent Owner indicate that these patents are related to the '302 patent: U.S. Patent Nos. 5,761,112; 6,849,897; 6,020,259; 6,088,270; and 6,699,789. *Id.* Patent Owner identifies these *inter partes* review proceedings for the related patents: IPR2017-00032 (Patent No. 6,849,897); IPR2017-00033 and IPR2017-00035 (Patent No. 6,020,259); IPR2017-00036 (Patent No. 6,088,270); IPR2017-00037 (Patent No. 6,699,789); and IPR2017-00040 (Patent No. 5,761,112). Paper 5, 1.

*B. The '302 Patent*

The '302 Patent is directed to a random access memory and the operations within a random access memory for reading or refreshing memory cells, specifically applied to sense amplifiers. Ex. 1001, 1:7–9.

The '302 Patent discloses a memory device with sense amplifiers, as illustrated in Figure 1, reproduced below:

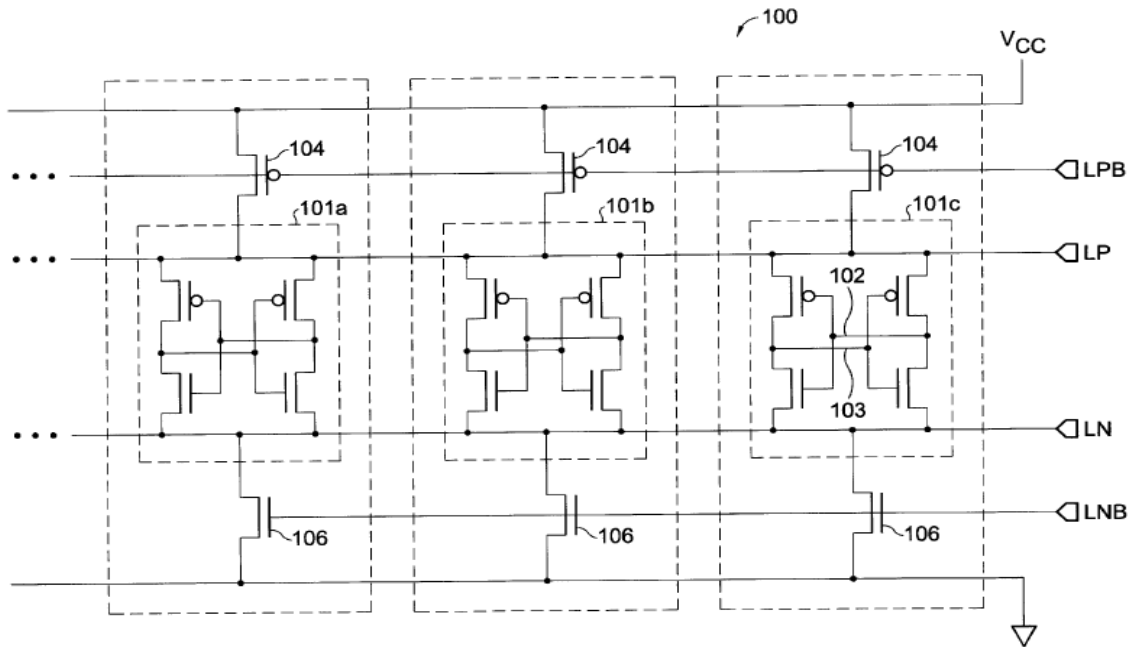


FIG. 1

Figure 1 illustrates a memory device according to an embodiment of the '302 Patent.

Sense amplifiers 101a–101c are coupled to high voltage line Vcc and ground via driver transistors 104 and 106, respectively. *Id.* at 4:40–5:4. Driver transistors 104, which are PMOS pull-up transistors, and driver transistors 106, which are NMOS pull-down transistors, are controlled by control signals LPB and LNB, respectively. *Id.* The '302 Patent illustrates

the functionalities of the sense amplifiers with respect to Figure 2,  
reproduced below:

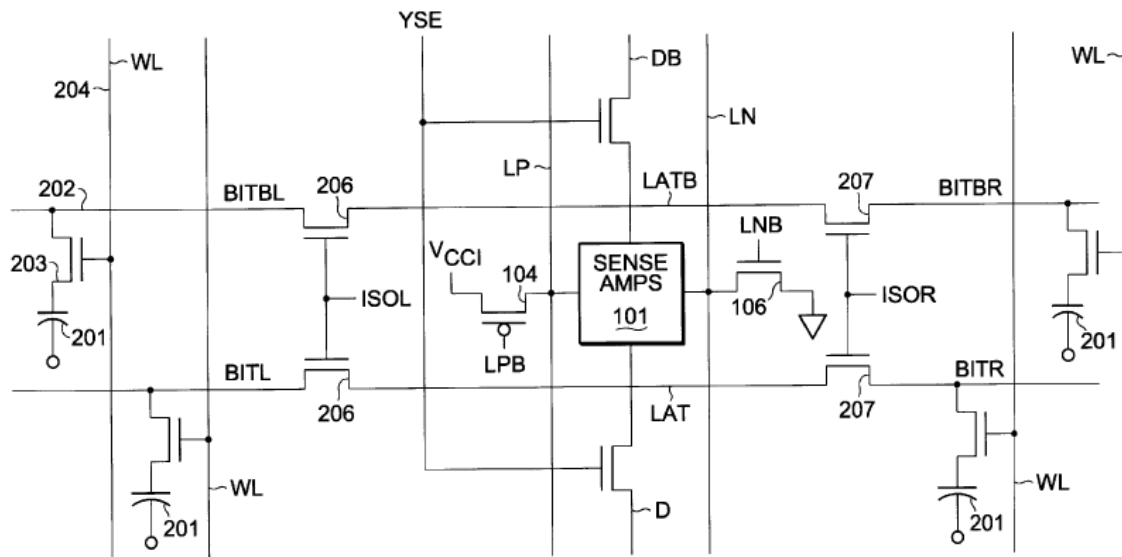


FIG. 2

Figure 2 illustrates a portion of a memory device according to an embodiment of the '302 Patent.

The '302 Patent discloses that storage capacitors 201 are selectively coupled to bit lines 202 through access switches 203 in response to address signals supplied to word lines 204. *Id.* at 5:5–9. Prior to a read operation, a pair of bit lines 202 are “equalized at some voltage between a logic high and a logic low signal,” and a word line (WL) signal is activated. *Id.* at 5:18–21, 5:35–37. After the WL signal is activated, “the LPB signal is driven to a logic low[,] coupling VCCI to sense amp 101 through drive transistor 104 [and] [s]imilarly, the LNB signal is driven high to couple sense amp 101 to ground or Vss through drive transistor 106.” *Id.* at 5:38–42. The '302 Patent also provides that “LNB and LPB are generated by a circuit such as that

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