

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KINGSTON TECHNOLOGY COMPANY, INC.,  
Petitioner,

v.

POLARIS INNOVATIONS LTD.,  
Patent Owner.

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Case IPR2017-00116  
Patent 7,334,150 B2

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Before SALLY C. MEDLEY, BARBARA A. PARVIS, and  
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

I. INTRODUCTION

Kingston Technology Company, Inc. (“Petitioner”) filed a Petition for *inter partes* review of claims 1–3, 5, 6, and 8–11 (“challenged patents”) of U.S. Patent No. 7,334,150 B2 (Ex. 1001, “the ’150 Patent”). Paper 2

IPR2017-00116  
Patent 7,334,150 B2

(“Pet.”). In support of its Petition, Petitioner proffers a Declaration of Dr. Vivek Subramanian. Ex. 1011. Polaris Innovations Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). Upon consideration of the parties’ contentions and supporting evidence, we instituted an *inter partes* review pursuant to 35 U.S.C. § 314, as to claims 1–3, 5, 6, and 8–11 of the ’150 Patent. Paper 9 (“Dec.”).

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 17, “PO Resp.”). In support of its Patent Owner Response, Patent Owner proffers the Declaration of Dr. Joseph Bernstein. Ex. 2019. Petitioner filed a Reply to Patent Owner’s Response (Paper 20, “Pet. Reply”). On December 6, 2017, we held an oral hearing. Paper 30 (“Tr.”).

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3, 5, 6, and 8–11 of the ’150 Patent are unpatentable.

#### *A. Related Matters*

The parties state that the ’150 Patent is the subject of a pending lawsuit in the Central District of California, i.e., *Polaris Innovations Ltd. v. Kingston Tech. Co.*, Case No. 8:16–cv-300 (C.D. Cal.),<sup>1</sup> and the lawsuit includes assertions against Petitioner. Pet. 2; Paper 3 (Patent Owner’s Mandatory Notices), 1; Paper 16 (Patent Owner’s Supplemental Mandatory Notices).

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<sup>1</sup> This lawsuit is referred to herein as the “companion district court lawsuit.”

*B. The '150 Patent*

The '150 Patent is directed to a semiconductor memory module that includes a register circuit and a clock signal regeneration circuit. Ex. 1001, 1:9–16. Figure 2 is reproduced below.

FIG 2

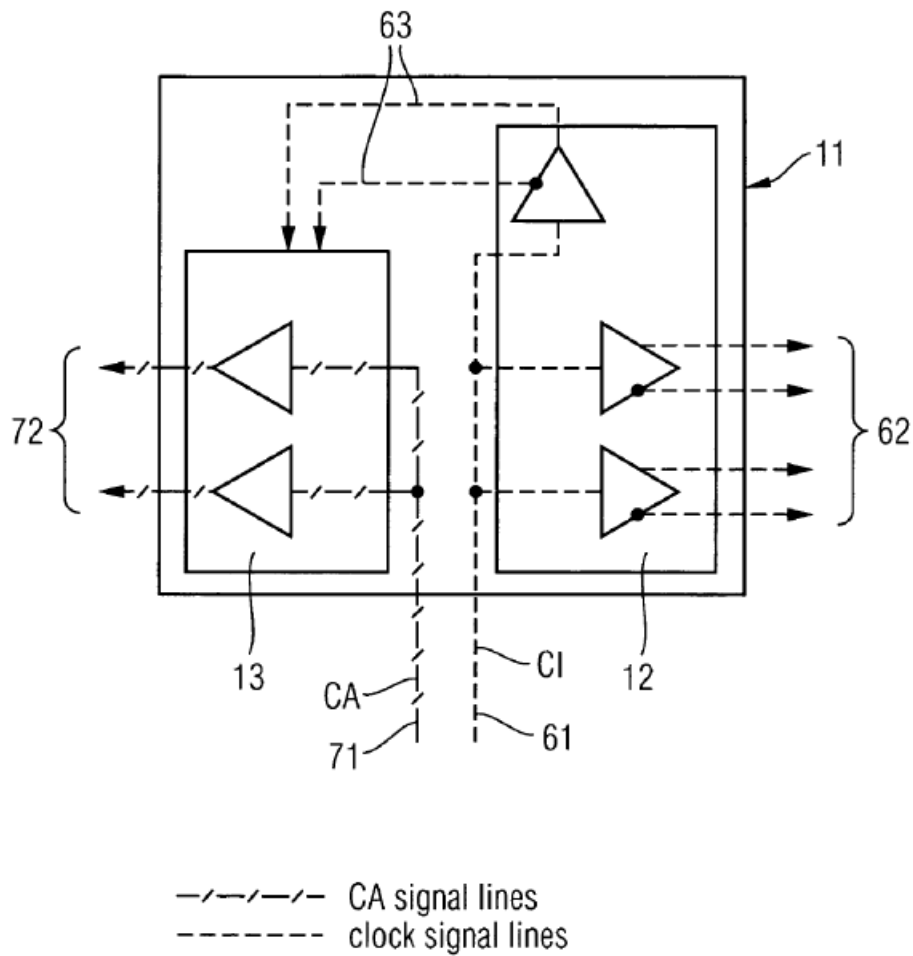


Figure 2 shows a top view of a clock signal regeneration circuit and register circuit in a common chip packing.

As shown in Figure 2 above, chip packing 11 contains clock signal regeneration circuit 12 and register circuit 13. Ex. 1001, 4:30–33. Differential clock signal input line 61 supplies clock signal Cl to common chip packing 11. *Id.* at 4:41–43. Line section 71 supplies command and address input signals “CA.” *Id.* at 4:43–45. Differential clock signal lines 62 from clock signal regeneration circuit 12 supply the conditioned clock signal to memory chips 4 and 4a. *Id.* at 4:49–53. Differential clock signal lines 63 supply the conditioned clock signal to register circuit 13. *Id.* at 4:54–56. From register circuit 13, temporarily stored command and address signals are supplied by differential command and address signal lines 72 to memory chips 4 and 4a. *Id.* at 4:56–60.

### *C. Illustrative Claim*

Petitioner challenges claims 1–3, 5, 6, and 8–11 of the ’150 Patent. Claim 1 is an independent claim. Claims 2, 3, 5, 6, and 8–11 depend directly from claim 1. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A memory module comprising:
  - a plurality of memory chips arranged on the memory module;
  - a plurality of bus signal lines operable to supply an incoming clock signal and incoming command and address signals to at least the memory chips;
  - a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having a same frequency as the incoming clock signal; and
  - a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock

signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

*Id.* at 7:1–25.

*D. Instituted Grounds of Unpatentability*

Petitioner asserts that claims 1–3, 5, 6, and 8–11 are unpatentable based on the following grounds (Pet. 4):

<b>Reference(s)</b>	<b>Basis</b>	<b>Challenged Claim(s)</b>
Lee <sup>2</sup>	§ 103(a)	1, 2, 5, 6, and 8–10
Lee and Keeth	§ 103(a)	3 and 11
Dodd <sup>3</sup>	§ 103(a)	1, 2, 5, 6, and 8–10
Dodd and Keeth <sup>4</sup>	§ 103(a)	3 and 11

We instituted on all of the asserted grounds of unpatentability above. Dec. 33.

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<sup>2</sup> U.S. Patent No. 6,898,726 B1, issued May 24, 2005 (Ex. 1008) (“Lee”).

<sup>3</sup> U.S. Patent No. 6,530,006 B1, issued Mar. 4, 2003 (Ex. 1003) (“Dodd”).

<sup>4</sup> U.S. Patent No. 7,123,046 B2, issue Oct. 17, 2006 (Ex. 1016) (“Keeth”).

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