

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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NETAPP, INC.,  
Petitioner,

v.

INTELLECTUAL VENTURES II, LLC,  
Patent Owner.

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Case IPR2017-00276  
Patent 6,633,945 B1

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Before JEFFREY S. SMITH, JENNIFER S. BISK, and BEVERLY M.  
BUNTING, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

DECISION  
Instituting *Inter Partes* Review  
37 C.F.R. § 42.108

## I. INTRODUCTION

Petitioner filed a Petition<sup>1</sup> for *inter partes* review of claims 1 and 6 of U.S. Patent No. 6,633,945 B1 (Ex. 1001, “the ’945 patent”). Paper 13 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). By statute, institution of an *inter partes* review may not be authorized “unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see also* 37 C.F.R. § 42.108.

Upon consideration of the Petition and the Preliminary Response, we are persuaded Petitioner has demonstrated a reasonable likelihood that it would prevail in establishing the unpatentability of claims 1 and 6 of the ’945 patent. Accordingly, we institute an *inter partes* review of claims 1 and 6 based on the grounds identified in the Order section of this decision.

### A. Related Matters

Both parties identify that the ’945 patent was asserted against NetApp Inc. in *Intellectual Ventures I, LLC v. NetApp Inc.*, Case No. 1:16-cv-10868-IT (D. Mass.), filed May 11, 2016. Pet. 17; Paper 4.

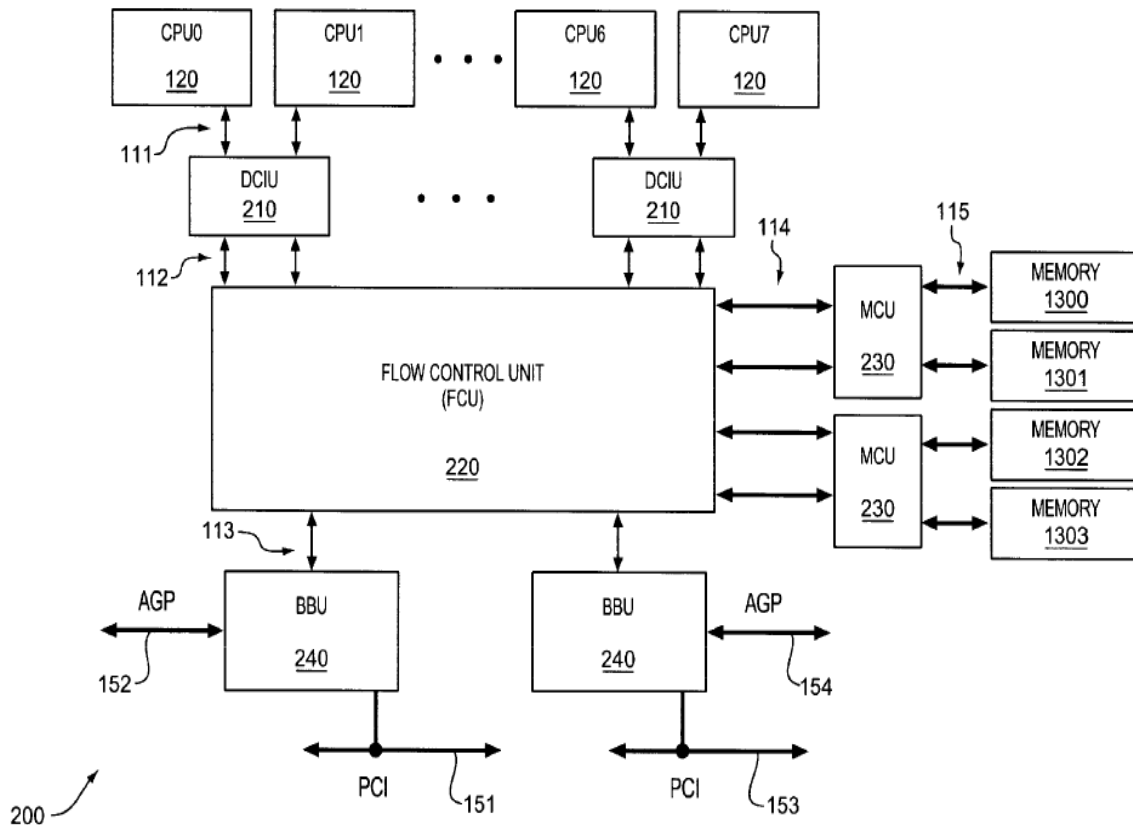
### B. The ’945 Patent

The ’945 patent relates generally to a fully connected multiple flow control unit (FCU) based architecture to reduce memory read latencies. Ex.

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<sup>1</sup> Petitioner filed an Original Petition on Nov. 18, 2016 (Paper 1), and a Corrected Petition on May 8, 2017 (Paper 13). In this Decision we cite to the Corrected Petition.

1001, 1:66–2:1. A symmetric multiprocessor system includes a switch matrix for data transfers that provides multiple concurrent buses that enable increased bandwidth between processors and shared memory. Ex. 1001, Abstract. A high-speed point-to-point channel couples command initiators and memory with the switch matrix and with input/output (I/O) subsystems. *Id.* Figure 2 of the '945 patent is reproduced below.



**FIG. 2**

Figure 2, above, shows a symmetric shared-memory multiprocessor system using a switched-fabric data path architecture centered on FCU 220. Ex. 1001, 2:59–62. Point-to-point (PP) interconnections 112, 113, and 114 provide channel interfaces between FCU 220 and dual CPU interface units (DCIUs) 210, memory control units (MCUs) 230, and bus bridge units (BBUs) 240, respectively. *Id.* at 2:67–3:8, 3:11–15.

Figure 12 of the '945 patent is reproduced below.

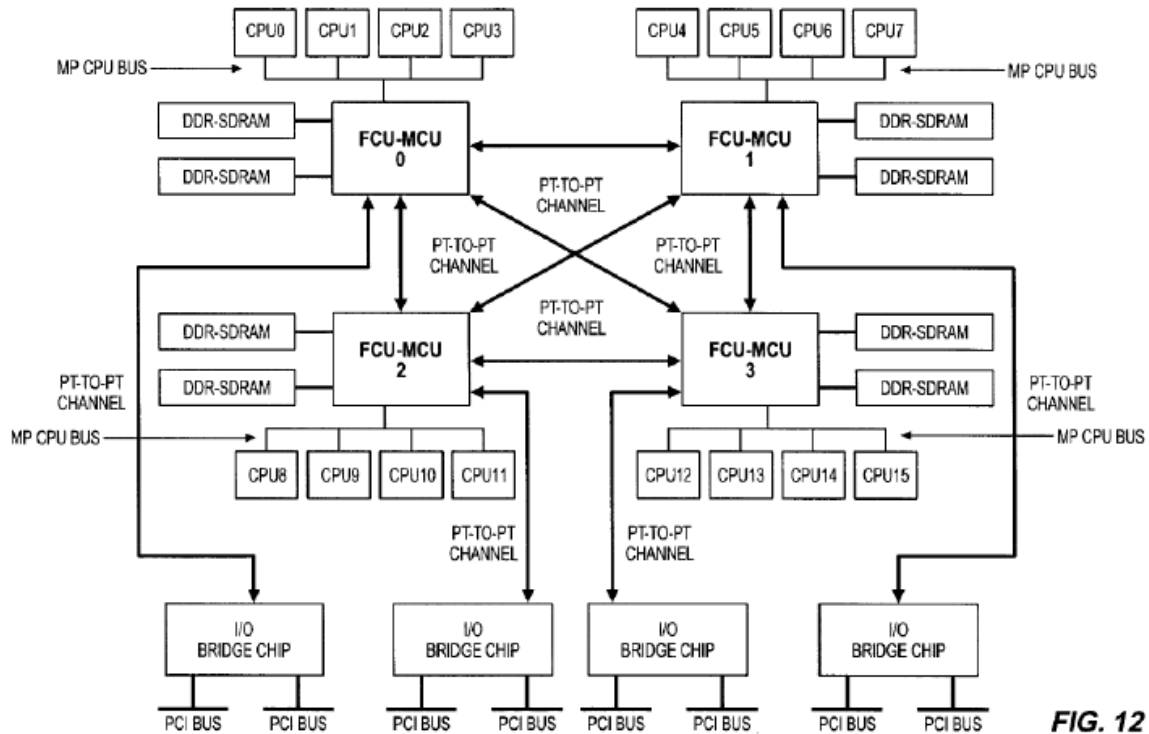


Figure 12, above, shows fully connected multiple FCU architectures. *Id.* at 6:22–23, 6:62–7:57. The interconnections between FCUs are point-to-point. *Id.* at 7:14–15. Each FCU has direction connection to all other FCUs and maintains cache coherency for transactions that belong to its memory region via the point-to-point interconnections. *Id.* at 7:15–21.

### C. Illustrative Claim

Challenged claims 1 and 6 of the '945 patent are independent. Claim 1 is illustrative of the claimed subject matter:

1. A multi-processor shared memory system comprising:
  - a first set of point-to-point connections;
  - a first set of processors each coupled to one of the first set of point-to-point connections;

a first memory coupled to one of the first set of point-to-point connections;

a first flow control unit including a first data switch coupled to the first set of point-to-point connections wherein the first data switch is configured to interconnect the first set of point-to-point connections to provide first data paths between the first memory and the first set of processors;

a second set of point-to-point connections;

a second set of processors each coupled to one of the second set of point-to-point connections;

a second memory coupled to one of the second set of point-to-point connections;

a second flow control unit including a second data switch coupled to the second set of point-to-point connections wherein the second data switch is configured to interconnect the second set of point-to-point connections to provide second data paths between the second memory and the second set of processors;  
and

a third point-to-point connection coupled to the first data switch and to the second data switch wherein the first data switch is configured to interconnect the first set of point-to-point connections to the third point-to-point connection and the second data switch is configured to interconnect the second set of point-to-point connections to the third point-to-point connection to provide third data paths between the second memory and the first set of processors and between the first memory and the second set of processors.

Ex. 1001, 9:2–36.

#### *D. References*

Petitioner relies on the following references. Pet. 25.

<b>Reference</b>	<b>Patent No.</b>	<b>Date</b>	<b>Ex. No.</b>
Sharma	US 6,055,605	Apr. 25, 2000	1002

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