UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICAN INC.,
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00577
Patent 8,516,185 B2

Record of Oral Hearing
Held: April 6, 2018

Before BRYAN F. MOORE, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE,
Administrative Patent Judges.

APPEARANCES:

ON BEHALF OF THE PETITIONER:

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The above-entitled matter came on for hearing on Friday, April 6, 2018, commencing at 3:30 p.m., at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

PROCEEDINGS

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JUDGE MOORE: Okay. We're at the second, I guess you would say, oral hearing of the day; this specifically for IPR2017-00577. Just to remind the parties, because we have new counsel here, that we have judges that are remote. They're not able to see the Elmo and the courtroom in the way that we are here; so be sure that you do indicate what page in the demonstratives you're on, and also if you're pointing to a figure, just be clear that your description is full in words, and don't rely on people being able to see the figure, necessarily, to understand your descriptions.

And for the new counsel, with me here are Judges Clements and McShane; so we should have a rollcall starting with the Petitioner.

MR. MICALLEF: Thank you, Your Honor -- Joe Micallef for the Petitioner. With me is my partner Steve Baik and my colleagues Wonjoo Suh, and Mr. Pazmandi.

JUDGE MOORE: Thank you; for Patent Owner.

MR. ARJOMAND: Good afternoon, Your Honors --. Mehran Arjomand of Morrison & Foerster for, Patent Owner, Netlist. With me is my colleague, David Kim.

JUDGE MOORE: Thank you; whenever you're ready.

MR. MICALLEF[CM1]: Thank you, Your Honor. This is the 577 proceeding, it relates to the 185 Patent. We have a number slides; I do not intend to use them all, but I will go through some of them. There is one ground at issue here, Your Honor; it is a ground of obviousness based on Halbert in view of Amidi. There's also really only one claim element in play which the parties have referred to as a selectively allowed limitation. What I'd like to do first is very briefly do an overview of the patent and the prior art, and that limitation, and then move on to some other things.

JUDGE MOORE: And I understand you weren't prepared -- and this maybe out of left field, but only because I was on it -- I know that a reset, remand came back on a term limitation selectively, electrically isolating which, of course, as you've mentioned, is not in controversy here but does exist in this case; and so, again, if you know, is there anything about the Fed Circuit's ruling of that limitation that would have an effect on what we're doing here?

MR. MICALLEF: No, I don't think so. I don't think that there's been any issue

raised that would affect this hearing. Of course, I believe the Board has actually issued an opinion after that remand.

JUDGE MOORE: Right. Yes, a remand opinion went out.

MR. MICALLEF: I don't think that affects us here.

JUDGE MOORE: Okay. And Patent Owner , do you agree, and once again, I understand you may not be aware of this issue and it wasn't brought up in any papers or anything in this, but just if you know?

MR. ARJOMAND: Your Honor, I don't believe those remand decisions impact the hearing today. There's no load isolation in the 185 Patent.

JUDGE MOORE: Right.

MR. MICALLEF: Thank you, Your Honor.

JUDGE MOORE: And I didn't mention, we have, I think, 30 minutes per side; so, do you want to reserve some time for rebuttal?

MR. MICALLEF: I'd like to reserve 10 minutes, Your Honor; and perhaps more if I finish my presentation.

JUDGE MOORE: 10 minutes, okay. Right; you'll get all the time that you have remaining, but I will make you aware when you are approaching your 10 minutes that you plan to hold.

MR. MICALLEF: Great; thank you. So, the 185 Patent, Your Honor, issued from a patent application filed in 2010 -- it was a CIP of an application filed in 2009. They've claimed priority back to 2009. It states that the problem in the prior art -- there was a problem because of the increased number of memory devices that were being used that increased the resistive and capacitive load on the memory bus leading to some signal propagation issues. The 185 Patent proposes to solve this problem by placing a number of circuits in the data path between the memory devices; and the system memory controller refers to it variously as load reducing circuits or load reducing switching circuits.

I'm on slide 8 of our slides, our demonstratives. In Figure 5 of the Patent there's sort of a blowout of these -- a diagram of one of these switching circuits; and you can see that in the middle of this diagram there is -- and we've highlighted in yellow -- a multiplexer 508, that selects between memory ranks. And we've shown on this slide just

sort of the selection of the data path towards and away from memory ranks a to c, and not memory ranks b to d and, of course, the multiplexer could select in the opposite way.

Here on slide 9, I've placed what we have been referring to as the selectively allowed limitation and I think it's important to just stop here for a second because the words of the claim actually do matter, obviously; and what this claim element says is that each circuit of the plurality of circuits is configured to selectively allow data transmission between the system memory controller and at least one memory device, and then it goes on. But why I want to stop on it is to point out what's not in this claim language. It does not require a multiplexer. In fact, it does not require any specific circuitry whatsoever. The Patentee chose to draft this particular element of the claim in terms of generic circuitry -- a plurality of circuits -- configured to perform certain functionality. So, that's the claim language that's at issue in this proceeding right here.

Now, the Board instituted on Halbert in view of Amidi -- so, let me very briefly talk about Halbert and Amidi. Halbert's a prior art patent 102B, issued in 2006. It discloses a memory module -- I'm here on slide 12. For example, in Figure 7 of Halbert shown on this slide, a number of memory devices 140, a plurality of interfaced circuits here -- left interface circuit 125 and R interface circuit 130 in the data path -- controlling communication with these memory devices. Halbert also has a blowout of his interface circuits -- this is slide 13, and here we've annotated Figure 4 of Halbert -- and you can see in this fit circuit, again in the middle, there is a multiplexer which selects between either the path to the upper rank, which I think is rank 140 of memory devices, and that's shown on the left, or the path on the right which is, I think, rank 142.

Now we argued in the petition that this satisfied the claim element that we're talking about today. The Board declined to institute on that; and, instead, found that Amidi taught that claim element. And so -- I'm at slide 14; let me just talk about Amidi very briefly. Published patent application in 2006 -- again, that's 102b prior art . It also discloses a memory module. In this memory module though there is controlled circuitry that permits what has been referred to as chip select emulation functionality. In the system disclosed in Amidi, the system memory controller would provide two chip select signals which would permit the activation of one or two memory ranks. Amidi says you could instead take those chip select signals -- and, I think, on the next slide, slide 16, it

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