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Paper 26
Entered: July 5, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00577
Patent 8,516,185 B2

Before BRYAN F. MOORE, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. 318(a)

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc., (collectively "Petitioner") filed a Petition (Paper 1, "Pet.") pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of 1–3, 7, 8, and 10–12 of U.S. Patent No. 8,516,185 B2 ("the '185 Patent," Ex. 1001). The Petition is supported by the Declaration of Harold S. Stone, Ph.D. ("Stone Declaration," "Stone Dec.," Ex. 1003). Netlist, Inc. ("Patent Owner") filed a Preliminary Response ("Prelim. Resp.," Paper 6).

On July 7, 2017, we instituted an *inter partes* review of claims 1–3, 7, 8, and 10–12 of the '185 Patent, but did not institute on all grounds. Paper 8, 6, 21 ("Inst. Dec."). Patent Owner filed a Response. Paper 12 ("PO Resp."). The Patent Owner Response is supported by the Declaration of R. Jacob Baker, Ph.D. ("Baker Declaration," "Baker Dec.," Ex. 2003). Petitioner filed a Reply. Paper 16 ("Reply").

On February 28, 2018, Patent Owner filed a motion to exclude. Paper 20 ("Mot. to Excl."). Petitioner filed a response to the motion to exclude. Paper 21 ("Mot. to Excl. Resp."). Patent Owner filed a reply to the response. Paper 22 ("Mot. to Excl. Reply").

An oral hearing was held on April 6, 2018. Paper 25 ("Tr.").

On May 2, 2018, pursuant to *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), we modified our institution decision to institute on all grounds presented in the Petition. Paper 24 ("SAS Order"). We invited the parties to request briefing regarding the newly added grounds and did not receive a request. *Id.*

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–3, 7, 8, and 10–12 are unpatentable.

A. Related Proceedings

Petitioner recites a list of District Court proceedings related to this *inter partes* review. Pet. ii.

B. The '185 Patent

The '185 patent relates generally to a memory module that includes a plurality of memory devices, a controller, and a plurality of circuits that are configured to selectively isolate the plurality of memory devices from the system memory controller. Ex. 1011, Abstract. In a conventional memory module, the system memory controller sees its load during a read or write operation as all of the memory devices, which causes significant performance issues. *Id.* at 4:47–52, 5:5–10, 11:34–38. To address this need, the '185 Patent discloses a memory module that employs data transmission circuits to reduce the load seen by the system memory controller. *Id.* at 10:41–47. Figure 3A of the '185 Patent is reproduced below.

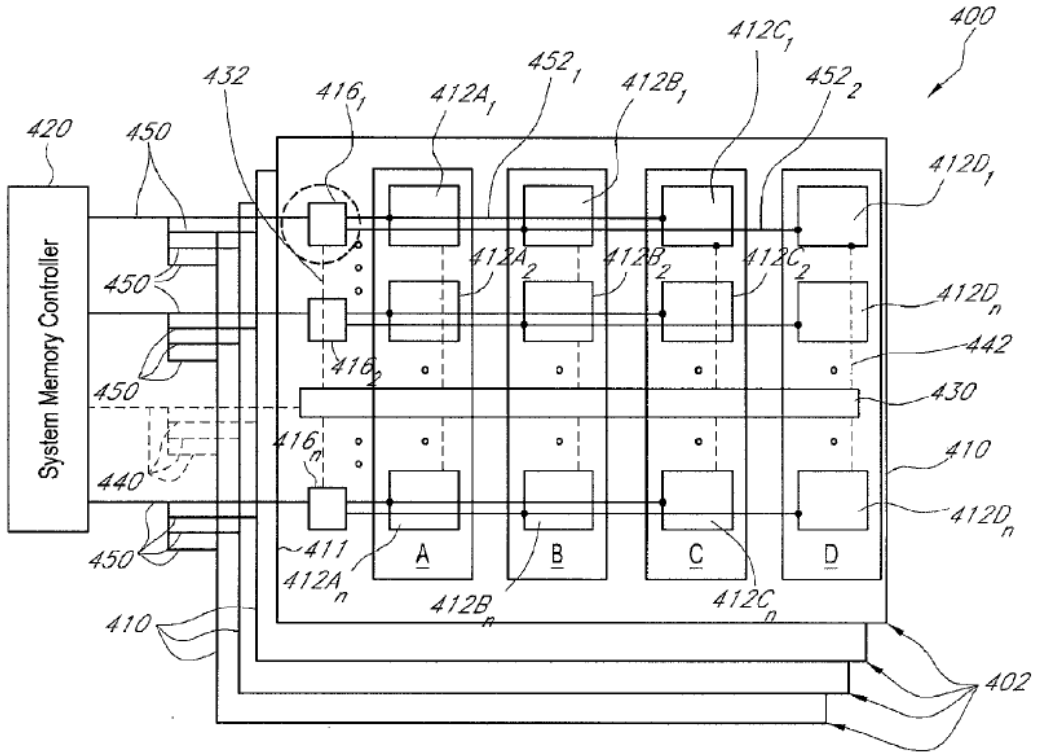

FIG. 3A

Figure 3A depicts an exemplary memory subsystem in accordance with one embodiment. *Id*. at 3:37–39. Each memory module 402 comprises multiple rows, or "ranks," of memory devices 412, control circuit 430, and a plurality of data transmission circuits 416. *Id.* at 7:61–8:13. In the embodiment depicted, each data transmission circuit 416 is coupled to four memory devices 412, and is configured to respond to module control signals from the control circuit 430 by selectively allowing or inhibiting data transmission between system memory controller 420 and at least one selected memory device. *Id.* at 8:13–31. System memory controller 420 is coupled to each memory module 402 by data lines 450 and address and control lines 440. *Id*. at 7:34–48. Because data lines 450 are operatively

coupled to single data transmission circuit 416 rather than to four memory devices 412, system memory controller 420 sees only a single load instead of concurrently seeing the loads of all four memory devices. *Id.* at 14:30–59. Thus, in comparison to prior art memory modules, the load seen by system memory controller 420 can be reduced by a factor of four. *Id*. at 14:59–62.

C. Illustrative Claim

Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory module comprising:
>
> a plurality of memory devices;
>
> a controller configured to receive control information from a system memory controller and to produce module control signals; and
>
> a plurality of circuits configured to receive the module control signals, each circuit of the plurality of circuits having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit width smaller than the first bit width, each circuit of the plurality of circuits comprising at least one write buffer and at least one read buffer and configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals, and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals, wherein each circuit of the plurality of circuits is operable, in response to the module control signals, to actively drive write data from the system memory controller to the at least one selected memory device of the at least two

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