

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00692
Patent 8,874,831 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION
Instituting *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–15 (“the challenged claims”) of U.S. Patent No. 8,874,831 B2 (Ex. 1001, “the ’831 patent”). Paper 1 (“Pet.”). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the ’831 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1–15 of the ’831 patent.

A. Related Proceedings

The ’831 patent is involved in *Netlist, Inc. v. Smart Modular Technologies, Inc. et al*, Case No. 2:13-cv-02613 (E.D. Cal.). Paper 4, 3. Related patents have been asserted in *Netlist, Inc. v. SMART Modular Technologies, Inc.*, Case No. 8-13-cv-00996 (C.D. Cal.), *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03916 (N.D. Cal.), *Diablo Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03901 (N.D. Cal.), and *Netlist, Inc. v. Smart Modular Technologies, Inc.*, 4-13-cv-05889

(N.D. Cal.). Pet. 2. Related patents are also the subject of *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00982 (PTAB) (institution denied), *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00994 (PTAB) (institution denied), *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01370 (PTAB) (institution denied); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01371 (PTAB) (institution denied), *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00587 (PTAB) (instituted June 22, 2017), and *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00649 (PTAB). Pet. 2; Paper 4, 3.

B. The '831 patent

The '831 patent, titled “Flash-Dram Hybrid Memory Module,” issued October 28, 2014, from U.S. Patent Application No. 13/559,476. Ex. 1001 at [54], [45], [21]. The '831 patent generally relates to a memory module with a non-volatile memory, a volatile memory, and a data manager through which the volatile memory and non-volatile memory may exchange data, and a controller to receive read/write commands from a memory controller hub (“MCH”) and transfer data between any two or more of the MCH, volatile memory, and non-volatile memory. *Id.* at Abstract. Figure 4A is reproduced below.

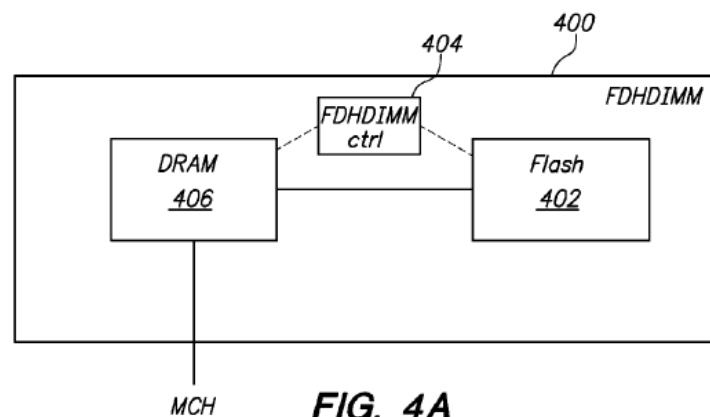


FIG. 4A

Figure 4A is a block diagram of a Flash-DRAM hybrid dynamic random access memory dual in-line memory module (DIMM). In this embodiment, volatile memory subsystem 406 (e.g. DRAM) is used as a data buffer such that data from Flash memory 402 is transferred to DRAM 406 at the Flash access speed, and buffered or collected into DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. *Id.* at 9:15–21. Similarly, when the MCH transfers data to DRAM 406, controller 404 manages the data transfer from DRAM 406 to Flash 402. *Id.* at 9:21–23.

Figure 5 is reproduced below.

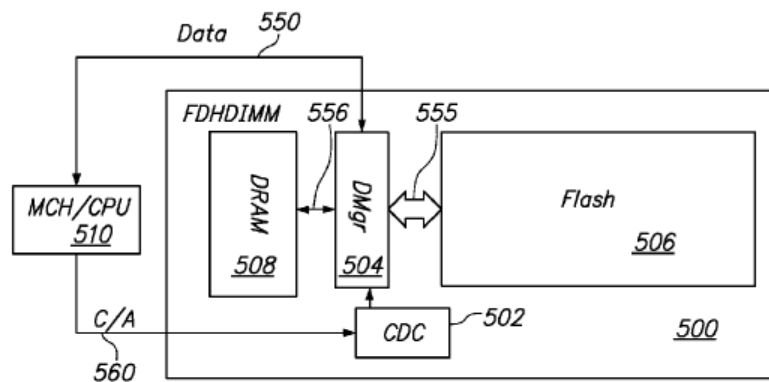


FIG. 5A

Figure 5A is a block diagram of memory module 500 in accordance with certain embodiments. Ex. 1001, 7:7–8. As shown in Figure 5, memory module 500 includes two on-module intermediary components: controller (CDC) 502 and data manager (DMgr) 504. *Id.* at 10:35–46. These components “manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.” *Id.* at 10:49–53. “In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM

memory from/to MCH 510.” *Id.* at 10:54–56. “In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction.” *Id.* at 11:18–21.

Figure 6 is reproduced below.

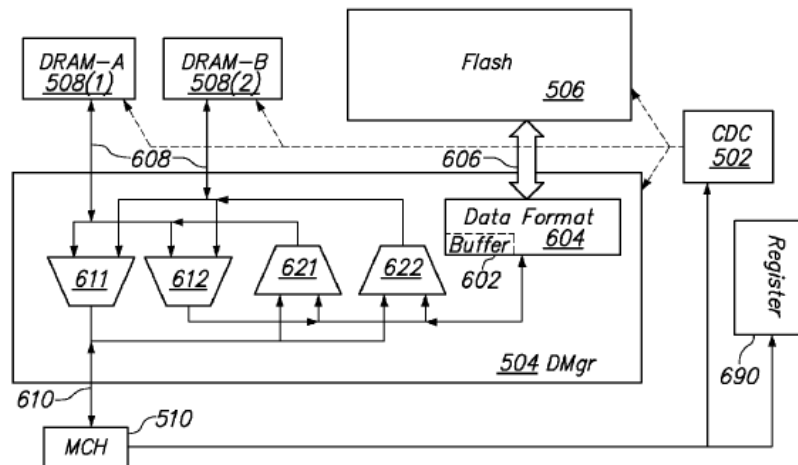


FIG. 6

Figure 6 is a block diagram showing some details of data manager 504. Ex. 1001, 7:11–12. “In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric.” *Id.* at 12:1–3. “For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508.” *Id.* at 12:3–5. “Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506.” *Id.* at 12:5–8. “Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B).” *Id.* at 12:8–11.

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