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Paper No. 8
Entered: July 21, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00730
Patent 9,128,632 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE *Administrative Patent Judges.*

CLEMENTS, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–5, 12–14, 19, and 20 ("the challenged claims") of U.S. Patent No. 9,128,632 B2 (Ex. 1001, "the '632 patent"). Paper 1 ("Pet."). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner does not establish a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '632 patent. Accordingly, pursuant to 35 U.S.C. § 314, we deny institution of an *inter partes* review of claims 1–5, 12–14, 19, and 20 of the '632 patent.

A. Related Proceedings

Petitioner represents that the '632 patent is not involved in any other legal proceedings to its knowledge. Pet. 1. Patent Owner identifies U.S. Patent Application No. 14/846,993 as the only related matter. Paper 5, 1.

B. The '632 patent

The '632 patent, titled "Memory Module with Distributed Data Buffers and Method of Operation," issued September 8, 2015, from U.S.

Patent Application No. 13/952,599. Ex. 1001 at [54], [45], [21]. The '632 patent generally relates to a memory module that includes memory devices, a module control device, and data buffers (also called "buffer circuits" or "isolation devices"). *Id.* at 3:8–10. "The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices." *Id.* at 3:33–36. "Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock." *Id.* at 3:36–39. "Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller." *Id.* at 3:39–42. "Thus, the memory controller does not have direct control of the memory devices." *Id.* at 3:42–43.

Figure 1 of the '632 patent is reproduced below.

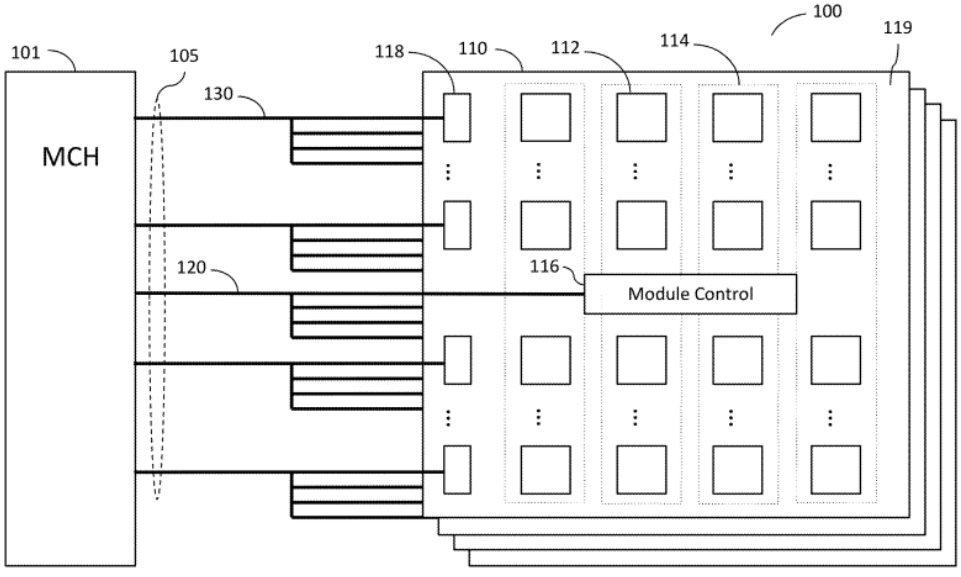

FIG. 1

As shown in Figure 1, memory controller (MCH) 101 and one or more memory modules 110 are coupled by memory bus 5, which includes command/address (C/A) signal lines 120 and groups of system data/strobe signal lines 130. *Id.* at 4:1–5. "[E]ach memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114." *Id.* at 4:6–7. Each memory module 110 also includes module control circuit 116 coupled to MCH 101 via C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to MCH 101 via respective groups of system data/strobe signal lines 130. *Id.* at 4:7–13. "[S]ystem 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101." *Id.* at 7:47–49.

Figure 12A, reproduced below, is a timing diagram for a write operation according to one embodiment. *Id.* at 14:60–61.

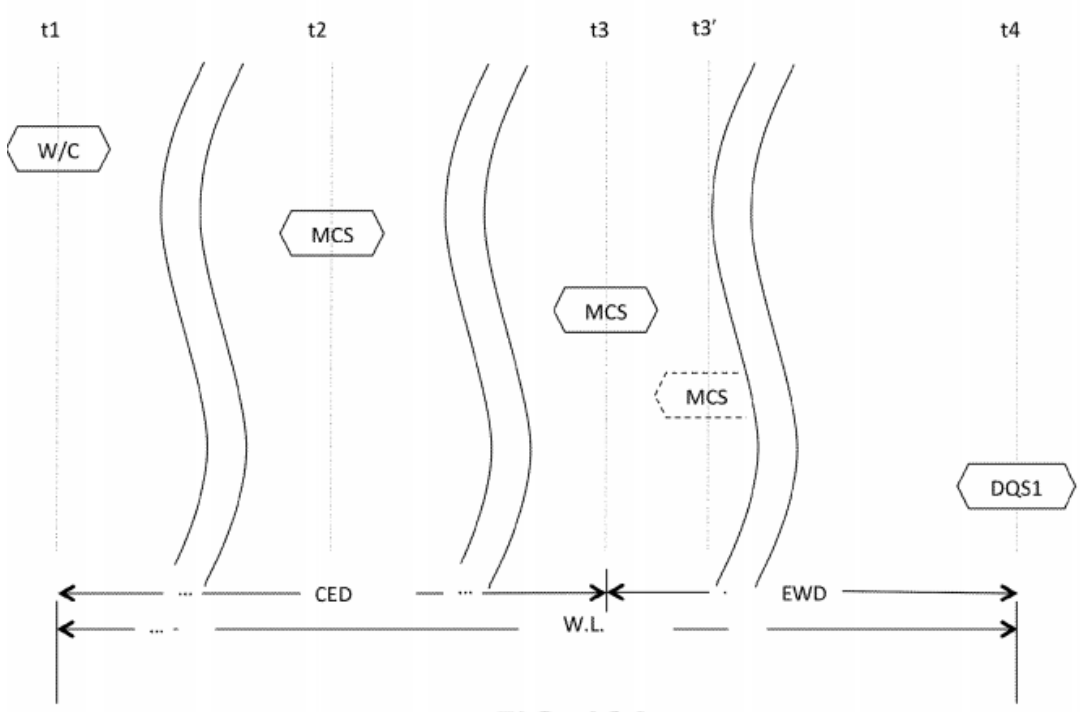

FIG. 12A

As shown in Figure 12A, in response to a write command issued at t1, module control circuit 116 issues one or more enable signals at time t2. *Id.* at 14:61–65. Those signals are received by isolation device 118 at t3, which then receives one or more strobe signals DQS at t4. *Id.* at 14:65–15:1. The one or more enable signals are received by a different isolation device 118 at t3′. *Id.* at 14:65–15:4. The time between t1 and t4 is the write latency "W.L." and is known to the isolation device 118. *Id.* at 15:4–7. The time interval between t4 and t3 (the "enable-to-write data delay" or "EWD") can be determined by isolation device 118. *Id.* at 15:7–10. Isolation device 118 can then determine the time interval between t1 and t3 (the "command-to-enable delay" or "CED"), "which can be used by the isolation device 118 to properly time transmission of read data to the MCH." *Id.* at 15:10–15.

C. Illustrative Claim

Of the challenged claims, claims 1 and 12 are independent, claims 2–5 depend from claim 1, and claims 13, 14, 19, and 20 depend from claim 12. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to the memory command signals;

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