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Paper 10
Entered: October 30, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00730
Patent 9,128,632 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE *Administrative Patent Judges.*

CLEMENTS, *Administrative Patent Judge.*

DECISION
Denying Petitioner's Request for Rehearing
37 C.F.R. § 42.71

I. INTRODUCTION

Pursuant to 37 C.F.R. § 42.71(d), SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. (collectively, "Petitioner") request rehearing of our Decision on Institution (Paper 8, "Dec."). Paper 9 ("Req. Reh'g"); Dec. 8–15 (analyzing obviousness). Specifically, Petitioner submits that we "overlooked or misapprehended the portions of the Petition explaining that the data buffers of Saito's memory modules do, in fact, utilize the timing intervals determined during read/write leveling initialization to adjust the timing of read operations during normal operations" and requests that "trial be instituted for claims 1-5, 12-14 and 19-20 of the 632 Patent over Saito and Swain (Ground 1) and claims 3 and 13-14 over Saito, Swain and Kim (Ground 2)." Req. Reh'g 1–2.

For the reasons set forth below, Petitioner's Request for Rehearing is *denied*.

II. STANDARD OF REVIEW

A party requesting rehearing bears the burden of showing that the decision should be modified. 37 C.F.R. § 42.71(d). The party must identify specifically all matters we misapprehended or overlooked, and the place where each matter was addressed previously in a motion, an opposition, or a reply. *Id.*

When rehearing a decision on a petition, we review the decision for an abuse of discretion. *See* 37 C.F.R. § 42.71(c). An abuse of discretion may be indicated if a decision is based on an erroneous interpretation of law, if a factual finding is not supported by substantial evidence, or if the decision represents an unreasonable judgment in weighing relevant factors. *See Star Fruits S.N.C. v. United States*, 393 F.3d 1277, 1281 (Fed. Cir. 2005); *Arnold*

P'ship v. Dudas, 362 F.3d 1338, 1340 (Fed. Cir. 2004); *In re Gartside*, 203 F.3d 1305, 1315–16 (Fed. Cir. 2000). With this in mind, we address the arguments presented by Petitioner.

III. ANALYSIS

A. The Explanation in the Petition

Petitioner argues that we overlooked or misapprehended the explanation in the Petition showing that Saito's data buffers time normal operations based on timing internals determined during read/write leveling initialization. Req. Reh'g 2–7. Specifically, Petitioner argues we misapprehended Saito's teaching of re-timing from CL=5 to CL=6 when we determined that it "does not explain how CL=6 was chosen." Req. Reh'g. 5–6 (quoting Dec. 12). According to Petitioner, paragraphs 101 and 138 of Saito "could not be more explicit that time intervals from the leveling operations are used to make timing adjustments during normal operation."

We disagree. Neither paragraph teaches that the re-timing from CL=5 to CL=6 is "based on signals received by the each respective buffer circuit during a memory" read or write "operation," as required by the claims. Paragraph 101 of Saito is reproduced below.

> Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner. Details on the timing adjustments will be described later.

Ex. 1005 ¶ 101. Paragraph 101 describes Figure 7. *See id.* ¶¶ 100, 101. Recognizing that the timing of signals DQ-Pre (between memory controller and data buffer 300 on connectors 120) and the timing of signals DQ-Post (between data buffer 300 and memory chips 200 on data lines L1 or L2) is "off" because "data DQ is buffered by the data register buffer 300," Saito teaches that "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner." Ex. 1005 ¶ 101. This paragraph, therefore, does not teach that re-timing from CL=5 to CL=6 is based on "time intervals from the leveling operations," as Petitioner contends. Req. Reh'g 7. To the contrary, it explicitly teaches the necessity of a "separate manner" for adjusting timing between a data buffer and memory chip (i.e., for "signals received by the each respective buffer circuit during a memory write operation," as recited in claim 1) and adjusting timing between a data buffer and a memory controller (i.e., for "transmission of a respective set of read data signals received from the respective group of memory devices," as recited in claim 1).

Paragraph 138 also does not teach that the re-timing from CL=5 to CL=6 is "based on signals received by the each respective buffer circuit during a memory" read or write "operation," as required by the claims. Paragraph 138 is reproduced below.

> Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing

> is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.

Ex. 1005 ¶ 138. As is apparent, paragraph 138 teaches performance of a write leveling operation to adjust write timing between data register buffer 300 and memory chip 200 and performance of a read leveling operation to adjust read timing between data register buffer 300 and memory chip 200. Paragraph 138 does *not* teach that any of the intervals determined during those leveling operations are subsequently used by data buffer 300 "to time transmission of a respective set of read data signals received from the respective group of memory devices" to the memory controller.

As a result, we are not persuaded that we overlooked or misapprehended any teaching in these paragraphs.

B. Other Portions of Saito Relied Upon in Our Decision

Petitioner also argues that the other portions of Saito relied upon in our Decision support its position. Req. Reh'g 7–12. Petitioner argues that (1) Saito's use of a "time A" to adjust the timing of "input buffer circuit INB and the like" teaches "tim[ing] transmission . . . of read data" as recited in the claims, (*id.* at 8–11); (2) that the "long" example of Saito supports its position (*id.* at 11–12); and (3) that leveling operations between the data buffer and the memory controller are irrelevant to consideration of the Petition (*id.* at 12–13).

These arguments were not in the Petition so we could not have misapprehended or overlooked them. To the extent that Petitioner is arguing that these paragraphs of our Decision indicate a misapprehension of what was argued in the Petition, we disagree. Specifically, we are unpersuaded by Petitioner's contention that Saito's teaching to use time A to time *reception*

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