

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON.COM, INC. and AMAZON WEB SERVICES, INC.,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

Case IPR2017-00814
Patent 6,766,389 B2

Before JAMES B. ARPIN, BARBARA A. PARVIS, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Amazon.com, Inc. and Amazon Web Services, Inc. (collectively, “Petitioner”) filed a Petition (“Pet.”) requesting *inter partes* review of claims 1–19 of U.S. Patent No. 6,766,389 B2 (“the ’389 patent,” Ex. 1001). Paper 2. Broadcom Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). Pursuant to 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

After considering the Petition, the Preliminary Response, and associated evidence, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of claims 1–3, 7, and 8. Thus, we institute an *inter partes* review as to these claims.

A. *The ’389 Patent and Illustrative Claims*

The ’389 patent is directed to a system on a chip for networking. Ex. 1001, 1:31. The ’389 patent discloses:

[A]n integrated circuit for a network device is contemplated. The integrated circuit includes at least one processor coupled to an interconnect; a cache coupled to the interconnect; a memory controller coupled to the interconnect; and one or more input/output (I/O) devices for networking applications. The at least one processor, the cache, the memory controller, the interconnect, and the one or more I/O devices are integrated onto the integrated circuit.

Moreover, an integrated circuit for a network device is contemplated, including at least one processor and an input/output (I/O) device capable of caching data. The processor and the I/O device are integrated onto the integrated circuit. Coherency is enforced between the processor and the I/O device.

Ex. 1001, 1:46–59.

Claims 1 and 7 are independent claims. Claims 2–6 depend directly or indirectly from claim 1, and claims 8–19 depend directly or indirectly from claim 7. Claims 1, 4, and 7 are illustrative and are reproduced below:

1. An integrated circuit comprising:
 - at least one processor coupled to a bus;
 - a cache memory coupled to the bus to cache data for the integrated circuit;
 - a memory controller coupled to the bus;
 - a bridge circuit coupled to the bus: and
 - at least one interface circuit to couple to a network external to the integrated circuit, the at least one interface circuit also coupled to the bridge circuit to allow the bridge circuit to initiate transactions onto the bus for data transfer between the bus and the at least one interface circuit.

4. The integrated circuit as recited in claim 2 wherein the bridge circuit to operate to maintain cache coherency for the integrated circuit.

7. In a network device, an integrated circuit containing a system thereon, comprising:
 - at least one processor coupled to a bus;
 - a cache memory coupled to the bus to cache data for the integrated circuit;
 - a memory controller coupled to the bus;

a plurality of interface circuits to couple to different networks to allow the network device to operate in more than one type of network; and

at least one bridge circuit coupled to the bus to operate as a bridge between the bus and the plurality of interface circuits to initiate transactions between the plurality of interface circuits and the bus.

B. References

Petitioner relies upon the following references:

Young	US 5,768,548	June 16, 1998	Ex. 1007
Shigeeda	US 5,778,425	July 7, 1998	Ex. 1004
“Fast Cache and Bus Power Estimation for Parameterized System-on-a-Chip Design,” T. D. Givargis, F. Vahid, J. Henkel (“Givargis”), Proceedings of Design, Automation and Test Conference and Exhibition 2000, March 27–30, 2000, ISBN 0-7695-0537-6, at pp. 333–339			Ex. 1006
“Broadcom, Cisco, Nvidia, Sun Among First Adopters of AMD’s New HyperTransport Technology,” Advanced Micro Devices, February 14, 2001 (“HT Press Release”)			Ex. 1008

C. Asserted Grounds of Unpatentability

Petitioner challenges claims 1–19 of the ’389 patent based on the asserted grounds of unpatentability set forth in the table below. Pet. 3.

Reference(s)	Basis	Claim(s) Challenged
Shigeeda	§ 102(b)	1–5, 7, 9, and 13
Shigeeda alone or in combination with Givargis	§ 103(a)	5–7, 9–11, and 13
Shigeeda and HT Press Release	§ 103(a)	8
Shigeeda, alone or in combination with Givargis, and also in combination with HT Press Release	§ 103(a)	8 and 12

Reference(s)	Basis	Claim(s) Challenged
Shigeeda, alone or in combination with Givargis, and also in combination with Young	§ 103(a)	14–18
Shigeeda, alone or in combination with Givargis, and also in combination with Young and HT Press Release	§ 103(a)	19

II. ANALYSIS

A. *Claim Construction*

In an *inter partes* review, “[a] claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears.” 37 C.F.R. § 42.100(b). In determining the broadest reasonable construction, we presume that claim terms carry their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). This presumption may be rebutted when a patentee, acting as a lexicographer, sets forth an alternate definition of a term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

The parties disagree as to the meaning of the term “Level 2 cache,” which is recited in dependent claim 3. Pet. 4; Prelim. Resp. 21–24. Based on the record and for purposes of this Decision, we determine that neither this term nor any other term in the claims of the ’389 patent requires express construction at this time.

B. *Principles of Law*

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net*

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