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Paper No. 8
Entered: August 28, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-00841
Patent 7,525,189 B2

Before MICHAEL J. FITZPATRICK, JENNIFER MEYER CHAGNON, and SHEILA F. MCSHANE, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Xilinx, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1, 2, 4, and 5 ("the challenged claims") of U.S. Patent No. 7,525,189 B2 (Ex. 1001, "the '189 patent"). Paper 1 ("Pet."). Petitioner relies on the Declaration of Jianmin Qu, Ph.D. (Ex. 1002) to support its positions. Godo Kaisha IP Bridge 1 ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

We have authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and for the reasons explained below, we determine that the information presented does not show a reasonable likelihood that Petitioner would prevail with respect to any of the challenged claims. *See* 35 U.S.C. § 314(a). Accordingly, we do not institute an *inter partes* review of the '189 patent.

A. Related Proceedings

The parties indicate that the '189 patent is the subject of the following ongoing district court proceeding: *Xilinx, Inc. v. Godo Kaisha IP Bridge 1*, Case No. 5:17-cv-00509 (N.D. Cal.). Pet. 1; Paper 4, 1. Patent Owner also indicates that three petitions for *inter partes* review have been filed for related patents: Cases IPR2017-00842, IPR2017-00843, and IPR2017-00844. Paper 4, 1.

B. The '189 Patent

The '189 patent is titled "Semiconductor Device, Wiring Board, and Manufacturing Method Thereof," and was filed as PCT application No. PCT/JP2005/009061 on May 18, 2005. Ex. 1001, at [22], [54], [86]. The

application entered the U.S. national stage as application No. 11/569,423 meeting the requirements under 35 U.S.C. § 371 on November 20, 2006. *Id.* at [21], [86]. The '189 patent claims priority to Japanese application No. 2004-152618, filed May 21, 2004. *Id.* at [30].

The embodiments described in the '189 patent "provide a highly reliable semiconductor device capable of improving the performance at a low cost." *Id.* at 4:6–8. Figure 1 of the '189 patent is reproduced below.

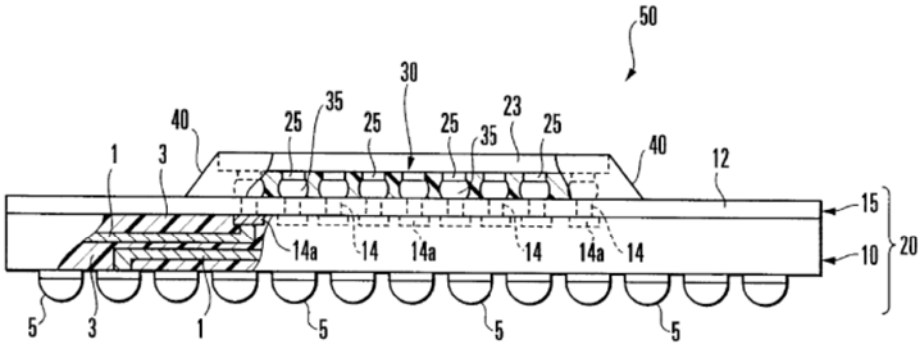

FIG. 1

Figure 1, above, illustrates a "partially cutaway side view schematically showing the first embodiment[] of a semiconductor device and wiring board of the present invention." *Id.* at 4:14–16. As seen in Figure 1, semiconductor device 50 includes semiconductor chip 30 mounted on wiring board 20 by flip chip bonding. *Id.* at 4:58–62. Wiring board 20 includes first wiring portion 10, and second wiring portion 15 electrically connected to and integrated with (i.e., stacked on) first wiring portion 10. *Id.* at 4:63–5:1.

First wiring portion 10 further includes a plurality of wiring layers 1 and interlayer dielectric films 3. *Id.* at 5:1–4. "[E]xternal connecting bumps 5 are formed [on] one surface . . . of the first wiring portion." *Id.* at

5:5–6. Second wiring portion 15 includes base 12 and connecting terminals 14 (each formed of a contact plug formed in a through hole) extending through the base. *Id.* at 5:9–17. In embodiments of the '189 patent, the "planar size of the second wiring portion 15 is equal to that of the first wiring portion 10." *Id.* at 5:22–24.

As further described, "the material of the base 12 of the second wiring portion 15 is selected so that the thermal expansion coefficient of the second wiring portion 15 is smaller than that of the first wiring portion 10, and equal to that of each semiconductor chip 30." *Id.* at 5:49–52. Having the thermal expansion coefficient of the second wiring portion 15 be equal to that of each semiconductor chip 30 makes it possible to suppress the internal stress caused by differences in the thermal expansion coefficients. *Id.* at 6:1–6.

C. Illustrative Claim

Of the challenged claims, claims 1 and 4 are independent. Claims 2 and 5 depend from claims 1 and 4, respectively. Independent claim 1 of the '189 patent is reproduced below, and is illustrative of the challenged claims.

> 1. A semiconductor device characterized by comprising:
>
> a wiring board comprising a plurality of connecting terminals arranged on one surface in a direction of thickness and a plurality of external connecting bumps arranged on the other surface in the direction of thickness; and
>
> at least one semiconductor chip connected to said connecting terminals,
>
> wherein said wiring board comprises:
>
> a first wiring portion comprising a plurality of wiring layers and said external connecting bumps; and

> a second wiring portion electrically connected to said first wiring portion and integrated with said first wiring portion in the direction of thickness,
>
> said connecting terminals are made of contact plugs formed in through holes extending through the second wiring portion in the direction of thickness,
>
> sizes of opposing surfaces of said first wiring portion and said second wiring portion are equal,
>
> a thermal expansion coefficient of said second wiring portion is smaller than a thermal expansion coefficient of said first wiring portion and equal to a thermal expansion coefficient of said semiconductor chip,
>
> said semiconductor chip is a silicon chip,
>
> said second wiring portion comprises a base made of silicon, and
>
> said contact plugs are formed in said base.

Ex. 1001, 14:49–15:8.

D. The Applied References

Petitioner relies on the following references in the asserted grounds.

Pet. 19–20.

Reference	**Date**	**Exhibit**
U.S. Patent Appl. Pub. No. 2002/0180015 A1 (“Yamaguchi”)	Dec. 5, 2002	Ex. 1004
U.S. Patent No. 5,258,648 (“Lin”)	Nov. 2, 1993	Ex. 1005
U.S. Patent No. 6,617,681 B1 (“Bohr”)	Sept. 9, 2003	Ex. 1006

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