

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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IPR2017-00844  
Patent 6,653,731 B2

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Before MICHAEL J. FITZPATRICK, JENNIFER MEYER CHAGNON,  
and SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

DECISION  
Instituting *Inter Partes* Review  
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

## I. INTRODUCTION

### A. Background

Xilinx, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claim 5 (“the challenged claim”) of U.S. Patent No. 6,653,731 B2 (Ex. 1001, “the ’731 patent”) pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Godo Kaisha IP Bridge 1 (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”).

We have authority under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the Petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” *See* 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”).

We determine that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail with respect to the one challenged claim. For the reasons described below, we institute an *inter partes* review of claim 5 of the ’731 patent.

### B. Related Proceedings

The parties indicate that a related matter is: *Xilinx, Inc. v. Godo Kaisha IP Bridge 1*, Civ. No. 5:17-cv-00509 (N.D. Cal.). Pet. 1, Paper 4, 1. Patent Owner also indicates that three petitions for *inter partes* review have been filed for related patents: Cases IPR2017-00841, IPR2017-00842, and IPR2017-00843. Paper 4, 1.

### C. The ’731 Patent

The ’731 patent is entitled “Semiconductor Device And Method For Fabricating Same,” and issued on November 25, 2003, from an application

filed on February 15, 2001. Ex. 1001, [22], [45], [54]. The '731 patent claims foreign priority to application JP 2000-051873, dated February 28, 2000. *Id.* at [30].

The '731 patent is directed to a semiconductor device in which a chip with bumps, and having a protective resin, is provided. Ex. 1001, Abstract. The bare chip is coated with protective resin in order to prevent it from being cracked. *Id.* at 1:7–11. A semiconductor device, such as a large-scale integration (LSI) chip 101, is reproduced in Figure 1 below.

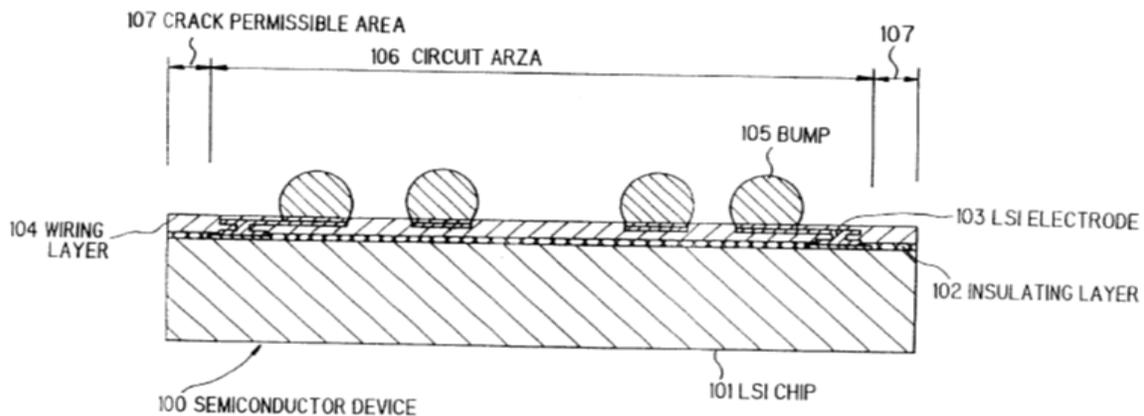


Figure 1, above, show a conventional bare chip. Ex. 1001, 1:20–21.

Insulating layer 102 is provided on the surface of LSI chip 101, with wiring layer 104 with LSI electrodes 103. *Id.* at 1:22–24. Plural bumps 105 are mounted on the leading ends of LSI electrodes 103, and serve as external electrodes. *Id.* at 1:24–27. Figure 4A, reproduced below, shows a cross-sectional view of a chip with resin.

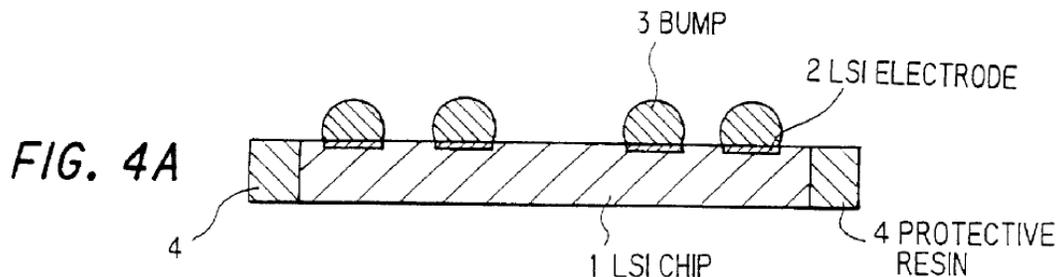


Figure 4A, above, depicts protective resin 4 coating the sides of LSI chip 1. Ex. 1001, 4:48–51. Testing of chip reliability of a chip such as that shown in Figure 4A was performed “supposing a condition that the semiconductor devices are packed up and transported,” where “[t]he permissible width of the semiconductor device shown in FIG. 4A is defined as the sum of 25  $\mu\text{m}$  and the thickness of protective resin 4.” *Id.* at 10:29–40. Figure 12, reproduced below, shows the relationship “between the permissible widths of the semiconductor devices and percent de[f]ectives of the semiconductor devices” (*id.* at 10:49–51):

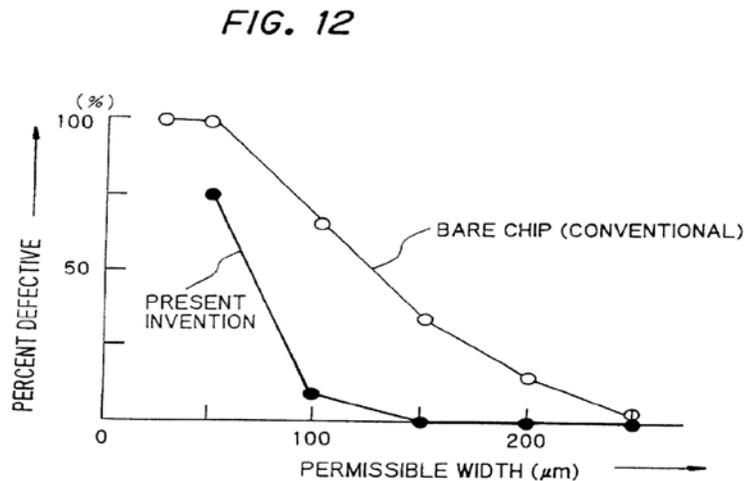


Figure 12, above, depicts, in black circles, data of semiconductor devices such as that shown in Figure 4A, and the white circles show test data of the conventional semiconductor device such as that shown in Figure 1. Ex. 1001, 10:51–55. The data indicates that the defective percentages of the semiconductor device shown in Figure 4A decreases as the permissible width increases, and when the permissible width is more than 100  $\mu\text{m}$ , the effect is a noticeable improvement in mechanical reliability as compared to a conventional semiconductor device with the same dimensions. *Id.* at 10:55–65.

Claim 5, reproduced below, is the only challenged claim of the '731 patent.

5. A semiconductor device, comprising:

a bare chip;

plural bumps provided on an active surface of said bare chip;

and

protective members formed on side surfaces of said bare chip to surround a periphery of said bare chip,

wherein a sum of a thickness of each of said protective members and a width of said bare chip is more than 100  $\mu\text{m}$ .

Ex. 1001, 12:55–64.

#### *D. Asserted Grounds of Unpatentability*

Petitioner asserts the following grounds of unpatentability against claim 5 of the '731 patent:

Ground	Prior Art
§ 102	Yoshikazu <sup>1</sup>
§ 103	Yoshikazu and Ohta <sup>2</sup>
§ 102	Ohta
§ 102	Lau <sup>3</sup>

Pet. 29–30.

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<sup>1</sup> U.S. Patent No. 5,989,982 (issued November 23, 1999) (Ex. 1005). Petitioner asserts that Yoshikazu is prior art to the '731 patent under 35 U.S.C. § 102(e). Pet. 29.

<sup>2</sup> U.S. Patent No. 6,228,688 B1 (issued May 8, 2001) (Ex. 1006). Petitioner asserts that Ohta is prior art to the '731 patent under 35 U.S.C. § 102(e). Pet. 29.

<sup>3</sup> FLIP CHIP TECHNOLOGIES (John H. Lau ed., McGraw-Hill 1996) (Ex. 1007). Petitioner asserts that Lau is prior art to the '731 patent under 35 U.S.C. §§ 102(a) and 102(b). Pet. 30.

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