

JASON D. EISENBERG
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May 24, 2013

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. To be assigned; Filed: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Payment made via EFS-Web for \$6080.00 to cover:
\$3,040.00 Patent Application fee (including basic filing, search, and examination fees);
\$3040.00 Excess claims fee; and
2. Reissue Patent Application Transmittal Form (PTO/AIA/50);
3. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);
4. Preliminary Amendment in a Reissue Application Under 37 C.F.R. § 1.173(b) and Statement of Status and Support for all Changes to the Claims Under 37 C.F.R. § 1.173(c);
5. A copy of an original Reissue Application: Consent of Assignee; Statement of Non-Assignment;
6. A copy of an original executed Power of Attorney by Applicant; and
7. Statement Under 37 C.F.R. § 3.73(c);
8. U.S. Narrowing Reissue Application entitled:

Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Commissioner for Patents
May 24, 2013
Page 2

and naming as inventor:

Kimmo MYLLY

the application consisting of:

- a. An Application Data Sheet (37 C.F.R. § 1.76);
- b. Reissue Application Declaration by the Assignee Form (PTO/AIA/06);
- c. the application consisting of:
 - i. Reissue Application Cover Sheet with Abstract;
 - ii. A specification and claims in double column copy of patent format consisting of a total of seven (7) pages; and
 - iii. Four (4) sheets of drawings (Figures 1-4).

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided via EFS-Web. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/lvt
Enclosure(s)

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

REISSUE PATENT APPLICATION TRANSMITTAL

Address to: Mail Stop Reissue Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Attorney Docket No.	3371.002RE10
	First Named Inventor	Kimmo MYLLY
	Original Patent Number	7,278,033
	Original Patent Issue Date (Month/Day/Year)	October 2, 2007
	Express Mail Label No.	

APPLICATION FOR REISSUE OF:

(Check applicable box)

 Utility Patent Design Patent Plant Patent**APPLICATION ELEMENTS (37 CFR 1.173)**

1. Fee Transmittal Form (PTO/SB/56)
2. Applicant asserts small entity status. See 37 CFR 1.27
3. Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. Specification and Claims in double column copy of patent format (amended, if appropriate)
5. Drawing(s) (proposed amendments, if appropriate)
6. Reissue Oath/Declaration or Substitute Statement (37 CFR 1.175) (PTO/AIA/05, 06, or 07)
7. Application Data Sheet **NOTE:** Benefit claims under 37 CFR 1.78 and foreign priority claims under 37 CFR 1.55 MUST be set forth in an Application Data Sheet (ADS).
8. Original U.S. Patent currently assigned? Yes No
(If Yes, check applicable box(es))
 - Written Consent of all Assignees (PTO/AIA/53)
 - 37 CFR 3.73(c) Statement (PTO/AIA/96)
9. CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
 - Landscape Table on CD
10. **Nucleotide and/or Amino Acid Sequence Submission** (if applicable, items a. - c. are required)
 - a. Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. CD-ROM (2 copies) or CD-R (2 copies); or
 - ii. Paper
 - c. Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

11. Statement of status and support for all changes to the claims. See 37 CFR 1.173(c).
12. Power of Attorney
13. Information Disclosure Statement (IDS)
PTOSB/08 or PTO-1449
 Copies of citations attached
14. English translation of Reissue Oath/Declaration (if applicable)
16. Return Receipt Postcard (MPEP § 503) (Should be specifically itemized)
17. Other: Preliminary Amendment in a Reissue Application Under 37 C.F.R. § 1.173(b), and

Authorization to Treat a Reply as Incorporating
an Extension of Time Under 37 C.F.R. 1.136(a)(3).

This is a continuation reissue or divisional reissue application (i.e., a second or subsequent reissue application for the same issued patent). (Check box if applicable.)

18. CORRESPONDENCE ADDRESS

The address associated with Customer Number: 26111 OR Correspondence address below

Name			
Address			
City	State	Zip Code	
Country	Telephone		
Email			
Signature	Date	5/24/13	
Name (Print/Type)	Registration No.	43,447	

This collection of information is required by 37 CFR 1.173. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Reissue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: To be assigned

(*Narrowing Reissue of U.S. Patent No. 7,278,033;
Issued October 2, 2007*)

**For: Method and a System for Determining the
Power Consumption in Connection with an
Electronic Device, and an Electronic Device**

Confirmation No.: To be assigned

Art Unit: To be assigned

Examiner: To be assigned

Atty. Docket: 3371.002REI0

**Authorization to Treat a Reply as Incorporating an
Extension of Time Under 37 C.F.R. § 1.136(a)(3)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

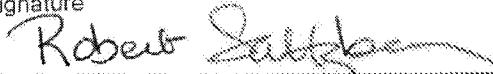
Date: _____

5/29/13

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

1691387_1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT		Docket Number (Optional) 3371.002RE10
This is part of the application for a reissue patent based on the original patent identified below.		
Name of Patentee(s) Memory Technologies LLC		
Patent Number 7,278,033 B2	Date Patent Issued October 2, 2007	
Title of Invention Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device		
<p>1. <input checked="" type="checkbox"/> Filed herein is a statement under 37 CFR 3.73(c). (Form PTO/AIA/96)</p> <p>2. <input type="checkbox"/> Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.</p> <p>One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee."</p> <p>The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.</p>		
The assignee(s) owning an undivided interest in said original patent is/are <u>Memory Technologies LLC</u> and the assignee(s) consents to the accompanying application for reissue.		
Name of assignee/inventor (if not assigned) Memory Technologies LLC		
Signature 	Date May 23, 2013	
Typed or printed name and title of person signing (if assignee (if assigned)) Robert Saltzberg Authorized Representative		

This collection of information is required by 37 CFR 1.172. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

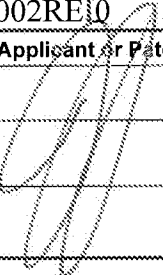
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	To be assigned
Filing Date	Herewith
First Named Inventor	Kimmo MYLLY
Title	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
Art Unit	To be assigned
Examiner Name	To be assigned
Attorney Docket Number	3371.002RE10

SIGNATURE of Applicant or Patent Practitioner

Signature		Date	5/29/13
Name	Jason D. Eisenberg	Telephone	(202) 772-8645
Registration Number	43,447		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/B2A or equivalent):

26111

OR

I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/B2A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

The address associated with the above-mentioned Customer Number

OR

The address associated with Customer Number:

26111

OR

Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant:

Inventor or Joint Inventor

Legal Representative of a Deceased or Legally Incapacitated Inventor

Assignee or Person to Whom the Inventor is Under an Obligation to Assign

Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature	<i>Robert Salzman</i>	Date	May 23, 2013
Name	<i>Robert Salzman</i>	Telephone	
Title and Company	<i>Attorney and Representative</i> Memory Technologies LLC		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below.

*Total of _____ forms are submitted

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

Atty. Docket No. 3371.002REIU

Applicant/Patent Owner: Kimmo Mylly
 Application No./Patent No.: To be assigned Filed/Issue Date: Herewith
 Titled: Method and a System for Determining the Power Consumption in Connecting with an Electronic Device, and an Electronic Device
Memory Technologies LLC a corporation
 (Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. The assignee of the entire right, title, and interest.
2. An assignee of less than the entire right, title, and interest (check applicable box):
- The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Kimmo Mylly To: Nokia Corporation

The document was recorded in the United States Patent and Trademark Office at
 Reel 013928, Frame 0450, or for which a copy thereof is attached.

2. From: Nokia Corporation To: Nokia Inc.

The document was recorded in the United States Patent and Trademark Office at
 Reel 030189, Frame 0381, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: Nokia Inc. To: Memory Technologies LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 030190, Frame 0043, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet(s).

As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Robert Saltzberg
Signature

May 23, 2013
Date

Robert Saltzberg (Authorized Representative)
Printed or Typed Name Title or Registration Number

REISSUE APPLICATION DECLARATION BY THE ASSIGNEE		Docket Number (optional) 3371.002RE10	
I hereby declare that: The residence and mailing address of the inventor or joint inventors are stated below. I am authorized to act on behalf of the following assignee: <u>Memory Technologies LLC</u> The entire title to the patent identified below is vested in said assignee.			
Inventor: <u>Kimmo MYLLY</u>			
Residence: City <u>Julkujärvi</u>	State	Country <u>Finland</u>	
Mailing Address <u>Niemenkuja 8 A</u>			
City <u>Julkujärvi</u>	State	Zip <u>FIN-39160</u>	Country <u>Finland</u>
<input type="checkbox"/> Additional Inventors are named on separately numbered sheets attached hereto.			
Patent Number <u>7,278,033 B2</u>		Date of Patent Issued <u>October 2, 2007</u>	
I believe said inventor(s) to be the original inventor or original joint inventors of the subject matter which is described and claimed in said patent, for which a reissue patent is sought on the invention titled:			
<u>Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device</u>			
the specification of which			
<input checked="" type="checkbox"/> is attached hereto.			
<input type="checkbox"/> was filed on _____ as reissue application number _____.			
The above-identified application was made or authorized to be made by me.			
I hereby acknowledge that any willful false statement in this reissue declaration is punishable under 35 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.			
I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)			
<input type="checkbox"/> by reason of a defective specification or drawing.			
<input checked="" type="checkbox"/> by reason of the patentee claiming more or less than he had the right to claim in the patent.			
<input type="checkbox"/> by reason of other errors.			

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 422 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE

Docket Number (Optional)
 3371.002RE10

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified and the box below must be checked:

Applicant seeks to clarify claim 28 by additionally reciting: "wherein the means for setting the maximum power consumption includes a processor configured to read an indication of the value from the received information and to set the maximum power consumption to the value based on the indication."

[Attach additional sheets, if needed.]

The application for the original patent was filed under 37 CFR 1.46 by the assignee of the entire interest.

I hereby appoint:

Practitioners associated with Customer Number

26111

OR

Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Correspondence Address: Direct all communications about the application to:

The address associated with Customer Number:

26111

OR

<input type="checkbox"/> Firm or Individual Name			
Address			
City	State		Zip
Country			
Telephone		Email	

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR § 2.13(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature *Robert Saltzberg*

Date (Optional) *May 23, 2013*

Full name of person signing (given name, family name)
Robert Saltzberg

Address of Assignee
 6787 W. Tropicana Ave., Suite 238, Las Vegas, Nevada 89103, US

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	3371.002RE10
		Application Number	
Title of Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to <input type="checkbox"/> 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)	
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Inventor Information:

Inventor 1 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Kimmo		MYLLY	
Residence Information (Select One) <input type="radio"/> US Residency <input checked="" type="radio"/> Non US Residency <input type="radio"/> Active US Military Service				
City	Julkujärvi	Country of Residence ⁱ	FI	
Mailing Address of Inventor:				
Address 1		Niemenkuja 8 A		
Address 2				
City	Julkujärvi	State/Province		
Postal Code	FIN-39160	Country ⁱ	FI	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
<input type="checkbox"/> An Address is being provided for the correspondence information of this application.	
Customer Number	26111
Email Address	Add Email Remove Email

Application Information:

Title of the Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device		
Attorney Docket Number	3371.002RE10	Small Entity Status Claimed	<input type="checkbox"/>
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3371.002RE10
	Application Number	
Title of Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device	

Publication Information:

<input type="checkbox"/>	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
<input type="checkbox"/>	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
	reissued of	10401338	2003-03-26	7278033	2007-10-02

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Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)
20020594	FI	2002-03-27	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3371.002RE10
	Application Number	
Title of Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3371.002RE10
	Application Number	
Title of Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device	

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Assignee Legal Representative under 35 U.S.C. 117 Joint Inventor

Person to whom the inventor is obligated to assign. Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3371.002REI0
	Application Number	
Title of Invention	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device	

Prefix	Given Name	Middle Name	Family Name	Suffix

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Address 2			
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Signature		Date (YYYY-MM-DD)	2013-05-24
First Name	Jason	Last Name	Eisenberg
Registration Number		43447	
Additional Signature may be generated within this form by selecting the Add button.			

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BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application for Broadening Reissue of:

Kimmo MYLLY

U.S. Patent No. 7,278,033

Date of Patent: October 2, 2007

Title: Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Atty. Docket No. 3371.002REI0

ABSTRACT

The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Signaling between the electronic device and the peripheral device sets a maximum value for the power consumption of the peripheral device which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied.



US007278033B2

(12) **United States Patent**
Mylly

(10) **Patent No.:** **US 7,278,033 B2**
(45) **Date of Patent:** **Oct. 2, 2007**

(54) **METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE**

(75) **Inventor:** **Kimmo Mylly, Tampere (FI)**

(73) **Assignee:** **Nokia Corporation, Espoo (FI)**

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 472 days.

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(21) **Appl. No.:** **10/401,338**

(22) **Filed:** **Mar. 26, 2003**

(65) **Prior Publication Data**
US 2003/0188205 A1 Oct. 2, 2003

(30) **Foreign Application Priority Data**
Mar. 27, 2002 (FI) 20020594

(51) **Int. Cl.**
G06F 1/00 (2006.01)
G06F 1/26 (2006.01)
G06F 1/32 (2006.01)

(52) **U.S. Cl.** 713/300; 713/320; 713/322

(58) **Field of Classification Search** 713/300, 713/320, 322

See application file for complete search history.

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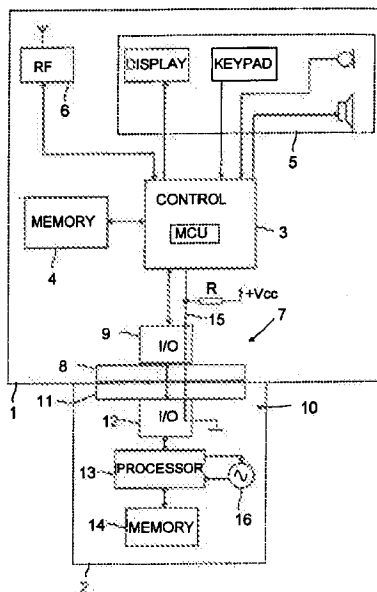
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Primary Examiner—Chun Cao
Assistant Examiner—Ji H Bae

(57) **ABSTRACT**

The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Signaling between the electronic device and the peripheral device sets a maximum value for the power consumption of the peripheral device which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied.

29 Claims, 4 Drawing Sheets



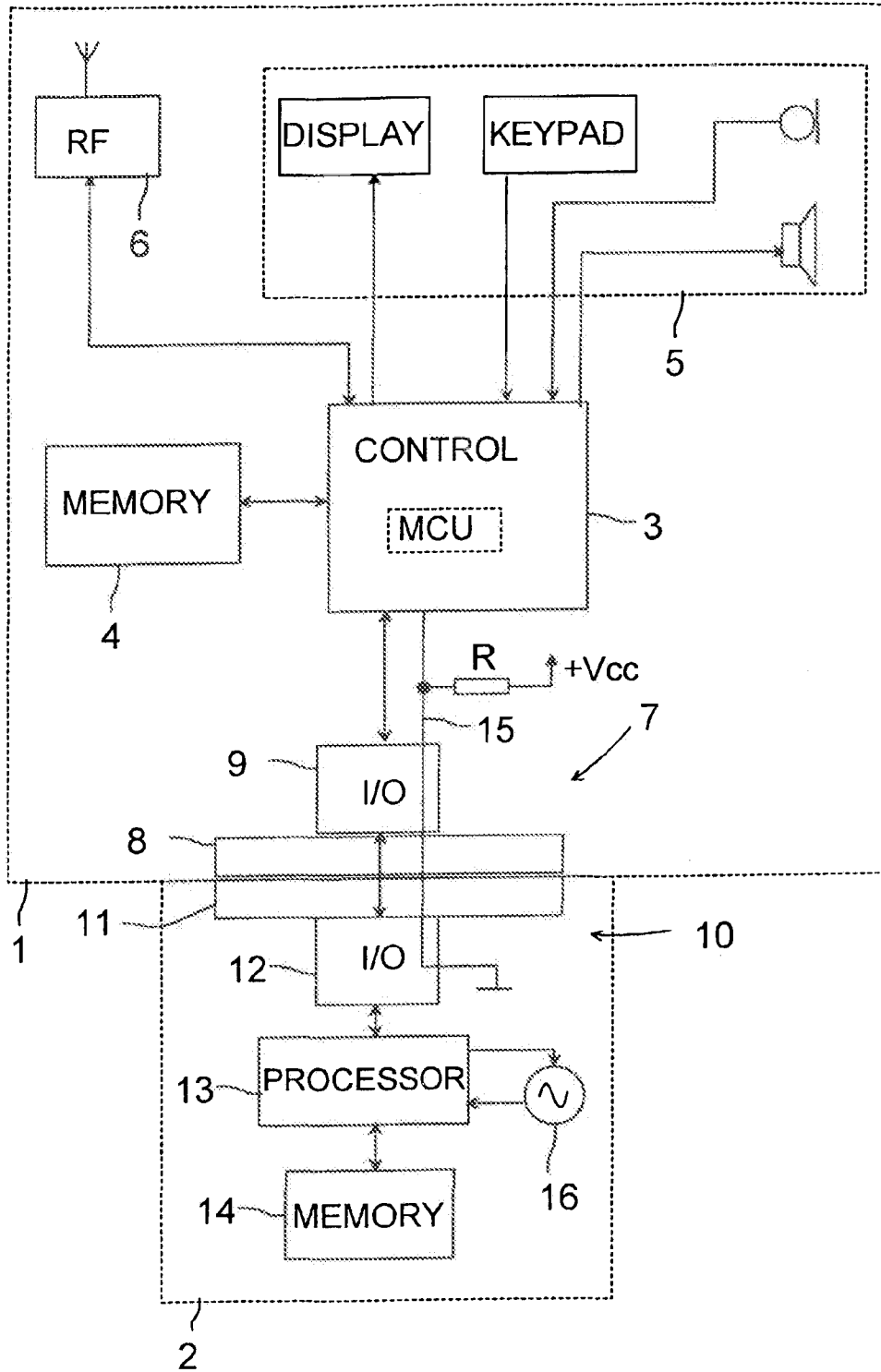


Fig 1

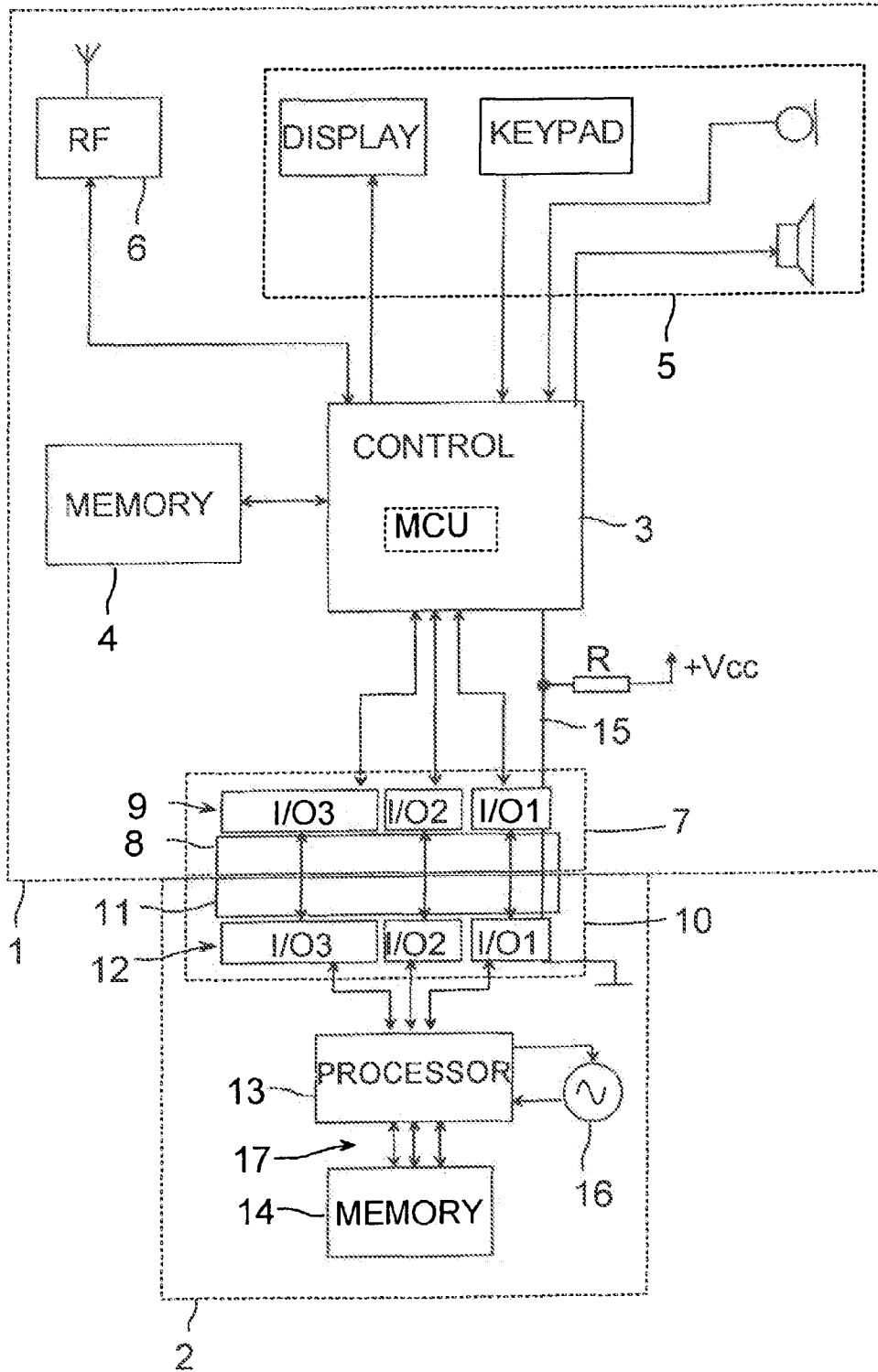


Fig 2

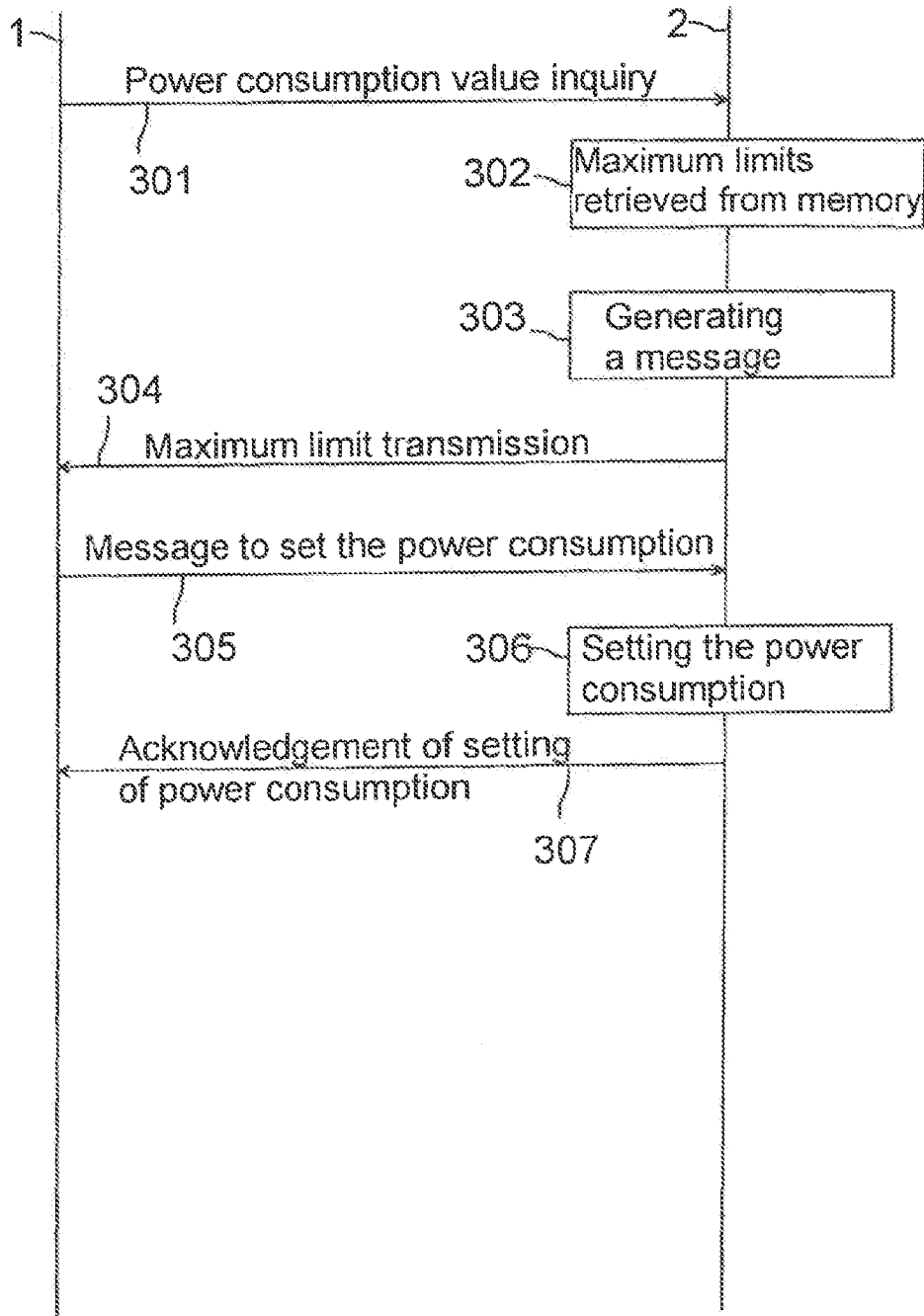


Fig 3

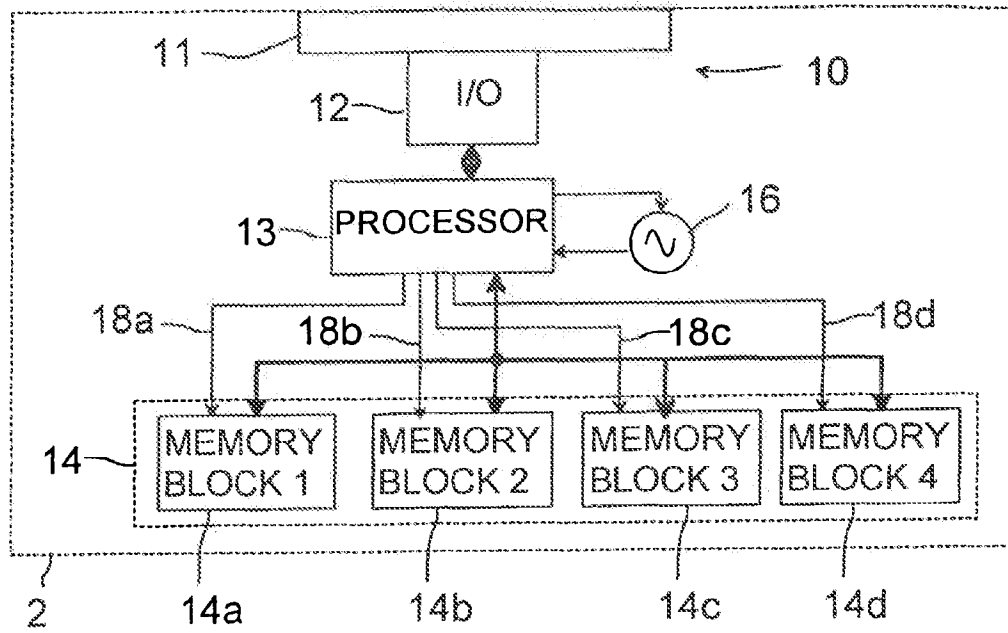


Fig 4

1

METHOD AND A SYSTEM FOR
 DETERMINING THE POWER
 CONSUMPTION IN CONNECTION WITH AN
 ELECTRONIC DEVICE, AND AN
 ELECTRONIC DEVICE

CROSS-REFERENCE TO RELATED
 APPLICATIONS

This application claims priority under 35 USC §119 to 10
 Finnish Patent Application No. 20020594 filed on Mar. 27,
 2002.

FIELD OF THE INVENTION

The present invention relates to a method for determining 15
 the power consumption in an electronic device, to which a
 peripheral device is connected, which is supplied with
 power from the electronic device. The invention also relates
 to a system which comprises an electronic device provided 20
 with means for connecting a peripheral device and means for
 supplying power to the peripheral device, and which system
 comprises means for determining the power consumption.
 Furthermore, the invention relates to an electronic device
 provided with means for connecting a peripheral device, 25
 means for supplying power to the peripheral device, and
 means for determining the power consumption of the periph-
 eral device. Moreover, the invention relates to a peripheral
 device provided with means for connecting the peripheral
 device to an electronic device, from which the power needed 30
 for using the peripheral device is arranged to be supplied to
 the peripheral device.

BACKGROUND OF THE INVENTION

At present, several such electronic devices are in use, to 35
 which it is possible to connect various peripheral devices,
 e.g. to expand the properties of the electronic device and to
 produce auxiliary functions. For example, it is possible to
 connect peripheral devices, such as connection cards (e.g. 40
 PCMCIA cards), to laptop computers to connect the laptop
 computer to a local area network, a landline or wireless
 telephone network, etc. Furthermore, peripheral devices can
 be used to expand the memory of the laptop computer, to 45
 connect an external fixed disk, a CDROM station, or the
 like.

The MultiMediaCard™ Association is, among other 50
 things, developing a standard for memory expansion boards
 (MultiMediaCard™; MultiMediaCard™ is a trademark of
 Infineon Technologies AG). These memory expansion
 boards can be used in various portable electronic devices,
 such as wireless communication devices and communicator
 type devices, to expand the memory capacity.

Because the peripheral devices can be connected to a 55
 variety of devices, the power consumption of the peripheral
 device should not exceed the maximum power that can be
 supplied from the electronic device to the peripheral device.
 Otherwise, the operation of the peripheral device and/or the
 electronic device may be disturbed and the electronic device 60
 may even be overheated. On the other hand, the power
 consumption requirements of different peripheral devices
 may be very different, wherein manufacturers of electronic
 devices should provide for the maximum power consump-
 tion in the power supply of the peripheral device connection.
 Solutions are known, such as Nokia Communicator 9110/ 65
 9210, in which the power supply of the peripheral device
 connection of the electronic device is provided with a

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relatively efficient regulator, for example in the order of 150
 mA/3 V. Such an efficient regulator is a relatively bulky
 component, which may cause placement problems, particu-
 larly in portable electronic devices. The provision for the
 maximum power consumption will be unnecessary in such 5
 electronic devices, whose users do not use, in connection
 with the electronic device, such a peripheral device whose
 power consumption is close to the maximum power con-
 sumption of the peripheral device designed for the electronic
 device. On the other hand, another user of a similar elec-
 tronic device may use such a peripheral device whose power
 consumption is in the order of the maximum power con-
 sumption of the peripheral device designed for the electronic
 device.

In some electronic devices and peripheral devices to be 15
 connected to them, the operating voltage is selected at the
 stage when the peripheral device is turned on, e.g. when the
 electronic device is turned on or when the peripheral device
 is connected. Thus, signalling will be performed between the
 electronic device and the peripheral device, for the elec-
 tronic device to determine the level of the operating voltage
 required by the peripheral device and to select an operating
 voltage suitable for the peripheral device to the operating
 voltage line(s) of the peripheral device.

In said MultiMediaCard Association, a maximum limit 25
 has been proposed for the power consumption of memory
 cards of the MultiMediaCard™ type. Thus, in electronic
 devices supporting this standard, the provision is made to
 supply a defined maximum power to the peripheral device.
 Moreover, the power consumption of memory cards of the 30
 MultiMediaCard™ type should thus not exceed the defined
 maximum limit. Such an arrangement is difficult, for
 example, for the reason that the power consumption of new
 memory cards to be developed is limited to this maximum
 value, wherein it may be an impediment for the implemen- 35
 tation of such memory cards whose power consumption
 cannot be made smaller than the selected maximum limit. If
 the maximum limit is set so high that the power consumption
 of other memory cards to be developed later on is also very
 likely to be smaller than this, it will mean that relatively
 efficient and large regulators must be used in electronic
 devices, perhaps unnecessarily.

The power consumption of the peripheral device is nor- 40
 mally proportional to the clock frequency used in the
 peripheral device, wherein an increase in the clock fre-
 quency will increase the power consumption. In a corre-
 sponding manner, to decrease the power consumption, the
 clock frequency of the peripheral device can be decreased,
 if this is possible in view of the other functions of the
 peripheral device. However, the operating rate of the periph- 45
 eral device will thus decrease, which is not necessarily
 desirable. Also, the bus width used in the peripheral device
 has an effect on how much power is consumed in the
 peripheral device.

SUMMARY OF THE INVENTION

It is an aim of the present invention to provide an 50
 improved method and system for determining the power
 consumption to be suitable in each situation. It is another
 aim of the invention to provide an electronic device and a
 peripheral device for applying the method. The invention is
 based on the idea of determining at least a first and a second
 maximum value for the power consumption, wherein the
 electronic device and the peripheral device set the power
 consumption to a value between these first and second
 maximum values. Thus, in different operating situations, for 55

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example the peripheral device can adjust its power consumption to be suitable for the situation. The method according to the present invention is primarily characterized in determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and setting, between the electronic device and the peripheral device, the maximum for the power consumption of the peripheral device to a value which is substantially between said first and second maximum values. The system according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. The electronic device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value. Furthermore, the peripheral device according to the invention is primarily characterized in that at least a first maximum value and a second maximum value which is higher than the first maximum value, are defined for the power consumption, and that the means for determining the power consumption comprise means for setting the maximum for the power consumption of the peripheral device to a value which is between said first maximum value and said second maximum value.

The present invention shows remarkable advantages over solutions of prior art. By the method according to the invention, it is possible to avoid the use of an unnecessarily large regulator in an electronic device, which saves costs, and wherein the size of the electronic device can, in some cases, be reduced and, on the other hand, problems of heating caused by high power consumption can be avoided. Also the power consumption can be reduced, which is advantageous particularly in portable devices. By means of the invention, the peripheral device connection can also be provided with flexibility, because the power consumption of the peripheral device can be adjusted and set to a value suitable for each situation of use. Also, the clock frequency and bus width of the peripheral device can be changed in the system according to an advantageous embodiment of the invention. Furthermore, the invention makes it possible that new peripheral devices to be developed will function in connection with electronic devices made earlier, and existing peripheral devices will function in connection with new electronic devices to be developed. With the solution according to the invention, it is also possible to achieve an improvement in the user-friendliness of the electronic device, for example, in a situation in which the peripheral device cannot fully operate on a lower level of power consumption but it can, however, inform the electronic device about this. Thus, the electronic device can take care of the shutdown (turning off) of the peripheral device in the appropriate way and notify the user of this.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, the invention will be described in more detail with reference to the appended drawings, in which

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FIG. 1 shows the system according to a preferred embodiment of the invention in a simplified block diagram,

FIG. 2 shows a system according to a second preferred embodiment of the invention in a simplified block diagram,

FIG. 3 shows signalling in the method according to a preferred embodiment of the invention in a simplified manner, and

FIG. 4 shows a peripheral device according to yet another preferred embodiment of the invention in a simplified block diagram.

DETAILED DESCRIPTION OF THE INVENTION

In the system according to an advantageous embodiment of the invention, shown in FIG. 1, the electronic device 1 is exemplified by a wireless communication device. In this example, the peripheral device 2 is a memory card, such as a memory card complying with the MultiMediaCard™ standard. However, it will be evident that the present invention is not limited solely to such electronic devices and peripheral devices, but the invention can also be applied in connection with other electronic devices and peripheral devices. The peripheral device 2 can be, for example, an interface card or also another device. The electronic device 1 contains a control block 3 comprising one or more processors, such as a micro controller unit (MCU). Furthermore, the electronic device 1 comprises a memory 4, a user interface 5 and means 6 for performing mobile station functions, such as GSM and/or UMTS mobile communication means. The user interface 5 preferably comprises a display, a keypad and audio means in a way known as such. For the connection of the peripheral device 2, the electronic device 1 is provided with connecting means 7 which comprise at least one connector 8 as well as the necessary I/O blocks 9, for example to connect the buses of the peripheral device 2 and the electronic device 1 to each other.

The peripheral device is also provided with corresponding connecting means 10 for connecting the peripheral device 2 to the electronic device 1. The connecting means 10 of the peripheral device comprise at least one connector 11 which can be connected to the connector 8 of the electronic device 1, and an I/O block 12. The power supply to the peripheral device 2 is arranged from the electronic device 1 via the connectors 8, 11. The I/O blocks are used for communication between the electronic device 1 and the peripheral device 2. This can take place as parallel data transmission or serial data transmission. For example, said peripheral device according to the MultiMediaCard™ specifications applies serial data transmission. However, in view of the present invention, which format is used for the data transmission between the electronic device 1 and the peripheral device 2 is not significant.

The peripheral device 2 also comprises a processor 13 or the like for controlling the functions of the peripheral device 2. Furthermore, the peripheral device comprises a memory 14, such as a read/write memory (RAM), e.g. for the storage of data, as well as a read-only memory (ROM, NVRAM) for the storage of the program code. The processor is responsible, for example, for controlling the I/O blocks in the data transmission between the peripheral device 2 and the electronic device 1. At least a first maximum value and a second maximum value for power consumption, which are used in the method according to the present invention, are also stored in the memory 14 of the peripheral device. Furthermore, the peripheral device comprises means for generating

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one or more clock signals required for the operation of the processor, such as a clock generator 16.

The following is a description of the operation of the method according to a preferred embodiment of the invention in a system shown in FIG. 1. For example, information on whether a peripheral device 2 is placed in the connector 8 of the connecting means of the electronic device, is transmitted via the I/O blocks to the electronic device 1. This can be implemented, for example, by providing the I/O block 9, 12 with a detection line 15 whose state is changed when the peripheral device 2 is placed in the connector 8. In this advantageous embodiment of the invention, the detection line 15 is implemented so that the detection line 15 is set in the logical 1 state by means of a pull-up resistance R in the electronic device 1. In the system of FIG. 1, the change of state is achieved in such a way that the peripheral device 2 grounds the detection line 15, wherein the state of the detection line 15 is changed to the logical 0 state. This change of state is detected in the electronic device 1, for example, in such a way that the change of state causes an interrupt in the control block 3, wherein a corresponding interrupt service program is run and the running of the initializing functions of the peripheral device are started. After the operating voltages have been coupled to the peripheral device, the processor 13 of the peripheral device 2 will start to run its own initializing operations. For example, the power consumption of the peripheral device 2 is set to a default value which, in this advantageous embodiment, is a power consumption value according to the first maximum limit. In this context, it is assumed that the first maximum limit is lower than the second maximum limit. The processor also sets the frequency of the clock generator 16 to correspond to this power consumption value. Typically, the frequency of the clock generator is set to a minimum value. In all peripheral devices 2, it is not necessarily possible to control the frequency of the clock generator 16, wherein the clock generator 16 cannot be used for controlling the power consumption.

In the operations of initializing the peripheral device, performed by the electronic device 1, the type of the peripheral device 2 is preferably examined, which may affect the type of initialization operations to be performed. However, this description will only discuss the operations which are essential in view of the invention. The signalling to be performed in this method according to the advantageous embodiment of the invention is illustrated in a simplified manner in the appended FIG. 3. The determination of the type of the peripheral device 2 will be followed by determining the first and second maximum limits for power consumption which have been stored on the device 2, such as a card. Thus, a maximum limit reading message is preferably transmitted from the electronic device 1 to the peripheral device 2. This is illustrated by a signal on a line 301 in the chart of FIG. 3. The message is received in the peripheral device 2 and its content is preferably examined in the processor 13. On the basis of the message, the processor 13 reads the first maximum limit and the second maximum limit from the memory 14 (block 302 in FIG. 3). If there are more than two maximum limits, the number of the maximum limits is preferably stored in the memory means, wherein the processor 13 reads the values of all the maximum limits from the memory 14. After this, the processor 13 generates a reply message (block 303) containing the requested information, such as the first and second maximum limits and, if necessary, also the number of the maximum limits. In the case of several maximum limits, also the values of the other maximum limits are preferably

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included in the message. The message is transmitted via the I/O blocks 9, 12 to the electronic device (as indicated by a signal on a line 304), in which the control block reads the information of the received message and, if necessary, stores the information in the memory 4 of the electronic device.

After the maximum limits of power consumption supported by the peripheral device are known in the electronic device 1, it is possible to start to adjust the power consumption of the peripheral device, if necessary. Let us assume that the electronic device 1 is capable of supplying the power corresponding to the second maximum limit to the peripheral device 2. Thus, a power control message is transmitted from the electronic device 1 to the peripheral device 2 (as indicated by a signal on a line 305). This power control message indicates the power consumption value which is to be set as the maximum value for the peripheral device 2, for example said second maximum limit. The processor 13 of the peripheral device examines the type of the received message, and after determining that it is a power control message, reads the maximum value for power consumption indicated in the message (block 306). Next, the processor 13 of the peripheral device sets, for example the operating frequency of the clock generator 16 to a value corresponding to this maximum value for power consumption, for example to the highest possible frequency. In some embodiments, the bus widths within the processor can also be changed according to the maximum limit used for power consumption. Furthermore, the peripheral device 2 preferably informs the electronic device 1 that the power consumption has been limited to the requested value (as indicated by a signal on a line 307).

If the electronic device 1 cannot supply the peripheral device 2 with the power of the second maximum limit, or if, for another reason, the electronic device 1 tends to set the maximum value for power consumption lower than the second maximum limit, it is possible to perform signalling, by which the electronic device 1 and the peripheral device try to find such a maximum limit for power consumption which is suitable in the situation. This can be carried out, for example, in such a way that the electronic device 1 selects, between the first and second maximum limits, a value which is a maximum value from the point of view of the electronic device 1. Information about this limit is transferred to the peripheral device 2, in which the suggested value is examined in the processor 13, and if it is found acceptable, this information is transferred to the electronic device 1. If the peripheral device 2 cannot set its own power consumption to such a level which corresponds to the suggested maximum value, the peripheral device 2 will suggest a lower value between the first and second maximum values. If this value is possible from the point of view of the electronic device 1, the electronic device 1 will transmit this information to the peripheral device 2, in which the power consumption is set to this value. If the value suggested by the peripheral device 2 is not suitable, the electronic device 1 advantageously selects another, preferably lower value which, however, is at least equal to the first maximum limit, and reports it to the peripheral device 2. The above-presented steps are iterated, until such a power consumption value is found which is suitable for both the electronic device 1 and the peripheral device 2. In some cases, it may occur that the only suitable value is the first maximum value, wherein the power consumption does not need to be adjusted, because this value is the default value.

There may also be a need to change the value of the power consumption during the operation of the electronic device 1 and the peripheral device 2 connected together. For example,

if the peripheral device is a transceiver card, such as a mobile station card or a modem card, there may be a need to significantly change the power consumption limit of the peripheral device 2, for example, for the time of a transmission. Thus, at the stage when e.g. the peripheral device 2 detects a need to change the power consumption, it transmits a message to the electronic device 1 and proposes a new power consumption value which is, however, in the range between the first and second maximum values. An exchange of messages is performed between the electronic device 1 and the peripheral device 2 by applying the above-described principles, to control the power consumption of the peripheral device according to the need. When the need for power consumption is changed again, a new adjustment of the power consumption can be made.

The need to change the power consumption of the peripheral device may also develop in the electronic device 1. For example, when the operation of the electronic device 1 shifts to a power saving mode, or when the charge of a battery (not shown) in the electronic device is reduced, the electronic device 1 may control the peripheral device 2 to shift to a less power consuming state.

The peripheral device according to the invention can also be connected to such an electronic device 1 which does not have a possibility to adjust the power consumption. Thus, the peripheral device 2 sets a default value, i.e. preferably the first maximum limit, as the power consumption value. Consequently, the peripheral device according to the invention can also be connected to such an electronic device 1 in which the steps of the method according to the invention are not carried out to control the power consumption of the peripheral device 2.

Above, the use of more than two different maximum limits were mentioned as the maximum values for power consumption. In this context, it is assumed that the other maximum limits are between the first and second maximum limits. These different maximum limits are feasible, for example, in such applications, in which different bus widths can be selected in the peripheral device. For example, in the system of FIG. 2, the bus width of the connection between the peripheral device and the electronic device can be selected to be any of the three values: 8, 16 or 32 bits. At the same time, this bus width selected for the connection is, in this advantageous embodiment, also used in the internal bus 17 of the peripheral device 2. Typically, the power consumption is the higher, the wider the bus used. Thus, the presumption is preferably that the bus width at the start-up stage is 8 bits, but the electronic device 1 and the peripheral device 2 may negotiate on the use of another bus width, i.e. on the change of the maximum limit for power consumption. This can be implemented by applying the principles described above. However, it will be obvious that said bus widths are only some non-restricting examples of bus widths.

The frequency of the clock generator 16 of the peripheral device is not necessarily adjustable in a stepless manner, but it is possible to select a value for the frequency from some predetermined values. Thus, the maximum limits for power consumption corresponding to these different frequencies can be stored as said maximum limits in the peripheral device, or if only the first maximum limit (lowest power consumption) and the second maximum limit (highest power consumption) are stored, it is possible to perform the exchange of messages between the electronic device 1 and the peripheral device, as described above in this description, to adjust the suitable power consumption limit.

Consequently, the power consumption of the peripheral device 2 can be adjusted e.g. by changing the clock fre-

quency and/or the bus width, but it should be evident that other methods for adjusting power consumption are also known and are applicable in connection with the invention. Power consumption can also be controlled by controlling the operating voltage, if the operating voltage of the peripheral device 2 does not need to be a given constant value. Peripheral devices are known, in which the operating voltage can be selected to be, for example, either 3 V, 3.3 V, or 5 V. Yet another example to be mentioned in this context of the possibilities to control the power consumption of the peripheral device is to control the current consumption of the peripheral device.

Further, the power consumption of the peripheral device 2 can also be adjusted by changing the clock frequency of the bus of the connection between the peripheral device and the electronic device, if it is independently adjustable. The clock frequency of the bus can be changed e.g. by the electronic device 1 and/or by the peripheral device 2, if necessary. The electronic device 1 controls a clock generator(s) (not shown) which produces the timing signals for the bus according to the same principles as was presented above.

In an advantageous embodiment of the invention, at least a part of the memory of the peripheral device 2 is divided into two or more memory blocks, to form so-called storage banks. Thus, in the peripheral device, one or more of these memory blocks can be selected for use, e.g. on the basis of the maximum power consumption value defined for the peripheral device 2. With higher power consumption values, it is typically possible to take more memory blocks into use than with lower power consumption values. FIG. 4 shows an example of the structure of such a peripheral device. In the peripheral device 2 shown in FIG. 4, the memory 14 is provided with four memory blocks 14a, 14b, 14c, 14d, but it will be obvious that in practical applications, the number of storage banks can, within the scope of the invention, also be other than four. To take the memory blocks 14a-14d into use and to remove them from service, connection lines 18a-18d are preferably provided from the processor 13, to couple e.g. the operating voltage to the desired memory blocks 14a-14d, or the coupling lines are used to switch each memory block 14a-14d either to an active mode or to a power-saving mode. Also the above-presented method can be used to control the power consumption of the peripheral device 2 instead of or in addition to the methods for controlling the power consumption as presented above in this description.

In the electronic device 1, the power control can be performed, for example, by providing the electronic device 1 with a power source whose output voltage can be changed. Thus, in the electronic device 1, the operating voltage to be supplied to the peripheral device is selected to be the voltage value corresponding to the power consumption at the time.

The method according to the invention can also be applied in the implementation of various contents for use in connection with electronic devices 1, for example in the following way. As the peripheral device 2, it is possible to use a memory card, such as a card complying with the definitions of the MultiMediaCard™ standard, in which contents can be stored. In this context, contents refer to data files, application programs, electronic books, audiovisual information, such as music, videos, etc. For example, a content provider stores such contents on the memory card. Thus, the memory card 2 is connected to an electronic device provided with means for transferring the content to the memory card 2. Thus, before starting the storage, the electronic device and the memory card 2 set the power consumption of the

memory card preferably to a value corresponding to the second maximum limit. This is possible, because in such an electronic device 1 used for storing contents, the power consumption of the memory card has hardly any significance, but the electronic device 1 can supply the memory card 2 with the sufficient power. The storage can thus be performed at a maximum rate, because the clock frequency and/or bus width of the memory card can be set to the maximum. Also, the checkup of the content stored on the memory card 2, to detect possible storage defects, can be performed at a maximum rate. Thanks to the maximum storage and/or checkup rate, the content production rate of the electronic device 1 can be increased when compared with methods of prior art.

In a corresponding manner, at the stage when the content stored on the memory card 2 is to be used in an electronic device 1, the power consumption of the memory card 2 can be set to a level which is suitable for the electronic device 1, for example to the lowest possible power consumption. Thus, when applying the method of the invention, the content production rate does not need to be limited according to the maximum power consumption value possible in the use of the content.

Because the method according to the invention can be used for the power control of the peripheral device, the peripheral device 2 can be connected to a variety of electronic devices. In some electronic devices, it is only possible to supply the peripheral device with the power (voltage and current) corresponding to the minimum power consumption, wherein the electronic device 1 does not need a large regulator, and the size of the electronic device does not need to be increased because of the need of space for a large regulator. On the other hand, power consumption does not need to be restricted in peripheral devices 2 to be developed, because the suitable power consumption value can be negotiated by the electronic device and the peripheral device. Thus, if the peripheral device is connected to such an electronic device, in which a relatively high power can be supplied to the peripheral device connection, the peripheral device can be used as efficiently as possible (with a high clock frequency/large bus width). At the stage of initialization, even such a peripheral device will operate with a lower power consumption, until a suitable power consumption value has been selected. In the system according to the invention, it is possible to provide for the use of peripheral devices which will be developed in the future and may require even high power in electronic devices. However, it is not necessary to consider cards with a high power consumption in the design of all electronic devices.

It will be evident to those of skill in the art that the steps to be taken in the setting of the power consumption can also be implemented in another way than the above-presented hand-shake in the form of messages. For example, the connection means 7, 10 can be provided with connection lines which are used to set the power consumption of the peripheral device. Furthermore, the invention can be applied in such a way that certain alternative (allowable) values are defined for said maximum limits, wherein the first maximum limit and the second maximum limit for each peripheral device is selected from the set of these alternative limits.

It should also be mentioned that the peripheral device 2 does not need to be a card-format peripheral device, but the peripheral device 2 used can also be another device which can be connected to the electronic device 1. One non-restrictive example to be mentioned of such a peripheral device is a camera which is connected, for example, to a wireless communication device, a computer, or the like.

Thus, by controlling the power consumption, it is possible to affect the functional properties of the camera. For example, the rate of updating the images of the camera on the display of the electronic device may be lower with a lower power consumption than with a higher power consumption. Thus, the electronic device 1 may preferably set the power consumption of the camera used as the peripheral device 2 on the basis of how high a power can be supplied by the electronic device 1 to the peripheral device. In an advantageous embodiment of the invention, also the user of the electronic device 1 can set a maximum limit for the power consumption, wherein the user can, if necessary, e.g. reduce the maximum limit to prolong the time of operation of the electronic device.

It should be evident that the present invention is not limited solely to the above-presented embodiments but can be modified within the scope of the appended claims.

The invention claimed is:

1. A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption; setting the power consumption of the peripheral device at a startup state to said default value; reading from the memory at least said limiting value which is higher than said default value; and setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value, wherein information is transferred from the electronic device to the peripheral device for setting the maximum of the power consumption of the peripheral device.

2. The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption.

3. The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said default value.

4. The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

5. The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

6. The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

7. A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, wherein the peripheral device com-

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prises a memory, said memory storing a default value and a limiting value for the power consumption; setting the power consumption of the peripheral device at a startup stage to said default value; reading from the memory at least said limiting value which is higher than said default value; and setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

8. The method according to claim 7, wherein said limiting value is used as a highest allowable value for the power consumption.

9. A system comprising a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;

an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and

means for determining power consumption, wherein the power consumption of the peripheral device is set at a startup stage to said default value, wherein at least said limiting value which is higher than said default value is stored for the power consumption, wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

10. The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

11. The system according to claim 9,

wherein the peripheral device comprises at least one bus, and

wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

12. The system according to the claim 9,

wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

13. The system according to the claim 9, wherein the electronic device is a portable electronic device.

14. The system according to claim 13, further comprising means for performing mobile station functions.

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15. An electronic device comprising:

means for connecting a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;

means for supplying power to the peripheral device; and means for determining power consumption, wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value which is higher than said default value is defined for the power consumption,

wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

16. The electronic device according to claim 15, wherein it is a portable electronic device.

17. The electronic device according to claim 16, further comprising means for performing mobile station functions.

18. A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption;

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value which is higher than said default value is defined for power consumption, wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

19. The peripheral device according to claim 18, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

20. The peripheral device according to claim 18, further comprising

means for generating at least one clock signal and means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

21. The peripheral device according to claim 18, further comprising

at least one bus and means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

22. The peripheral device according to the claim 18, wherein the peripheral device is provided with two or more storage blocks, and

wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

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23. The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device.

24. The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard™ peripheral device.

25. An electronic device comprising:
a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;
a power supply configured to supply power to the peripheral device; and
a power gauge configured to determine power consumption, wherein the power consumption of the peripheral device is set at a startup stage to said default value, wherein at least said limiting value which is higher than said default value is defined for the power consumption, wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

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26. The electronic device according to claim 25, wherein it is a portable electronic device.

27. The electronic device according to claim 25, further comprising a memory configured to store the default value and the limiting value.

28. A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption;
a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device, wherein the power consumption of the peripheral device is set at a startup stage to said default value, wherein at least said limiting value which is higher than said default value is defined for power consumption, wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

29. The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo Mylly

Appl. No.: To Be Assigned

*(Narrowing Reissue of U.S. Patent No. 7,278,033
B2; Issued: October 2, 2007)*

Filed: Herewith

For: **METHOD FOR ADDRESSING
MEMORY CARD, A SYSTEM USING
A MEMORY CARD, AND A
MEMORY CARD**

Confirmation No.: To Be Assigned

Art Unit: To Be Assigned

Examiner: To Be Assigned

Atty. Docket: 3371.002REI0

**Preliminary Amendment in a Reissue Application Under 37 C.F.R. §
1.173(b) and Statement of Status and Support for all Changes to the Claims
Under 37 C.F.R. § 1.173(c)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In advance of prosecution, Applicant submits the following amendments and remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19 0036.

Amendments to the Claims

Please replace the originally patented claims with the claims as shown below.

The claim identifiers, or lack thereof, below conform identically to the rules for reissue amendments set forth in 37 C.F.R. §§ 1.173(b)(2), (c), (d), and (e). (See also, M.P.E.P. §§ 1453 (II), (IV), and (V)).

1. (Original Patent Claim) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;

setting the power consumption of the peripheral device at a startup state to said default value;

reading from the memory at least said limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum of the power consumption of the peripheral device.

2. (Original Patent Claim) The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption.

3. (Original Patent Claim) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption set for the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption set for the peripheral device is a value corresponding to said default value.

4. (Original Patent Claim) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

5. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

6. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

7. (Original Patent Claim) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which the power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;

setting the power consumption of the peripheral device at a startup stage to said default value;

reading from the memory at least said limiting value which is higher than said default value; and

setting the maximum of the power consumption to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum of the power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

8. (Original Patent Claim) The method according to claim 7, wherein said limiting value is used as a highest allowable value for the power consumption.

9. (Original Patent Claim) A system comprising
a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;
an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and
means for determining power consumption,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,
wherein at least said limiting value which is higher than said default value is stored for the power consumption,
wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and
wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

10. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

11. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises at least one bus, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

12. (Original Patent Claim) The system according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

13. (Original Patent Claim) The system according to the claim 9, wherein the electronic device is a portable electronic device.

14. (Original Patent Claim) The system according to claim 13, further comprising means for performing mobile station functions.

15. (Original Patent Claim) An electronic device comprising:
means for connecting a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;
means for supplying power to the peripheral device; and
means for determining power consumption,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,
wherein at least said limiting value which is higher than said default value is defined for the power consumption,
wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a

range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

16. (Original Patent Claim) The electronic device according to claim 15, wherein it is a portable electronic device.

17. (Original Patent Claim) The electronic device according to claim 16, further comprising means for performing mobile station functions.

18. (Original Patent Claim) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption;
means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value which is higher than said default value is defined for power consumption,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device.

19. (Original Patent Claim) The peripheral device according to claim 18, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

20. (Original Patent Claim) The peripheral device according to claim 18, further comprising

means for generating at least one clock signal and

means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

21. (Original Patent Claim) The peripheral device according to claim 18, further comprising

at least one bus and

means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

22. (Original Patent Claim) The peripheral device according to the claim 18, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

23. (Original Patent Claim) The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device.

24. (Original Patent Claim) The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard.TM. peripheral device.

25. (Original Patent Claim) An electronic device comprising:
a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for the power consumption;
a power supply configured to supply power to the peripheral device; and
a power gauge configured to determine power consumption,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,
wherein at least said limiting value which is higher than said default value is defined for the power consumption,
wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and
wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum of the power consumption of the peripheral device.

26. (Original Patent Claim) The electronic device according to claim 25, wherein it is a portable electronic device.

27. (Original Patent Claim) The electronic device according to claim 25, further comprising a memory configured to store the default value and the limiting value.

28. (Amended) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption;
a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value which is higher than said default value is defined for power consumption,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, [and]

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum of the power consumption of the peripheral device, and

wherein the means for setting the maximum power consumption includes a processor configured to read an indication of the value from the received information and to set the maximum power consumption to the value based on the indication.

29. (Original Patent Claim) The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device.

30. (New) The peripheral device of claim 28 further comprising:

a clock generator,

wherein the processor is configured to adjust a frequency of the clock generator in response to the received information from the electronic device.

31. (New) The peripheral device of claim 30, wherein the processor is configured to adjust the frequency of the clock generator to a first frequency corresponding to the maximum power consumption.

32. (New) The peripheral device of claim 28, wherein the peripheral device is a memory card.

33. (New) The peripheral device of claim 28, wherein the limiting value is a highest possible maximum power consumption of the peripheral device.

34. (New) The peripheral device of claim 28 further comprising:
a plurality of memory blocks, wherein each of the plurality of memory blocks is configured to include at least an active mode and a power-saving mode.

35. (New) The peripheral device of claim 34, wherein the processor is configured to adjust the number of memory blocks in the plurality of memory blocks that are in the active mode in response to the received information from the electronic device.

36. (New) The peripheral device of claim 35, wherein the processor is further configured to increase the number of memory blocks in the plurality of memory blocks that are in the active mode in response to the received information from the electronic device indicating the value for the maximum power consumption being greater than the default value.

37. (New) The peripheral device of claim 28, wherein the default value is a lowest possible maximum power consumption for the peripheral device.

Remarks

Specification Amendments (37 C.F.R. § 1.173(b)(1) and (d))

No amendments are being sought in the patented specification.

Notification of Concurrent Proceeding (37 C.F.R. § 1.178(b))

Applicant has no knowledge of related concurrent proceedings.

Statement of Status of Currently Pending Claims (37 C.F.R. § 1.173(c))

Upon entry of the foregoing amendment, patent claims 1-28 and added new claims 30-37 are pending in the application, with claims 1, 7, 9, 15, 18, 25, and 28 being the independent claims. Patent claim 28 is sought to be amended. New claims 30-37 are sought to be added. The amended and added claims are believed to introduce no new matter, and their entry is respectfully requested.

Explanation of Support for Added Claims (37 C.F.R. § 1.173(c))

Example support in the issued patent for the amended and new claims is shown in the table below.

Claim	Example Support (Col:line or Fig./Element)
28	[6:12-25]
30	[8:13-22]
31	[7:54-65]
32	[8:57-60]
33	[7:57-65]
34	[8:23-47]
35	[8:23-47]
36	[8:23-47]
37	[7:57-65]

Conclusion

Prompt and favorable consideration of this Preliminary Amendment is respectfully requested. Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jason D. Eisenberg #43447/

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date: May 24, 2013

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
1684908_1.DOCX

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device			
First Named Inventor/Applicant Name:	Kimmo MYLLY			
Filer:	Jason Daniel Eisenberg/LaTishia Tillman			
Attorney Docket Number:	3371.002REI0			
Filed as Large Entity				
Reissue (Utility) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility Reissue Basic	1014	1	280	280
Design and Utility Reissue Basic	1114	1	600	600
Design and utility Reissue Basic	1314	1	2160	2160
Pages:				
Claims:				
Reissue claims in excess of 20	1205	17	80	1360
Independent Claims Reissue	1204	4	420	1680
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD (\$)	6080

Electronic Acknowledgement Receipt

EFS ID:	15866662
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Jason Daniel Eisenberg/LaTishia Tillman
Filer Authorized By:	Jason Daniel Eisenberg
Attorney Docket Number:	3371.002REI0
Receipt Date:	24-MAY-2013
Filing Date:	
Time Stamp:	15:42:36
Application Type:	Reissue (Utility)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$6080
RAM confirmation Number	3400
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /zip	Pages (if appl)
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1		3371002REI0AppFiling.pdf	1863139 4ec8ceeeef8e970e23b9090339495824d1b744bb	yes	11
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Transmittal Reissue Application	1	3	
		Authorization for Extension of Time all replies	4	4	
		Consent of Assignee accompanying the declaration	5	5	
		Power of Attorney	6	7	
		Assignee showing of ownership per 37 CFR 3.73.	8	9	
		Reissue dec filed in accordance with MPEP 1414	10	11	
Warnings:					
Information:					
2	Application Data Sheet	3371002rei0ADS.pdf	961674 2e0db243036dee55a1286204a2d8046c9adb778	no	6
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3		3371002REI0App.pdf	1910647 10fcff1c53c5d328f4938223c8357a962890d9ed	yes	13
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Abstract	1	2	
		Drawings-only black and white line drawings	3	6	
		Specification	7	10	
		Claims	11	13	
Warnings:					
Information:					
4		3371002rei0PreliminaryAmendment.pdf	172175 ed396a014193cf21651cbbbed8a75a6f6dbc0c1c2	yes	12

Multipart Description/PDF files in .zip description			
Document Description	Start	End	
Preliminary Amendment	1	1	
Claims	2	10	
Applicant Arguments/Remarks Made in an Amendment	11	12	

Warnings:

Information:

5	Fee Worksheet (SB06)	fee-info.pdf	38009	no	2
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Warnings:

Information:

Total Files Size (in bytes):			4945644		
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/902,227	Filing Date 05/24/2013	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input checked="" type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	280
<input checked="" type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	600
<input checked="" type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	37 minus 20 =	* 17	x \$80 =	1360
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4	x \$420 =	1680
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL
				4640

APPLICATION AS AMENDED – PART II

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	05/24/2013	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	* 37	Minus	** 37	= 0	x \$80 = 0
	Independent (37 CFR 1.16(h))	* 7	Minus	***7	= 0	x \$420 = 0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	0

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$ =
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

LDRC
/ROBERT TALBERT/

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Application Number	13/902,227
			Filing Date	May 24, 2013
			First Named Inventor	Kimmo MYLLY
			Art Unit	2184
			Examiner Name	To be assigned
			Attorney Docket Number	3371.002RE10
Sheet	1	of	1	

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
	US1	4,841,440		06-20-1989	Yonezu et al.	
	US2	5,483,656		01-09-1996	Oşrescu et al.	
	US3	5,532,945		07-02-1996	Robinson	
	US4	5,606,704		02-25-1997	Pierce et al.	
	US5	5,613,130		03-18-1997	Yeng et al.	
	US6	5,737,616		04-07-1998	Watanabe	
	US7	5,758,108		05-26-1998	Nakamura	
	US8	5,758,171		05-26-1998	Ramamurthy et al.	
	US9	5,884,086		03-16-1999	Amoni et al.	
	US10	5,892,729		04-06-1999	Holder, Jr.	
	US11	5,996,083		11-30-1999	Gupta et al.	
	US12	6,178,514 B1		01-23-2001	Wood	
	US13	6,477,388 B1		11-05-2002	Schmutz	
	US14	6,785,830 B1		08-31-2004	McKeen et al.	
	US15	6,859,882 B2		02-22-2005	Fung	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					
	FP1	GB 2 235 797 A		03-13-1991	Apple Computer		
	FP2	WO 98/41987 A1		09-24-1998	Hitachi LTD		
	FP3	WO 02/07494 A2		01-31-2002	Sierra Wireless Inc.		

1699182_1.DOCX

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	13/902,227
		Filing Date	May 24, 2013
		First Named Inventor	Kimmo MYLLY
		Art Unit	2184
		Examiner Name	To be assigned
		Attorney Docket Number	3371.002REJ0
		Sheet	1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	USB Specification Revision, published April 27, 2000; pp.171-174	
	NPL2	English-Language Abstract for International Patent Publication No. 98/41987 A1, published September 24, 1998; 1 page	
	NPL3	Notice of Allowance mailed June 13, 2007 for U.S. Patent Application No.10/401,338, filed March 26, 2003; 12 pages	
	NPL4	Non-Final Rejection mailed September 22, 2005 for U.S. Application No.10/401,338, filed March 26, 2003; 10 pages	
	NPL5	Non-Final Rejection mailed July 14, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 8 pages	
	NPL6	Final Rejection mailed March 23, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 11 pages	
	NPL7	Final Rejection mailed December 27, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 8 pages	
	NPL8	International Search Report directed to related International Patent Application No. PCT/FI03/00233, mailed June 27, 2003; 5 pages	
	NPL9	International Preliminary Report on Patentability directed to related International Patent Application No. PCT/FI03/00233, mailed June 24, 2003; 7 pages	
	NPL10	European Search Report directed to related European Patent Application No. 03 708 304.5-1527, mailed November 24, 2006; 6 pages	

Examiner Signature		Date Considered	
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO				Complete if Known	
				Application Number	13/902,227
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Filing Date	May 24, 2013
				First Named Inventor	Kimmo MYLLY
				Art Unit	2184
				Examiner Name	To be assigned
				Attorney Docket Number	3371.002REI0
				Sheet	2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T ²
	NPL11	European Search Report directed to related European Patent Application No. 03 708 304.5-1527, mailed December 20, 2007; 5 pages	
	NPL12	European Search Report directed to related European Patent Application No. 03 708 304.5-1527, mailed March 5, 2009; 4 pages	

1700245_1.DOCX

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

(21) Application No 9018259.3
 (22) Date of filing 20.08.1990
 (30) Priority data
 (31) 405637 (32) 08.09.1989 (33) US

(51) INT CL⁵
 G06F 1/32
 (52) UK CL (Edition K)
 G4A ASX
 (56) Documents cited
 US 4698748 A
 (58) Field of search
 UK CL (Edition K) G4A ASX
 INT CL⁵ G06F

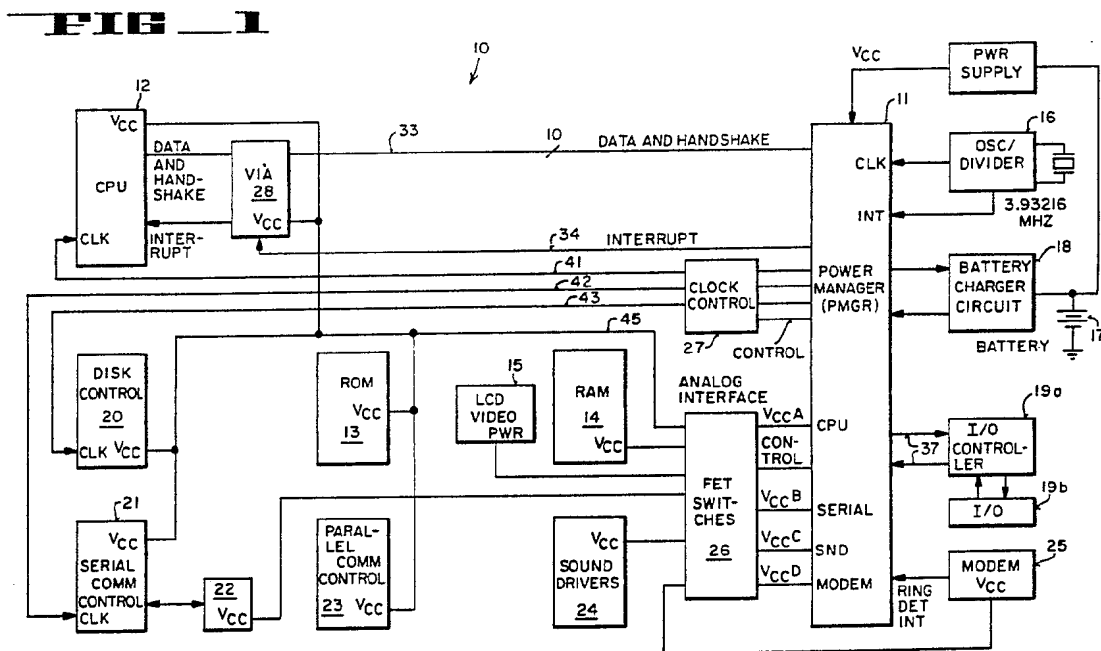
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(72) Inventors
R Steven Smith
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Robert L. Bailey

(74) Agent and/or Address for Service
Potts Kerr and Co
 15 Hamilton Square, Birkenhead, Merseyside,
 L41 6BR, United Kingdom

(54) Power management for a portable computer

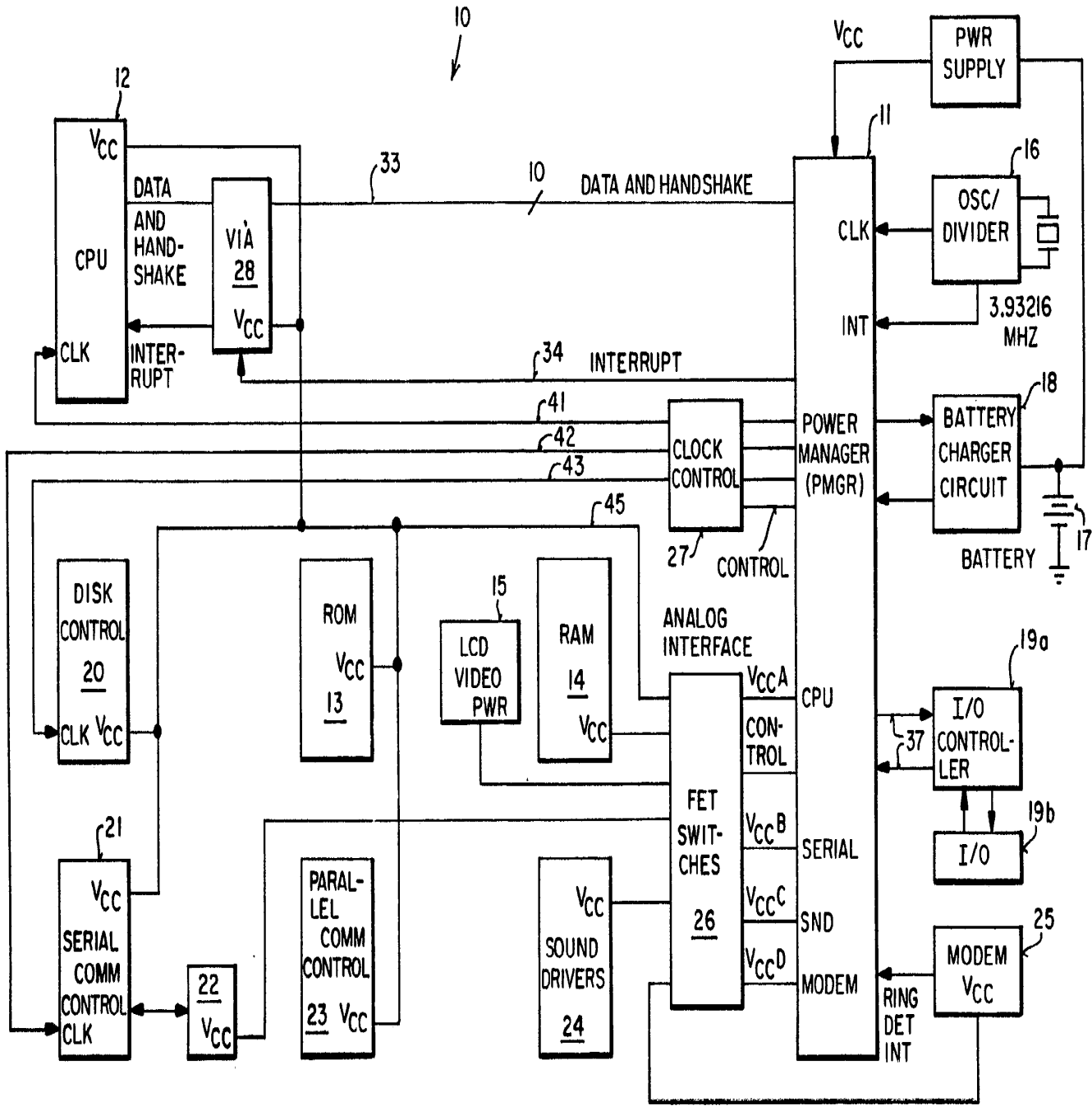
(57) A power manager (PMGR) within a portable laptop computer provides power (via 26) and clocking control (via 27) to various units within the computer in order to conserve battery power. Transistor switches controlled by the power manager control the distribution of power and clock signals to the various units within the computer. The power manager includes a software routine for continually monitoring various units and when certain units are either not needed and/or not currently in use, power and/or clock signals are removed from a given unit, and the computer can be switched between three modes viz. normal, slow and sleep.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 235 797 A

FIG 1



1/2

FIG 2

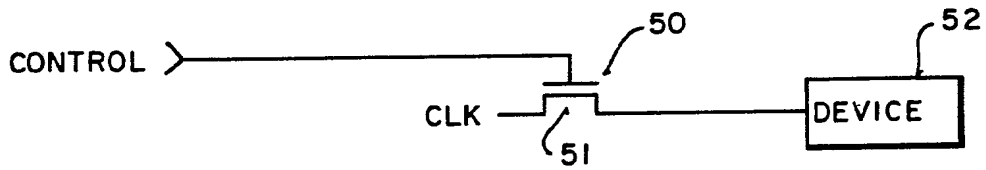
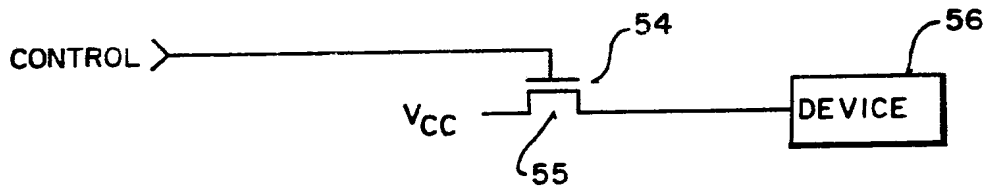


FIG 3



BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power distribution scheme in a portable computer and, more specifically, to power management in a laptop computer.

2. Prior Art

Power consumption in an electronic device is always a significant concern and a power supply must be designed to adequately power the device. Aside from the capability of the power supply to provide ample power to power the corresponding device, heat dissipation, physical size, weight, efficiency, and other related characteristics are paramount in designing or selecting the power source. These characteristics become exceptionally critical when the device the power supply is to support is a self-sufficient portable unit.

In many portable units, a self-supporting power source, such as a battery, is used to provide the power when the unit is decoupled from its main or external power source, such as 110 Volt AC (ordinary house current). Typically a battery is used to provide the independent and portable power source. In some instances the battery functions as an auxiliary power source to maintain certain critical circuits active, such as keeping the memory alive to retain any information stored in the memory. In other instances, the battery functions as the main power source to fully power the device.

In the area of information processing, miniaturization of processing devices has permitted the portability of computing devices. One of the first such portable processing devices was a hand held calculator, wherein the calculator operated from a battery power source and could easily be carried about by the user. The battery would power all of the functions of the calculator

and the user could readily transport the calculator without any attachment to an external power source. The batteries were either replaced or recharged. The earliest calculators simply had an on/off state in which full power was available during the on state and the power was completely shut off during the off state.

5 Because of the volatile nature of many early semiconductor memories, information stored in such volatile memories were lost when the calculator was turned off. Subsequent calculators attempted to incorporate nonvolatile memory, or in the alternative, standby power was provided to such a memory when the device was turned off, so that the memory retained whatever
10 information was present. More advanced schemes were devised to monitor various functions, so that power was removed from various elements when those elements were not needed. Further, a time-out scheme was devised to put the calculator in a stand-by mode, such as when a key was not depressed after a certain time period, in order to preserve power. All of these features
15 were devised primarily to extend the time period that the device could operate from its internal power source.

When the processing technology was expanded beyond a simple calculator to encompass personal desk top computers, additional constraints were placed to power consumption and management control schemes. Aside
20 from the additional circuitry, additional memory devices consumed considerable amounts of power. These memory devices include semiconductor devices, such as read-only memories (ROMs) and random-access memories (RAMs) which include volatile and non-volatile memories, floppy disk drives and hard disk drives and other magnetic media. Also, additional
25 power is required to power the display unit which typically includes a viewing screen. Various schemes were devised to monitor and control the power distribution during on/off states.

However, as the personal desk top computer systems are made portable, it is desirable to provide a computer which contains a fully contained power source so that the computer is completely portable. These self-sufficient computer systems are typically referred to as laptops (because of the small physical size and light weight) and are designed to operate for a certain number of hours from its internal power source, which is typically a battery. Although a variety of the portable calculator technology can be implemented within such a laptop, additional constraints are placed in that the additional circuitry, memory, viewing screen and any peripheral devices attached to the system will necessarily consume additional power. In order to extend the self-sustaining time period of these laptops while keeping the battery size and weight to a minimum, a sophisticated power management scheme is required to provide power only to those circuits and devices which require such power and to remove power, or at least to make a given circuit enter a low power consumption mode, when that circuit is not needed. The management scheme must also continually monitor the various circuits and devices in order that power can be applied immediately to activate such circuits and devices when needed.

The present invention provides for such a power management apparatus for a laptop computer in order to extend the self-sustaining time period so that the laptop computer can operate for an extended period of time once external power is disconnected.

3. Prior Art References

A number of prior art references are known for monitoring and controlling the consumption of power to a device or to a portion of a device including a means of providing a timeout when user interaction has not occurred for a given time period. However, these references pertain to the simpler calculator technology or to portions of a computer system and fail to disclose the

sophisticated power management scheme for a laptop of the present invention.

The references are:

1. U.S. Patent No. 4,019,068, issued April 19, 1977, for Low Power Output Disable Circuit For Random Access Memory;
- 5 2. U.S. Patent No. 4,074,351, issued February 14, 1978 for Variable Function Programmed Calculator;
3. U.S. Patent No. 4,151,611, issued April 24, 1979 for Power Supply Control System For Memory Systems;
4. U.S. Patent No. 4,293,927, issued October 6, 1981 for Power
10 Consumption Control System For Electronic Digital Data Processing Devices;
5. U.S. Patent No. 4,279,020, issued July 14, 1981 for Power Supply Circuit For A Data Processor;
6. U.S. Patent No. 4,381,552, issued April 26, 1983 for Standby Mode Controller Utilizing Microprocessor;
- 15 7. U.S. Patent No. 4,409,665, issued October 11, 1983 for Turn-Off-Processor Between Keystrokes;
8. U.S. Patent No. 4,611,289, issued September 9, 1986 for Computer Power Management System;
9. U.S. Patent No. 4,615,005, issued September 30, 1986 for Data
20 Processing Apparatus With Clock Signal Control By Microinstruction For Reduced Power Consumption And Method Therefor; and
10. U.S. Patent No. 4,712,196, issued December 8, 1987 for Data Processing Apparatus.

SUMMARY OF THE INVENTION

The present invention describes a power manager for use in a laptop computer. The laptop computer is a fully self-sufficient computer which is
5 powered by an internal battery when the computer is disconnected from an external power source. Because power conservation is paramount to sustain the computer as long as possible from the internal battery, a power manager is provided to monitor and control various circuit operations. Various units of the computer, including peripheral units, generally function equivalently to
10 well-known personal desktop computers. However, the power source to the various devices are controlled by the power manager and a plurality of transistor switches are used to switch the power source to the various devices. The operation of these switches is controlled by the power manager. Additionally, various clock signals are also coupled through switches which
15 are controlled by the power manager so that the clock signals can be disconnected from certain units of the computer.

The power manager continually monitors various circuit functions such that devices not in use have their power sources or clock signals disconnected in order to deactivate devices to conserve battery power. The removal of clock
20 signals from those units having clock control places these various units into an inactive state. However, because power is still applied to these units, various internal states retain their current state until the clock signal is restored.

The power manager is capable of operating in one of three modes of operation. In a first mode the computer operates in a normal active mode where
25 most of the units are active at all times and/or some of the other units are caused to be made active when needed. A second state is a sleep state in which the computer enters into an inactive state and the power manager continues to monitor various circuit conditions. When a certain predetermined

condition occurs, it causes the computer to awake from its sleep state. A third state is an intermediate state in which the power manager controls the frequency of the clock signals to be decreased such that the power consumption drops by approximately 25-30% from the normal active mode.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit block diagram of the various units of the laptop computer and showing power lines, clock signal lines and control lines
5 pertaining to the power management scheme of the present invention.

Figure 2 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of a clock signal to a given device.

10

Figure 3 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of power to a given device.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

A power management system for a laptop computer is described. In the following description, numerous specific details are set forth, such as specific circuits, devices, etc., in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known circuits and signal lines have not been described in detail in order not to unnecessarily obscure the present invention.

Referring to Figure 1, an architecture for a portable computer 10 is shown, including the power manager (PMGR) 11 of the present invention. Although computer 10 can be of a variety of computers, computer 10 of the present invention is a portable computer and, more specifically, a laptop computer which is capable of operating without an external power source. Aside from the PMGR 11, computer 10 is comprised of a CPU 12, read-only memory (ROM) 13, random-access memory (RAM) 14, liquid crystal display (LCD) unit 15 which includes a viewing screen and associated video circuitry, crystal controlled clock and oscillator 16, a battery 17, a battery charger circuit 18 and an input/output (I/O) unit 19 which includes an I/O controller 19a and at least one I/O device 19b. These components are typically present in most desktop or portable computer systems. Computer 10 of the present invention further includes a disk controller 20, a serial communication controller 21 and its drivers 22, a parallel communications controller 23, sound circuit and drivers 24, and a modem 25. It is to be appreciated that although units 20-25 are included within computer 10 that these devices are typically a design choice and the computer 10 can readily operate as a functioning computer without the presence of these units.

Several additional units are included within computer 10 to operate with the PMGR unit 11. Analog interface unit 26, clock control unit 27 and an internal interface unit, referred to as a via unit 28, are included to function in conjunction with the PMGR 11. It is to be appreciated that units 12-25 are devices used in prior art computers and such description and operation of these units are not included herein. Units 12-25, except for unit 17 and 18, are available with the Macintosh™ brand computers of Apple Computer Inc., of Cupertino, California.

In functional terms, CPU 12 is the main processing unit for computer 10 and in the preferred embodiment is a 68000 based (part numbers 68000, 68020 and 68030) processor manufactured by Motorola Corporation. ROM 13 is used to store the operating system of the computer 10 as well as other proprietary programs, such as file directory routines. RAM 14 is utilized as the internal memory of the computer for accessing of data. The LCD display 15 with its associated video circuitry provides for the presentation of a display on a viewing screen. The crystal operated clock 16 provides for the necessary timing reference signals which are needed for the operation of computer 10. The battery 17 powers computer 10, permitting computer 10 to be a fully portable unit. Battery charger circuit 18 monitors the level of the battery 17 as well as charging the battery 17 when computer 10 is coupled to an external power source such as 110 Volts AC.

The I/O unit 19 interfaces with various I/O devices, such as keyboards and cursor control devices, such as a "mouse" or a trackball. The disk controller unit 20 is used to access a disk storage medium, such as a floppy disk. In computer 10, a hard disk is coupled and accessed by the parallel communications controller 23. The serial communication controller 21 and its drivers 22 are utilized to provide serial communication, such as supporting a RS-232 protocol. The sound circuits and drivers of sound unit 24 are utilized to

generate various audio signals from computer 10. Modem 25 is typically an external device, however, in this instance it is included within computer 10 to provide full modem capability, in order that the portable computer 10 has capabilities of interfacing with telecommunication lines at various remote
5 locations.

The power management apparatus of the present invention is comprised of PMGR 11, analog interface unit 26, clock control unit 27 and via unit 28. Functionally, PMGR 11 is an intelligent assistant to the CPU 12, wherein PMGR 11 monitors the state of charge of battery 17, controls the power
10 consumption of the various subsystems, includes a real time clock which frequency is determined by the clock circuit 16, interfaces to the internal modem 25, as well as an interface to the I/O peripheral devices 19b through I/O controller 19a. It is to be appreciated that PMGR 11 of the preferred embodiment includes its own ROM, RAM, timers, analog to digital converters,
15 and general purpose I/O lines. Although a variety of devices can be used to perform the functions of PMGR 11, the preferred embodiment uses part number 50753, which is a semiconductor chip manufactured by Mitsubishi Corporation.

The software stored within PMGR 11 of the present invention provides
20 for three main functions in controlling the power management of the various devices. These functions are receiving commands from the CPU 12 and performing in response to these commands, controlling the transfer of communications between the PMGR and peripheral units coupled to the I/O controller unit 19, and monitoring the system as well as providing the timer to
25 maintain the real time clock. An 8-bit data bus and two handshake lines provide the coupling between CPU 12 and PMGR 11 through the via unit 28. The 8-bit databus is used to transfer command and data between CPU 12 and PMGR 11. This 8-bit communication is achieved by the use of a two line

handshaking scheme wherein commands are provided by CPU 12 and replies are provided by PMGR 11 on data and handshake lines 33.

Once the command is sent from CPU 12 through via unit 28 to PMGR 11 and the handshake is completed, PMGR 11 decodes the command and
5 executes it. If no reply data is to be returned, PMGR 11 waits for the handshake for the next command to begin from CPU 12. If reply data is to be returned, PMGR 11 begins the reply handshake and returns the requested data. In the preferred embodiment commands and replies are transmitted in a protocol comprising of a command/reply byte, a count byte and optional data bytes.

10 Once every 1/60 of a second (frequency of 60 Hz), the clock oscillator 16 generates an interrupt to PMGR 11 and this interrupt is coupled to CPU 12 on line 34. When this interrupt is generated, PMGR 11 closes the I/O channel from I/O controller 19 and further, will not respond to any handshake requests from CPU 12. The interrupt on line 34 causes CPU 12 to suspend the data
15 transfer to PMGR 11. During this interrupt cycle, PMGR 11 performs its periodic monitoring routines which include updating the real time clock, checking the battery power level and sending an auto poll command. The auto poll command is associated with the auto poll scheme of the preferred embodiment in which the CPU 12, through PMGR 11, automatically
20 interrogates (polls) devices coupled to bus 37 to determine the presence of data for transfer.

PMGR 11 contains the necessary I/O transceiver functions for transfer of information between PMGR 11 and I/O unit 19 on bus 37. Packets of information to be sent on bus 37 to I/O unit 19 are sent by CPU 12 to PMGR 11
25 in the data portion of the command signal. Data received by PMGR 11 from I/O controller 19 is buffered internally and once received, this data is stored within PMGR 11 until requested by CPU 12. If a new I/O command was transmitted by CPU 12 during a previous command/execution cycle, the new command and

its corresponding data is supplied as the next I/O command which is to be sent. If the I/O device has any data to return, PMGR 11 receives, buffers and stores the data. When the data is completely received, PMGR 11 interrupts CPU 12 on interrupt line 34 and CPU 12 responds to the interrupt by determining the source of the interrupt and data is obtained from PMGR 11.

5 PMGR 11 includes a one second timer which is based on the 60 Hz frequency of clock 16. PMGR 11 also includes its own internal clock which performs as a real time clock. The one second timer is used to supply a wake up timer and create the one second interrupt for triggering the various monitoring functions. That is, as each new second is counted within PMGR 11, a number of periodic operations occur. Firstly, the real time clock and the wake up timer (if enabled) are updated. The wake up timer is an internal alarm clock which is used to provide an alarm/signal whenever the real time clock coincides with the time set for the wake up timer (if enabled). Next, computer 10's power system and battery 17 are checked to determine the battery power level and if a low battery condition exists. The battery charger circuit 18 includes means for monitoring the level of the battery and for determining if the power level drops below a predetermined level. Then, the internal temperature is also checked followed by the interrupt to the CPU. Subsequently PMGR 11 sends any pending I/O transactions to CPU 12.

15 20 It is to be appreciated that via unit 28 performs the function of an interface unit between the CPU 12 and PMGR 11. Via unit 28 includes general purpose I/O devices, internal timers, interrupt generators, as well as input and output ports. However, it is to be noted that PMGR 11 can be readily adapted to operate without such a via unit 28 without departing from the spirit and scope of the present invention.

In order to provide the control over the consumption of power by computer 10 for the primary purpose of extending the life of battery 17 when

computer 10 is disconnected from an external power source, PMGR 11 provides for a number of control and monitoring functions for this purpose. PMGR 11 is utilized to cause computer 10 to be in one of three separate modes of operation. The three modes are the normal, slow and sleep modes. PMGR 5 11 responds to each of these modes by controlling the clocking signal being sent to a given device and/or controlling the voltage being supplied to a given unit. The clock signals coupled from the clock oscillator 16 to PMGR 11 are coupled to the clock control unit 27. Clock control unit 27 operates as a switch to couple the various clock signals on lines 41, 42 and 43 to CPU 12, serial 10 communication controller unit 21 and the disk controller unit 20, respectively.

A power supply 29, which receives its power from battery 17, provides the needed voltages by computer 10. These supply voltages, shown as Vcc's in Figure 1, are coupled through PMGR 11, wherein PMGR 11 provides separate Vcc sources to the various units through the analog interface unit 26. 15 As shown in Figure 1, VccA is coupled to the CPU 12 and related units. Three other separate Vcc sources are also provided from PMGR 11 as dedicated Vcc voltages to serial communication drivers 22, sound unit 24 and to the modem 25 through analog interface unit 26. These voltages are designated as VccB, VccC and VccD, respectively. It is to be noted that control lines are 20 also present between PMGR 11 and clock control unit 27 and between PMGR 11 and analog interface unit 26. In the preferred embodiment, analog interface unit 26 is comprised of a plurality of transistor switches for switching the various Vcc sources onto their corresponding lines. The clock control unit 27 also includes various switches for coupling the clock signals to the corresponding 25 units. Further, it is to be appreciated that PMGR 11 also includes circuitry for the various clocking signals for distribution onto lines 41-43. It is to be noted that PMGR 11 can change the various clocking rates of the clocking signals present on lines 41-43.

In the normal (or wake) mode of operation, computer 10 is fully active and all of the switches within clock control unit 27 and the analog interface unit 26 are closed. However, commands can be provided by CPU 12 automatically in response to stored routines, or in response to a user input through I/O unit 19, to deactivate transistor switches which couple VccB, VccC and VccD, in order to remove the applicable Vcc power from the serial communication controller drivers 22, sound drivers of unit 24 and modem 25. Alternatively, in order to conserve power of the battery, Vcc voltages for powering units 22, 24 and 25 need not be applied until such unit usage is requested by the system or the user.

In order to further conserve power, PMGR 11 will send computer 10 into a sleep (inactive) mode under an occurrence of either of two conditions. When the battery charger circuit 18 notes that battery 17 has dropped to a predetermined level, which level is deemed to be detrimental to further operation of computer 10, PMGR 11 places computer 10 into a sleep mode. PMGR 11 can also enter the sleep mode when a sleep command is provided by CPU 12. CPU sends a sleep command to PMGR 11 when there has been no user activity for a predetermined amount of time or when the user decides to stop work and shut down the computer 10.

Before entering the sleep mode, the operating system of the computer, as well as the various drivers, save the current state information in RAM 14. Thus, the state of the various registers, drivers and other memory devices are stored within RAM 14 for later restoration. Once these necessary states are stored in RAM 14, PMGR 11 releases all of the switches in analog interface unit 26 so that power is removed from the various units of computer 10. It is to be noted that power is removed from RAM 14 if RAM 14 is comprised of non-volatile memory such as an EPROM, which is the case with the memory device 14 of the present invention. However, if RAM 14 is comprised of volatile

memory then the transistor switch applying Vcc power to RAM 14 is kept closed so that Vcc is still applied to RAM 14 keeping it active in order to retain the stored information. It is to be noted that non-volatile memory is preferred so that Vcc need not be applied to RAM 14 in the sleep mode. Further, it is to be noted that the preferred embodiment uses CMOS memory.

In an alternative embodiment, VccA can be coupled onto line 45 in order to keep the power supplied to CPU 12. The internal clock of PMGR 11 can be decoupled from CPU 12 by clock control unit 27 thereby disabling the clock input to CPU 12 and halting the execution of the CPU. The CPU internal states are frozen with all CPU internal RAM and control registers remaining intact by halting the execution of the CPU. Halting the execution of CPU 12 typically will lower its power consumption by two orders of magnitude.

Although a number of conditions can cause computer 10 to wake from the sleep mode, computer 10 of the present invention has three possible conditions which triggers it to leave the sleep mode. PMGR 11 continues to monitor lines 37 such that any input from I/O controller 19a will cause computer 10 to wake from the sleep state. The I/O input is typically a pressing of a key on the keyboard and/or the movement of the cursor control device. The second condition for waking up computer 10 occurs if the wake up timer (alarm clock) within PMGR 11 had been enabled and matches the real time clock within PMGR 11. Upon the activation of the alarm clock, PMGR wakes computer 10 from its sleep state. Finally, the third condition of computer 10 occurs if PMGR 11 was set to monitor the detection of a ring signal from modem 25. If an incoming signal is received by modem 25, the ring signal is detected by PMGR 11 and causes computer 10 to awake from its sleep state.

Upon waking, computer 10 accesses RAM 14 to retrieve the stored state of the various units for restoring computer 10 to the state it was in prior to

entering the sleep mode. Further, upon waking, computer 10 initiates a diagnostic routine for ensuring proper operation of computer 10.

The third mode of operation of computer 10 is known as the slow mode. The slow mode is a condition similar to the active mode, except that the clock rate of the clocking signal to the various units is slowed. That is, by reducing the clock rate of computer 10, as much as 25-30% of power savings can be obtained. Although all of the clocking signals on lines 41-43 can be slowed, it is to be noted that the clock signal on each line can be slowed. Slowing the clock rate of the clocking signal on line 41 to CPU 12 can achieve 25-30% savings in power.

Furthermore, the slow mode is entered from the normal mode when no activity has been detected after a predetermined time period, this time period being less than the time period for placing the system into the sleep mode. Thus, if no activity occurs for a certain duration, computer 10 enters the slow mode first and if the non-active cycle continues, computer 10 will eventually enter the sleep mode after an additional time period.

The slow state can be entered and departed by user command or CPU command. It is appreciated that clock signals to units 20 and 21 can be decoupled by clock control unit 27, wherein units 20 and 21 are deactivated and will not lose the current internal states of those units.

Referring to Figure 2, a transistor switch 50 utilized in the clock control unit 27 is shown. It is to be appreciated that only one switch 50 is shown, however, the actual clock control unit 27 is comprised of a plurality of these switches 50. A clock signal from PMGR 11 is coupled through transistor 51 to its corresponding device 52. The control signal is also obtained from PMGR 11 and is coupled to the gate of the transistor 51. When transistor 51 is made active by the control signal, the clock signal is coupled to device 52. Typically, device 52 is a CMOS device so that when the clock signal is

removed from this CMOS device, the device shuts down and consumes none or very little power. It is to be noted that in some of the devices, such as units 20 and 21, the clock signal can be decoupled from these devices while the Vcc supply to these devices are present.

5 Referring to Figure 3, a transistor switch 54 comprising one of the switches within analog interface unit 26 is shown. However, it is to be noted that a plurality of these switches reside within analog interface unit 26. One of the Vcc lines is coupled from PMGR 11 through transistor 55 to device 56. A control line also from PMGR 11 is coupled to the gate of transistor 55 for
10 controlling the coupling of Vcc to device 56 through transistor 55. It is to be noted that power is supplied to device 56 when transistor 55 is made active and that device 56 may not necessarily be a CMOS device since power will be removed from device 56 when transistor 55 is cut off.

It is to be appreciated that the above description in reference to Figures
15 1-3 can be represented in various other circuit equivalent forms without departing from the spirit and scope of the invention. Further, in reference to Figure 1, the actual devices and the switching of the power and clock signals can be readily adapted to operate with other designs without departing from the spirit and scope of the present invention. However, in order to provide a more
20 detailed workings of the present invention, various specific details pertaining to the preferred embodiment are disclosed below. CPU 12 provides various commands to PMGR 11 for connecting the Vcc power to applicable devices as needed. Further, clock signals can be either disconnected from various devices, or in the alternative, PMGR 11 can provide different clock speeds,
25 such as during the slow mode. CPU 12 can be made to provide these commands in response to a stored routine or in response to a monitoring function of the PMGR or in response to a user interaction through I/O unit 19.

It is to be noted that the various drivers of computer 10 are responsible for powering on and off their respective peripheral devices. It is to be noted that drivers of computer 10 can be hardware or software drivers, or a combination thereof, and the preferred embodiment uses software drivers. That is, software is used to control the powering on and off the respective devices. Thus, the power to the disk control unit 20 also powers the floppy disk, the power to the parallel communications controller 23 also powers its associated peripheral device, such as the hard disk. The drivers of the serial communications controller 21 and the power to the sound drivers 24 also are controlled as needed. These drivers are responsible for maintaining the time that these devices are powered to a minimum in order to conserve power. Thus, they are only activated when a given particular device is needed. Generally, each device driver will enable its peripheral device when the driver is needed.

In the case of the floppy disk controller 20, the power is only applied to the peripheral device when an actual disk read or write is under way. Also, in the instance with the modem 25, it is kept without power until a ring is detected by PMGR 11 or when activated by the CPU 12. As stated previously those devices that have system clock inputs are enabled/disabled by controlling their connection to the clock. They can remain powered even though the rest of the system is off, thereby retaining their internal states, but consuming less power. As such, clock control devices do not need be re-initialized or re-enabled when their clock is turned off. Those devices that do not have a clock input or do not require any state to be retained are enabled/disabled by controlling their connection to power. As stated previously, the power can be removed from CPU 12 in which case the internal states of CPU 12 are stored in RAM 14 prior to power down. It is to be stressed that the clock input can be removed from CPU 12 in which case the internal states of CPU 12 are retained.

In reference to the battery charger circuit 18, the circuit charges the battery when coupled to an external power source, but circuit 18 is also utilized to monitor battery 17. PMGR 11 monitors the power level of battery 17 and alerts the user when that level drops to a predetermined level, permitting the user to finish the current job of the computer and shutting down the computer prior to complete breakdown of computer 10. An analog-to-digital converter within PMGR11 provides for the conversion of the analog battery voltage to a digital signal. Although not shown in Figure 1, a temperature sensing mechanism is also coupled to a PMGR 11 to sense the temperature and another analog-to-digital converter within PMGR 11 is also used to convert this analog signal to a digital signal.

It is to be appreciated that the PMGR 11 of the preferred embodiment of the present invention provides for a variety of techniques to monitor and control the distribution of power and clocking signals in order to conserve the time that computer 10 can be self-sustaining when decoupled from an external power source.

CLAIMS

1. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, comprising:

control means coupled to said CPU for receiving commands from said CPU and also coupled to receive inputs from said user interactive device;

said control means also coupled to said battery for controlling distribution of said power to various units of said computer;

said control means also coupled to provide an internal clock and distributing a clock signal to some of said units of said computer;

first switching means coupled to said control means for distributing said power to some of said various units, said first switching means including first switches for switching said power, said first switches being controlled by said control means;

second switching means coupled to said control means for distributing said clock signals to some of said units, said second switching means including second switches for switching said clock signal, said second switches being controlled by said control means.

2. The apparatus of Claim 1, wherein said first switching means decouples power from each of said various units coupled to said first switching means until each of said respective units are needed to be accessed by said CPU.

3. The apparatus of Claim 2, wherein said second switching means decouples said clock signal from each of various units coupled to said second switching means until each of said respective units are needed to be accessed by said CPU.

4. The apparatus of Claim 3, wherein said control means provides for three modes of operation, a first mode for providing power and clock signals to said various units when needed by said computer, a second mode for removing power or clock signal to deactivate respective devices to conserve power, and a third state in which the frequency of said clock signal is reduced in order to reduce power consumption to those units coupled to receive said clock signal.

5. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, comprising:

control means coupled to said CPU for receiving commands from said CPU and also coupled to receive inputs from said user interactive device;

said control means also coupled to said battery for controlling distribution of said power to various units of said computer;

said control means also coupled to provide an internal clock and distributing a clock signal to some of said units of said computer;

said control means providing for three modes of operation of said computer, an active mode for providing active operation of said computer, a sleep mode for placing said computer in an inactive state to conserve power and a slow mode in which the frequency of said clock signal is reduced in

order to reduce power consumption to those units coupled to receive said clock signal:

first switching means coupled to said control means for distributing said power to some of said various units, said first switching means including first switches for switching said power, said first switches being controlled by said control means;

second switching means coupled to said control means for distributing said clock signals to some of said units, said second switching means including second switches for switching said clock signal, said second switches being controlled by said control means;

monitoring means for monitoring said various units and providing information of monitored units to said control means.

6. The apparatus of Claim 5, wherein said first switching means decouples power from each of said various units coupled to said first switching means until each of said respective units are needed to be accessed by said CPU.

7. The apparatus of Claim 6, wherein said second switching means decouples said clock signal from each of various units coupled to said second switching means until each of said respective units are needed to be accessed by said CPU.

8. The apparatus of Claim 7, wherein prior to entering said sleep mode said apparatus stores CPU states in said memory and retrieves said CPU states from said memory when reactivated to said active mode.

9. The apparatus of Claim 8, wherein said computer enters its sleep mode if an input from an input/output (I/O) device does not occur for a first predetermined time period.

10. The apparatus of Claim 9, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from said I/O device.

11. The apparatus of Claim 10, wherein said computer enters its slow mode if said input from said I/O device does not occur for a second predetermined time period, said second predetermined time period being shorter than said first predetermined time period.

12. The apparatus of Claim 11, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from a modem coupled to said control means.

13. The apparatus of Claim 12, wherein said I/O device is said user interactive device.

14. The apparatus of Claim 10, wherein said first and second switches are field-effect transistors.

15. The apparatus of Claim 14 further including a reference clock means coupled to said control means for providing a crystal controlled reference clock signal.

16. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, substantially as hereinbefore described with reference to the accompanying drawings.



PCT

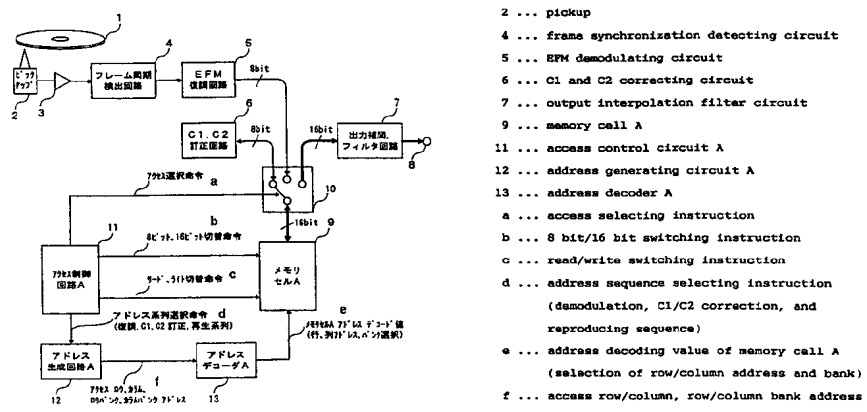
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<p>(21) 国際出願番号 PCT/JP97/00910</p> <p>(22) 国際出願日 1997年3月19日(19.03.97)</p> <p>(71) 出願人 (米国を除くすべての指定国について) 株式会社 日立製作所(HITACHI, LTD.)(JP/JP) 〒101 東京都千代田区神田駿河台四丁目6番地 Tokyo, (JP)</p> <p>(72) 発明者 ; および (75) 発明者 / 出願人 (米国についてのみ) 平山洋志(HIRAYAMA, Hiroshi)(JP/JP) 〒245 神奈川県横浜市泉区新橋町728番1号 Kanagawa, (JP) 竹内敏文(TAKEUCHI, Toshifumi)(JP/JP) 〒244 神奈川県横浜市保土ヶ谷区峰沢町307番2号 Kanagawa, (JP) 永井 裕(NAGAI, Yutaka)(JP/JP) 〒245 神奈川県横浜市泉区中田町643番1号 Kanagawa, (JP) 川前 治(KAWAMAE, Osamu)(JP/JP) 〒245 神奈川県横浜市泉区岡津町2580番5号 Kanagawa, (JP) 星沢 拓(HOSHIZAWA, Taku)(JP/JP) 〒251 神奈川県藤沢市辻堂5977番1号 Kanagawa, (JP) 赤星健司(AKAHOSHI, Kenji)(JP/JP) 〒244 神奈川県横浜市戸塚区戸塚町3514番 Kanagawa, (JP)</p>	<p>(74) 代理人 弁理士 小川勝男(OGAWA, Katsuo) 〒100 東京都千代田区丸の内一丁目5番1号 株式会社 日立製作所内 Tokyo, (JP)</p> <p>(81) 指定国 CN, JP, KR, US, 欧州特許 (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>添付公開書類 国際調査報告書</p>
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(54)Title: DEVICE AND METHOD FOR REPRODUCING DIGITAL SIGNAL USING VARIABLE BUS-WIDTH MEMORY AND DEVICE AND METHOD FOR RECORDING DIGITAL SIGNAL

(54)発明の名称 バス幅可変メモリを用いたデジタル信号再生装置、再生方法及び記録装置、記録方法



(57) Abstract

Digital data are stored in a memory means in prescribed arranging order and, when a data arrangement to be corrected for an error contained in the arrangement or a data arrangement to be produced is read out, the control of the access to the memory means is made easier, the number of accesses to the memory means is reduced and a data transfer speed is increased to thereby reduce the power consumption when using a semiconductor chip containing the memory means. The memory means which can switch the access bit width between (n) bits and (n x m) bits (n and m: natural numbers), a bus width switching means which can switch the memory access bit width between the (n) and (n x m) bits, and a control means which controls the access are provided. Since the control means controls the access so that the bus width can be switched to the (n x m) bit width at the time of reading out the data arrangement to be reproduced from the memory means, the number of accesses is reduced and the transferring speed of reproduced data is improved. When the memory means which can be changed in access bit width, a means required for the execution of processing, etc., are provided on the same semiconductor chip, the memory means is customized so that the access bit width can be variably set in accordance with each required means.

明 細 書

バス幅可変メモリを用いたデジタル信号再生装置、再生方法及び記録装置、記録方法

技術分野

- 5 本発明はデジタル信号再生装置、再生方法及び記録装置、記録方法に関し、特に一時的にデータを記憶するメモリ手段に対するアクセスにより、デジタル信号を所定の配列にならべ、ならべられた配列に対し、誤り訂正等所定の処理を実行するためのデータ系列の読み出し、及び所定の処理が終了したデータ系列の読み出しを行うことで、デジタル信号
- 10 号に対する再生処理、或は記録処理を行うデジタル信号再生装置、再生方法及び記録装置、記録方法に関する。

背景技術

- 従来、この類のデジタル信号再生装置、再生方法の一例としてCD
- 15 (Compact Disc)が挙げられる。このCDは、「CD-オーディオからパソコンへ 真利藤雄 監修、林 謙二編著 コロナ社 p 13 ~ p 14」に記載の技術のように、標本化された16ビットオーディオデータに対し、上位、下位それぞれ8ビット(1シンボル)単位に分割し複数のシンボルデータで1フレームを構成した後、誤り訂正符号としてC2訂正
- 20 符号付加、フレーム間でのインターリーブ、C1訂正符号付加、サブコード付加を行った後、1シンボル8ビット単位のデータを14ビット単位のデータに変調するEFM(Eight to Fourteen Modulation)と呼ばれる変調が行われ、ディスクへの記録周波数を下げる為のマージン3ビットを付加する。最後にマージンビットを含む合計17ビット単位のデ

ータを複数集めた物に対して同期信号を付加した後の信号をディスクに記録する。

再生の際にはディスクから読み取られた信号に対し、上記とは逆の順番で復調処理、C1、C2訂正符号の復号による誤り訂正処理、インターリーブ処理を実行することにより元のオーディオデータに対する再生データが得られる。

再生装置におけるメモリ手段に対してはシンボル単位のアクセスを行い、復調データの書込み、誤り訂正を行う対象の復調データの読み出し、時系列的に連続した順番で再生データの読み出しを行う事により再生が行われる。

上記した従来技術は、再生データを得る為に、誤り訂正等所定の処理を行う論理回路と、データを一時的に記憶し読み書きが自由なメモリ(RAM: Random Access Memory)が用いられる。この場合メモリに対しては、復調データ系列のフレーム書込み、C1訂正系列のフレーム読み出し、C2訂正系列のフレーム読み出し、再生データ系列のフレーム読み出しと、所定の各処理に応じたシンボル単位のメモリアクセスが必要である。

メモリアクセス時には、インターリーブ遅延を考慮して処理対象のデータ系列にアクセスしなければならず、メモリに対するアドレス制御、管理が複雑となり、アドレス制御を行う論理回路が複雑となる問題がある。

また、メモリに対する全てのアクセスはシンボル単位で行われる為、全てのアクセスに対するメモリアドレスを指定しなければならずメモリアクセス回数が増加するという問題がある。

この場合、特に高速で論理回路とメモリが動作する場合の消費電力が大きくなるという問題、メモリアクセス回数増加の為、本来メモリが持

つアクセス性能を活かせなくなり、再生データを読み出す際のデータ転送レートが低下するという問題が有る。

更に上記した論理回路とメモリを同一の半導体チップ上に設けた場合も同様の問題が生ずる。

5 また、最近は大規模、安価で一定時間間隔でリフレッシュが必要なD R A M (Dynamic Random Access Memory) を大規模な論理回路と共に同一の半導体チップ上に混載可能な半導体技術が開発された。このD R A M混載技術を用いて上記した処理を論理回路とD R A Mで実現した場合、アクセス回数を減少させないと、特に高速動作時の半導体チップ全体の
10 消費電力が大きくなるという問題が有る。

一方、近年開発が進んでいるD V Dにおいて、そのデジタル信号処理は、大容量のメモリと大規模な論理回路が必要である。大容量メモリの点でD R A Mが有利であり、高速でこの大容量メモリにアクセスしデジタル信号処理を行うためには、上記したD R A M混載技術でD R A M
15 Mと論理回路を同一の半導体チップ上に設けて実現する事が必須となる。この場合もメモリアクセス回数、高速動作の点で半導体チップ全体の消費電力の問題が顕著に現れる。

従って本発明の目的は、メモリにアクセスする際のアドレスを容易に制御でき、かつメモリアクセス回数を減少させると共に、転送データの
20 転送速度を向上させる事が可能なデジタル信号再生装置、再生方法及び記録装置、記録方法を提供するものであり、同一の半導体チップ上に処理手段とメモリとを設けた際に、半導体チップ全体の消費電力の低減を実現すると共に、デジタル信号処理を高速で処理し、データの高速転送を実現する半導体チップ上のデジタル信号処理システムを提供す
25 るものである。

発明の開示

上記問題を解決するための、少なくとも、記録媒体からの読取り信号を復調し、復調データを n ビット単位で出力する復調処理手段と、誤り訂正処理に対するデータ配列に対し、 n ビット単位で処理を行う誤り訂正処理手段と、再生データのデータ配列に対し、 $n \times m$ ビット単位で処理を行う出力処理手段と、メモリ手段のデータバスに対し、上記手段のデータバスを選択的に接続する接続手段と、上記各処理手段それぞれの処理に必要なデータ配列のアクセスに必要なアドレスを生成する手段と、生成されたアドレスをメモリ手段上の実際のアドレスにデコードする手段と、メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、メモリ手段は、アクセスビット幅が n ビットと $n \times m$ ビットに切替えてアクセス可能なバス幅可変手段を有し、メモリ手段にアクセスを行う制御手段を設け、その制御手段は、上記 $n \times m$ ビット単位で出力処理手段への転送データの読み出しを行う際に、 $n \times m$ ビットのバス幅とすることで行う。

これにより、メモリのアクセス回数を減少させると共に、データの転送速度の向上が図れる。

また、これらアクセスビット幅が可変なメモリ手段と、接続手段、メモリの制御手段、処理手段を同一の半導体チップ上に設ける際には、可変なアクセスビット幅の種類（ n ビット幅と $n \times m$ ビット幅）に対応したアクセスビット幅のカスタマイズが行われ、アクセスビット幅を可変に設定できるメモリ手段が半導体チップ上に設けられ、大容量のメモリ手段が半導体チップ上に必要な場合は一定時間でリフレッシュ動作の必要なダイナミックなメモリをメモリ手段として用いる。

D R A M混載技術により、論理回路及び同一の半導体チップ上に設けられるメモリは、デジタル処理を行うのに必要なアクセスビット幅及

び記憶容量に応じて自由に構成することが可能となる。すなわち、所定の処理に必要なそれぞれの論理回路を処理効率の点から有利なように構成でき、それぞれの論理回路に必要なアクセスビット幅に合わせてアクセスが可能なメモリが構成できるようになる。

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図面の簡単な説明

第1図は、本発明による第1の実施形態の構成を示すブロック図である。

10 第2図は、第1図の実施形態におけるメモリセルAのアクセス制御の過程を示すフローチャートである。

第3図は、出力補間、フィルタ処理までに必要な各処理のアクセス系列、メモリセルAのアドレス制御方法を示す図である。

第4図は、8ビット、16ビットとアクセスビット幅が可変なメモリセルAの一構成例を示すブロック図である。

15 第5図は、第1図に示した実施形態における光ディスク1に記録されるデータのフレーム構造を示す図である。

第6図は、第1図に示した実施形態におけるで光ディスク1からの復調後のシンボルデータに対し、各処理におけるフレーム間遅延を示す図である。

20 第7図は、本発明による第2の実施形態の構成を示すブロック図である。

第8図は、第7図の実施形態におけるメモリセルBのアクセス制御の過程を示すフローチャートである。

25 第9図は、第7図に示した実施形態でメモリセルAから読みだされたデータで構成される1セクタの構成を示す図である。

第10図は、第7図に示した実施形態で、インターフェイス回路への

データ転送までに必要な各処理のアクセス系列、メモリセルBのアドレス制御方法を示す図である。

第11図は、本発明による第3の実施形態の構成を示すブロック図である。

5 第12図は、8、32ビットとアクセスビット幅が可変なメモリセルCの一構成例を示すブロック図である。

第13図は、第11図に示した実施形態で、インターフェイス回路へのデータ転送までに必要な各処理のアクセス系列、メモリセルCのアドレス制御方法を示す図である。

10 第14図は、第11図の実施形態におけるメモリセルCのアクセス制御の過程を示すフローチャートである。

第15図は、本発明による第4の実施形態の構成を示すブロック図である。

15 第16図は、第15図の実施形態におけるメモリセルCのアクセス制御の過程を示すフローチャートである。

第17図は、本発明の第5の実施形態の構成を示すブロック図である。

発明を実施するための最良の形態

以下、本発明の実施の形態を図面を用いて説明する。

20 第1図は本発明の第1の実施形態に関する再生装置及び再生方法の構成を示すブロック図である。同図において、参照数字1は記録する16ビットデジタルオーディオ信号に対し、所定のフォーマットでエンコードを行ったデジタル信号を記録した光ディスク、2は光ディスク1に記録された信号を読み取るピックアップ、3はプリアンプ、4は光ディスク1から読みだされた信号より構成されるフレームの先頭を示す同期信号の検出を行うフレーム同期検出回路、5は変調されて記録された光

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ディスク 1 からの読み出し信号を元の 8 ビット、1 シンボル単位のデータに復調する E F M 復調回路、6 はディスク読み出し時に発生したエラーに対し信号中に付加された訂正符号の復号を行い信号内に存在するシンボル単位のエラー訂正を行う C 1、C 2 訂正回路、7 は 16 ビット、

5 2 シンボル単位で処理を行い、訂正不能と判断された際には再生データの補間を実行、フィルタ処理を行う出力補間、フィルタ回路、8 は出力端子、9 はアクセスビット幅を 8 ビット、16 ビットと可変にアクセスでき、8 ビット単位でアクセスするメモリバンクを 2 面持つメモリセル A、10 はメモリセル A にアクセスする対象を制御し、8 ビットアクセスの場合、メモリセル A の 16 ビットデータバスの下位 8 ビットとアクセスする対象の 8 ビットデータバスをダイレクトに接続し、16 ビットアクセスの場合はメモリセル A の 16 ビットデータバスをそのままダイレクトに接続するセクタ A、11 はメモリセル A のアクセス対象の選択を制御するアクセス選択命令、メモリのリード、ライト切替命令、

15 8 ビット、16 ビット切替命令、メモリセル A にアクセスする際のアドレス系列（復調系、C 1、C 2 訂正系、再生系）選択命令をそれぞれ生成するアクセス制御回路 A、12 はアドレス系列選択命令に従い、アクセスを行うアドレスを生成するアドレス生成回路 A、13 は生成されたアドレスをメモリセル A のアドレスにデコードするアドレスデコーダ A

20 である。

第 1 図において、光ディスク 1 に記録されている再生されるべきデジタルオーディオ信号がピックアップ 2 から読みだされ、読みだされた信号中に含まれるフレーム同期信号検出を 4 のフレーム同期検出回路 4 で行う。

25 ここで第 5 図により光ディスク 1 に記憶されるデジタル信号の処理単位であるフレームの構造、第 6 図により再生データを得る為に必要な

処理について説明する。

第5図に示すように、光ディスク1に記録する単位であるフレーム501の構成は、フレームの先頭を示す同期信号502と、そのフレームについての再生時間情報などを記録したサブコード503、フレームデータ504により構成される。フレーム同期信号の検出、EFM復調処理を行った後のサブコード、フレームデータは8ビットを1シンボルとした単位で構成され、フレームデータはデータ24シンボル、C1、C2訂正符号各4シンボル、合計32シンボルで構成される。元のオーディオ再生データを得る為には第6図に示すように復調処理を行ったフレームに対して、フレーム番号順に複数ならべたフレーム系列に対し（図中601）、C1訂正は奇数番号のシンボルデータを1フレーム分遅延した図中602に示す様なフレーム系列に対して行う。C2訂正はシンボル毎に4フレーム遅延が増加、最大108フレーム遅延までのフレーム系列（図中603）の $32 - 4 = 28$ シンボルに対して行い、再生データはC2訂正を終了したフレーム系列内の0～11までのシンボル番号の系列604と、2フレーム分遅延したC2訂正フレーム系列内の16～27までのシンボル番号の系列605からなる。

以上のような各系列のフレームデータに対する各処理を第1図で行い、出力補間、フィルタ回路7への再生データ読み出しを2シンボル（1ワード）単位で容易に行う為のシンボルデータの配置、及びメモリアドレス制御の方法を第3図を用いて説明する。

第3図において、304、305は再生データの読み出し制御を容易にかつ、アクセス単位を1ワードとする事が可能なシンボル単位のデータの配置例であり、304は第 $(n - 3)$ フレーム目の0～11シンボル目までの再生データ系列、305は第 $(n - 3)$ フレーム目の16～27シンボル目までの再生データ系列である。このような配置で再生デ

ータ系列を構成しようとする、C 2 訂正系列は第 6 図で説明した C 2 訂正系列 6 0 3 と再生系列 6 0 4、6 0 5 で示した関係のフレーム遅延で与えられるので、再生データ系列中の 0 ~ 1 5 シンボルと、2 フレーム遅延した再生データ系列の 1 6 ~ 2 7 シンボルとなる。従ってこの場合の再生系列に対する C 2 訂正系列は、3 0 3 の様に 1 列に並ぶ配置になる(第 3 図中、3 0 3 は第 (n - 1) フレーム目の C 2 訂正系列を示す)。C 2 訂正系列は C 1 訂正系列に対し最大フレーム遅延 1 0 8 フレームで、1 シンボル毎に 4 フレーム遅延が増加するので、3 0 3 の C 2 訂正系列に対し、C 1 訂正系列は 3 0 2 の様な配置になる。(図中 3 0 2 は (n - 1) フレーム目の C 1 訂正系列を示す)。更に C 1 訂正系列は、復調系列に対して奇数シンボル番号が 1 フレーム遅延されるので、復調系列は 3 0 1 の様な配置になる(図中 3 0 1 は n フレーム目の復調系列を示す)。以上の各系列のシンボル配置をメモリでアクセス際のアドレス制御方法は、アドレス制御を容易に行う為、例えば横方向に 1 6 シンボル、縦方向に 4 個の 6 4 バイトをアドレス制御の 1 単位、1 バンクとし(図中 3 0 6) アドレス制御の際の基本単位としている。3 0 7 は 1 バンクの縦方向のアドレスを示すカラムアドレス、3 0 8 は横方向のアドレスを示すロウアドレスである。更にバンク単位のアドレス制御を行う為、カラムバンクアドレス 3 0 9、ロウバンクアドレス 3 1 0 が与えられる。アクセスする際にはロウバンク、カラムバンクアドレスと、バンク内のロウ、カラムアドレスを指定してアドレス制御を行い、再生データ系の読み出しの際には、2 シンボル構成のワード単位の最初のシンボルに対するアドレスを指定して、1 ワード単位のアクセスを行う(図中 3 1 1)。

第 3 図で説明したアドレス制御方法を用い、第 1 図の再生装置において再生データを得るまでの処理の流れを第 2 図のフローチャートを併せて用いて説明する。

第1図において、アクセス開始命令に従い光ディスク1から信号の読み出しが開始されると、11のアクセス制御回路Aは、10のセクタA、9のメモリセルA、12のアドレス生成回路Aそれぞれの制御対象に対し各制御命令を生成する。10のセクタAはアクセス選択命令に従い5のEFM復調回路からの8ビットデータバスとメモリセルAの16ビットデータバスの下位8ビットに接続、9のメモリセルAは8ビット、16ビット切替命令に従い、シンボル単位の復調データをライトする為、アクセスビット幅を8ビットに設定、リード、ライト切替命令に従いライトを選択し、12のアドレス生成回路Aはアドレス系列選択命令に従い、復調系列のアドレスを生成するように設定される（ステップ201）。メモリセルAへのアクセス準備が完了するとEFM復調処理が開始され、12のアドレス生成回路Aは第3図で説明したアドレスの指定方法に従い、復調系列のロウ、カラムアドレス、ロウバンク、カラムバンクアドレスを1シンボルライト毎に生成、13のアドレスデコーダAでメモリセルAのアドレスにデコードされ1シンボル毎にメモリセルAにライトされる（ステップ203）。

ここでアクセスビット幅が8、16ビットと可変な10のメモリセルAについて説明する。第4図はメモリセルAの構成例で、8ビット単位でアクセス可能な2つのメモリバンク401と402を持ち、行方向、列方向のアドレスを指定する事でメモリバンクへのアクセスが可能となっている。403はバンク切替用のセクタでバンク選択信号に従い8ビット単位アクセスのメモリバンク選択が可能である。404は8ビット、16ビット切替命令に従い、メモリバンク1の8ビットバスを上位8ビット、メモリバンク2の8ビットバスを下位8ビット、合計16ビットデータをして扱う場合と、セクタ403で選択されたメモリバンク1または2の8ビットデータを下位8ビットとし、リード時、上位8

ビットのデータとして“0”を加え16ビットデータとした物の選択を行うセクタである。405はリード、ライト切替命令に従い、データの転送方向を決定するI/Oバッファである。このような構成でメモリセルAは構成され、アクセスビット幅の切替が可能になる。なお、物理的にバスを切り替える代わりに、物理的にはすべてのバスが接続されているがその時に使用するバス幅分のバスのみを有効にする構成としても構わない。

C2訂正可能な復調フレームのライトが終了したと判断されると(ステップ204)、アクセス制御回路Aは各制御対象に対しC1訂正系列のフレームをメモリセルAからリードする為の命令を生成する。セクタAはC1、C2訂正回路にC1訂正系列のシンボルデータをリード可能な様にC1、C2訂正回路への8ビットデータバスとメモリセルAの16ビットデータバスの下位8ビットを接続、メモリセルAはリードを選択、アドレス生成回路AはC1訂正系列のアドレスを生成するように設定される(ステップ205)。C1訂正処理の為のメモリアクセス選択が終了すると、アドレス生成回路AはC1訂正系列のロウ、カラム、ロウバンク、カラムバンクアドレスを1シンボルリード毎に生成、アドレスデコーダAでメモリセルAのアドレスにデコードされ1シンボル毎にC1訂正系列データがメモリセルAからリードされ(ステップ206)、リードされたC1訂正系列のフレームに対して系列中に発生したエラーの訂正が実行される(ステップ207)。

C1訂正系列の処理が終了すると、アクセス制御回路Aは各制御対象に対してC2訂正系列のフレームをメモリセルAからリードする為の命令を生成する。アドレス生成回路AはC2訂正系列のアドレスを生成するように設定され(ステップ208)、C2訂正系列のロウ、カラム、ロウバンク、カラムバンクアドレスを1シンボルリード毎に生成、アド

レスデコーダ A でメモリセル A のアドレスにデコードされ 1 シンボル毎に C 2 訂正系列データがメモリセル A からリードされ (ステップ 2 0 9)、リードされた C 2 訂正系列のフレームに対して系列中に発生したエラーの訂正が実行される (ステップ 2 1 0)。

5 C 2 訂正系列の処理が終了すると、アクセス制御回路 A は各制御対象に対して再生データ系列を 1 ワード (2 シンボル) 単位でメモリセル A からリードする為の命令を生成する。セクタ A は 1 ワード単位で処理を行う出力補間、フィルタ回路 7 への 1 6 ビットデータバスとメモリセル A の 1 6 ビットデータバスを接続、出力補間、フィルタ回路 7 への 1
10 ワード単位のデータ転送を可能にし、メモリセル A はアクセスビット幅を 1 6 ビットに選択、アドレス生成回路 A は再生データ系列のアドレスを生成するように設定 (ステップ 2 1 1)、リードの単位である 2 シンボルデータの中で最初にアクセスを行うのロウ、カラム、ロウバンク、カラムバンクアドレスを 1 ワードリード毎に生成し、アドレスデコーダ A
15 でメモリセル A のアドレスにデコードし再生データをリードする (ステップ 2 1 2)。リードされた再生データは 7 の出力補間、フィルタ回路において、訂正不能の場合は補間処理が行われ、フィルタ処理後、出力端子 8 より出力される。再生を継続する場合には、ステップ 2 0 1 から処理を再開する (ステップ 2 1 3)。

20 第 1 の実施形態の例において、光ディスク 1 から読み取られ、デジタル化されたシリアルデータに対する復調方法が、シリアルデータに同期して送られてくるビットクロック 1 7 個分のシリアルデータ (復調データ 1 4 ビットとマージン 3 ビット単位でシリアル転送される) から 8 ビット単位の平行データに E F M 復調回路で変換される場合、シ
25 アルデータの転送回数を示すビットクロック数と、出力補間、フィルタ回路へ 1 6 ビット単位でデータ転送を行う際のメモリのアクセス回数と

の関係は、アクセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が100%とすると、ビットクロック(17+17)個に対して、8ビットで書き込まれたメモリから16ビットのデータ量のデータ転送が1回で行われるので34:1となり、また、冗長度が0の場合17:1の関係となる。よって、一般的に冗長度は100%より小、0%より大であるので、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/34 < F_o < 1/17$ となる。

これに対して、出力補間、フィルタ回路へのデータ転送が1回につき8ビット単位であれば、同じ16ビットのデータ量を転送するのに2回の転送が必要となり、上記と同様の条件の場合、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/68 < F_o < 1/34$ となり、アクセスビット幅可変なメモリを用いた場合よりもデータの転送効率が低下する。

以上のように本発明の第1の実施の形態においては、光ディスクから読みだされた信号に対し同期信号の検出、復調処理後のシンボル単位のデータ書込みから、再生データの読み出しを行うまでの処理に対するアドレス制御を、まとまった複数シンボル単位で1バンクを構成、1バンク中のロウ、カラムアドレスと、バンクに対するロウ、カラムアドレスを指定してアクセス制御を行う事によりアドレス制御が容易となる。

また、アドレス制御を行う際の再生データ系列の配置を工夫する事により、2シンボル単位でアクセス、データリードが可能となり、再生データに対する出力処理を2シンボル単位で行う事ができる。

また、再生データ系列の読み出しの際のメモリセルAのアクセスビット幅を16ビット、リード単位を1ワード単位で行える為、メモリアクセス回数が減少し、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルA、各処理回路、制

御回路を同一の半導体チップ上に設けた場合でもメモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第7図は本発明による再生装置及び再生方法の第2の実施の形態を示すブロック図であって、参照数字1はホストコンピュータで処理を行うデジタルデータが記録された光ディスク、14はメモリセルAから1ワード単位でリードされた再生データで構成されるセクタの先頭を検出するセクタ同期信号検出回路、15は1セクタ内に含まれる訂正符号の復号によりセクタ中に発生したエラーの訂正を行うP、Q訂正回路、16はホストコンピュータと再生装置の間で2ワード(32ビット)単位のデータ転送を行うインターフェイス回路、17はアクセスビット幅が1ワード(16ビット)、2ワード(32ビット)と可変にアクセス可能で第4図に示したメモリセルAの構造においてメモリバンク1、2を16ビット単位でアクセスするメモリバンクに変更し、それ以外の部分を32ビット化したメモリセルB、31は1セクタ中に記録され光ディスク1でのセクタの存在する位置を示すセクタIDを検出、検出したセクタIDとホストコンピュータからのアクセス命令に含まれる転送開始セクタIDの一致を検出、一致検出結果を19のアクセス制御回路Bに出力するセクタID検出回路、18はメモリセルBにアクセスする対象を制御する際に、16ビットアクセスの場合は、メモリセルBの32ビットデータバスの下位16ビットとアクセスする対象の16ビットデータバスをダイレクトに接続し、32ビットアクセスの場合はメモリセルBの32ビットデータバスをそのままダイレクトに接続するセレクタB、19はメモリセルBのアクセス選択命令、リード、ライト切替命令、16ビット、32ビットアクセスビット幅の切替命令、メモリセルBのアドレス系列(セクタデータ系、P、Q訂正系、ホスト転送系)の選択命令を生成するアクセス制御回路B、20はアドレス系列選択命令に従い、

各系列の1ワード単位のデータに対するアドレスを生成するアドレス生成回路B、21は生成されたアドレスをメモリセルBのアドレスにデコードするアドレスデコーダBであり、第1図と共通の部分については同一の参照数字をつけて説明を省略する。

5 同図において、インターフェイス回路16がホストコンピュータからのアクセス命令を受付けると、ピックアップ2により光ディスク1に記録されている信号が読み取られ、第1図を用いて説明した動作に従い1ワード単位の再生データがメモリセルAよりリードされセクタ同期検出回路14に送られる。

10 ここで第9図を用いてメモリセルAからリードされる1ワード単位の再生データで構成される1セクタ構造を、第10図を用いて20のアドレス生成回路Bにおけるアドレス制御について説明する。

第9図において、メモリセルAからリードされ構成される1セクタ901の構成はセクタの先頭を示す12バイトのセクタ同期信号902と、
15 セクタの存在する光ディスク上のアドレス等の情報を格納した4バイト(2ワード)のセクタID、ホストコンピュータに転送を行うべきユーザデータ904、セクタ中に発生したエラーの訂正を行う為の288バイトのP、Q訂正符号で構成される。このような構成のセクタに対し、セクタ同期信号の検出を行った残りのデータ(906のワード単位の時
20 系列通し番号0~1169)に対するアドレス制御は、第10図に示すように、まず1ワード単位で時系列番号順に図の様にならべ、誤りの訂正を行う際には、P訂正系列10Aの縦方向の系列に対して行い、Q訂正系列10Bの斜め方向の系列に対して行う。ホストコンピュータにデータ転送する際にはワード単位の時系列通し番号2~1031を転送、
25 転送の単位は10Cに示すように2ワード(32ビット)で行われる。これらの各処理のデータ系列に対してアドレス制御を行う際には、図中

10 Dのロウアドレス、10 Eのカラムアドレスを指定して行い、インターフェイス回路へデータの転送を行う際には、2ワード単位の最初に転送を行うワードデータに対するアドレスを指定し、アドレス制御を行う。

- 5 第7図において、第10図に示したセクタデータのアドレス制御方法でメモリアクセス制御を実行、インターフェイス回路を介しホストコンピュータへ2ワード単位のデータ転送を行う様子を第8図のフローチャートを併せて用い説明する。

第7図、第8図において、インターフェイス回路16にホストコンピュータからのアクセス命令が受けられると、光ディスク1から信号の読み出しが開始され、メモリセルAにおけるアクセスで各処理を行い、1ワード単位のセクタデータがリードされる(ステップ801)、14のセクタ同期検出回路において、リードされたセクタデータに含まれるセクタ同期信号の検出後、1セクタ中に含まれるセクタIDの検出を31のセクタID検出回路で行う(ステップ812)。ホストコンピュータのアクセス命令にはデータ転送を開始する転送開始セクタIDが含まれており、この転送開始セクタIDと検出セクタIDの一致を検出すると、19のアクセス制御回路Bによる各制御対象に対する設定が開始され、一致しなければセクタIDの一致検出を継続する(ステップ802)。

20 セクタIDの一致検出に従い19のアクセス制御回路Bは18のセクタB、17のメモリセルB、20のアドレス生成回路Bの各制御対象に対し、転送開始セクタIDからのセクタデータをメモリセルBにライトする為の命令を生成、セクタBはアクセス選択命令に従いセクタ同期検出回路14からの1ワードデータバスとメモリセルBの2ワードデータバスの内下位1ワードとを接続、メモリセルBは16ビット、32ビット切替命令に従い、ワード単位(16ビット)で同期検出後のセク

タデータをライトする為、アクセスビット幅を16ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路Bはアドレス系列選択命令に従いセクタデータ系のアドレスを生成するように設定される（ステップ802）。メモリセルBへのアクセス準備が完了する
5 とセクタ同期信号の検出後のセクタデータが1ワード単位で送られ、アドレス生成回路Bは第10図に示したセクタデータのアドレス制御方法に従いロウアドレス、カラムアドレスを1ワードライト毎に生成、21のアドレスデコーダBでメモリセルBのアドレスにデコードされ1ワード毎にメモリセルBにライトされる（ステップ803）。

10 メモリセルBの記憶容量分まで1セクタ単位のセクタデータのライトが行われると（ステップ804）、アクセス制御回路Bは各制御対象にたいしてP訂正系列をメモリセルBからリードする為の命令を生成する。セクタBはP、Q訂正回路への1ワードデータバスとメモリセルBの下位1ワードデータバスとを接続、メモリセルBはリードを選択、アドレス生成回路BはP訂正系列のロウ、カラムアドレスを生成するように
15 設定される（ステップ805）。P訂正系列に対するメモリアクセス選択が終了すると、アドレス生成回路Bは1ワードリード毎にP訂正系列のアドレスを生成、アドレスデコーダBでメモリセルBのアドレスにデコードされ1ワード毎にP訂正系列データがメモリセルBからリードさ
20 れる。リードされたP訂正系列に対して系列中に発生したエラーの訂正が実行される（ステップ806）。

 P訂正系列の処理が終了すると、アクセス制御回路Bは各制御対象に対してQ訂正系列をメモリセルBからリードする為の命令を生成する。アドレス生成回路BはQ訂正系列のアドレスを生成するように設定され
25 （ステップ807）、Q訂正系列のロウ、カラムアドレスを1ワードリード毎に生成、アドレスデコーダBでメモリセルBのアドレスにデコー

ドされ1ワード毎にQ訂正系列データがメモリセルBからリードされる。リードされたQ訂正系列に対して系列中に発生したエラーの訂正が実行される(ステップ808)。

5 Q訂正系列の訂正処理が終了すると、アクセス制御回路Bは各制御対象
に対してホスト転送データ系列をメモリセルBからリードする為の命令
を生成する。セクタBはインターフェイス回路16への2ワード幅デ
ータバス(32ビット)とメモリセルBの2ワードデータバスを接続し、
メモリセルBはアクセスビット幅を32ビットに選択、アドレス生成回
路Bはホスト転送データ系列のアドレスを生成するように設定され(ス
10 テップ809)、2ワード単位のホスト転送データ系列の最初の1ワー
ドに対する ROW、カラムアドレスを2ワードリード毎に生成、2ワード
単位のデータの最初のワードに対する ROW、カラムアドレスを指定する。
アドレスデコードBは生成された2ワード単位の先頭アドレスをメモリ
セルBのアドレスにデコードし、1回のアクセスにつき2ワード単位で
15 リード、インターフェイス回路16に転送(ステップ810)、インタ
ーフェイス回路は2ワード単位でホストコンピュータへデータの転送を
行う。ホストコンピュータからの転送要求セクタ数に満たない場合(ス
テップ811)、ステップ802から処理を繰返し、要求セクタ数に達
したのであれば、処理を終了する。

20 この第2の実施形態において、光ディスク1から読み取られ、ディジ
タル化されたシリアルデータに対する復調方法が、シリアルデータに同
期して送られてくるビットクロック17個分のシリアルデータ(復調デ
ータ14ビットとマージン3ビット単位でシリアル転送される)から8
ビット単位の平行データにEFM復調回路で変換される場合、シリ
25 アルデータの転送回数を示すビットクロック数と、インターフェイス回
路から32ビット単位でデータ転送を行う際の転送回数との関係は、ア

クセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が100%とすると、ビットクロック(17+17)個に対して、8ビットで書き込まれたメモリから32ビットのデータ量のデータ転送が1回で行われるので34:1となり、また、冗長度が0の場合
5 17:1の関係となる。よって、一般的に冗長度は100%より小、0%より大であるので、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/34 < F_o < 1/17$ となる。

これに対して、インターフェイス回路からのデータ転送が1回につき16ビット単位であれば、同じ32ビットのデータ量を転送するのに2
10 回転送が必要となり、上記と同様の条件の場合、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/68 < F_o < 1/34$ となる。

更にインターフェイス回路からのデータ転送或は、メモリ手段からインターフェイス回路へのデータ転送が8ビット単位で行われるのであれば、32ビットのデータ量を転送するのにインターフェイス回路からの
15 転送或はメモリアクセスが4回必要となり、上記と同様の条件の場合、ビットクロック(17+17)×4個につき32ビットのデータ量の転送を行う事になるので(136~68):1の関係となり、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/136 < F_o < 1/68$ となり、データ転送効率が著しく低下する。従ってこの実施の形態に
20 においては、メモリセルAからリードされた1ワード単位のデータで構成されるセクタに対する必要な処理を行い、インターフェイス回路を通じてホストコンピュータにデータ転送を行う際には、2ワード単位で行う事が可能となるので、ホストコンピュータへのデータの転送速度が向上する。

25 また、メモリセルA、メモリセルBのアクセス回数が減少するので、上記した複数のセクタを一時的に記憶するのに必要な大容量のメモリセ

ルBを含む、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルA、メモリセルB、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、ホストコンピュータにデータ転送を行う際には、2ワード単位で行う事が可能となりデータ転送速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第11図は本発明によるの再生装置及び再生方法の第3の実施の形態を示すブロック図であって、参照数字1はホストコンピュータで処理を行うデジタルデータが記録され、第1図、第7図における光ディスクとは異なる変調方式、エンコード方法で記録した光ディスク、23は光ディスク1に記録された異なる変調方式の信号に対し元の8ビット単位のデータに復調するデータ復調回路、24は復調後の複数のセクタ単位のデータで構成される訂正ブロック単位で、光ディスクからの読み出しの際にブロック内に発生したエラーの訂正を行うPI, PO訂正回路、26はアクセスビット幅が8ビット、32ビットと可変にアクセス可能なメモリセルC、27はメモリセルCにアクセスする対象を制御し、8ビットアクセスの場合は、メモリセルCの32ビットデータバスの下位8ビットとアクセスする対象の8ビットデータバスをダイレクトに接続し、32ビットアクセスの場合はメモリセルCの32ビットデータバスをそのままダイレクトに接続するセレクタC、28はメモリセルCのアクセス選択命令、リード、ライト切替命令、8ビット、32ビットアクセスビット幅の切替命令、メモリセルCのアドレス系列（セクタデータ系、PI, PO訂正系、ホスト転送系）の選択命令を生成するアクセス制御回路C、29はアドレス系列選択命令に従い、各アクセス系列のアドレスを生成するアドレス生成回路C、30は生成されたアドレスをメモリセルCのアドレスにデコードするアドレスデコーダCであり、第1図、

第7図と共通の部分については同一の参照数字をつけて説明を省略する。

同図において、インターフェイス回路16がホストコンピュータからのアクセス命令を受付けると、ピックアップ2により光ディスク1に記録されている信号が読み取られ、14のセクタ同期検出回路でセクタの先頭を検出、23のデータ復調回路に送られる。データ復調回路23では光ディスク1に記録された変調方式に従いデータの復調を行う。

ここで、第13図を用いて復調データの配置方法、訂正系列、ホスト転送系列の説明、及びアドレス制御方法について説明し、第12図で8ビット、32ビットとアクセスビット幅の可変な26のメモリセルCについて説明する。

第13図は、アドレス制御を行うデータの配列を示したもので、誤り訂正処理を行う為の訂正ブロックの構成である。図中、復調後のセクタデータ13G、行方向のセクタデータに対して訂正を行うPI訂正符号13H、列方向のセクタデータに対して訂正を行うPO訂正符号13Iで構成され、誤り訂正はこの訂正ブロック単位内で実行される。13Gのセクタデータは図に示されるように172バイト×12を1単位として構成され、セクタデータ中4バイトのセクタID、メインデータ1～12、付加データで構成される。訂正ブロック内ではこの1セクタデータ単位の構成で配置される。また、13Aは同期信号の検出、データ復調処理後の8ビット単位のセクタデータ系列を、13Bは10バイトの13HのPI訂正符号を用い行方向の訂正を行うPI訂正系列を、13Cは16個の13IのPO訂正符号を用い列方向の訂正を行うPO訂正系列をそれぞれ示す。13DはPI、PO訂正後のセクタデータ13Gをホストコンピュータに転送する際の読み出し方向であり、1セクタデータの中でメインデータ1～12の部分を転送、アクセスは4バイト(32ビット)単位で行われるホスト転送データ系列である。このように配

置されるデータに対してアドレス制御を行う際には13Fのロウアドレス、13Eのカラムアドレスを指定することで行う。

第12図は第11図中のメモリセルCの構成例で、8ビット単位でアクセス可能な4つのメモリバンク12Aと12B、12C、12Dを持ち、行方向、列方向のアドレスを指定する事で各メモリバンクへのアクセスが可能となっている。12Eはバンク切替用のセクタでバンク選択信号に従い8ビット単位アクセスのメモリバンク12A～12Dの選択が可能である。12Fのセクタは8、32ビット幅切替命令に従い、アクセスビット幅を切替えるセクタで、32ビットアクセス時には図中12Hに示すように、メモリバンク1の8ビットバスを最上位8ビットとし、メモリバンク2、3の8ビットバスをそれぞれ中位8ビット、メモリバンク4の8ビットバスを最下位8ビット、合計32ビットデータとして扱う。8ビットアクセス時にはバンクセクタ12Eで選択されたメモリバンク1～4の8ビットデータを下位8ビットとし、リード時、上位24ビットのデータとして“0”を加え32ビットデータとして扱う。12Gはリード/ライト切替命令に従い、データの転送方向を決定する1/0バッファである。このような構成でメモリセルCは構成され、アクセスビット幅が8ビット、32ビット単位でアクセスが可能になる。

第11図において、第13図に示したデータの配列方法でメモリアクセス制御を実行、第12図に示した構成のメモリセルCを用いてアクセスを行い、インターフェイス回路を介しホストコンピュータまでデータ転送を行う様子を第14図のフローチャートを併せて用い説明する。

第11図、第14図において、ホストコンピュータからのホストアクセス命令が16のインターフェイス回路において受けられ、光ディスク1から信号の読み出しが開始されると、信号中に含まれるセクタの先

頭を示す同期信号の検出が14のセクタ同期検出回路で行われ、23のデータ復調回路で8ビット単位のデータに復調、復調されたデータ中のセクタIDを31のセクタID検出回路で行う。(ステップ14A)、

5 I Dが含まれており、この要求セクタIDと検出セクタIDが一致したのであれば28のアクセス制御回路CによるメモリセルCへのアクセスの為の各設定が開始され、一致しなければセクタIDの一致検出を継続する(ステップ14B)。

セクタIDの一致検出に従い28のアクセス制御回路Cは27のセクタC、26のメモリセルC、29のアドレス生成回路Cの各制御対象

10 に対し、転送開始セクタIDが含まれるセクタデータをメモリセルCにライトする為命令を生成、セクタCはアクセス選択命令に従いデータ復調回路23からの8ビットデータバスとメモリセルCの32ビットデータバスの内、下位8ビットとを接続、メモリセルCは8ビット、32

15 ビット切替命令に従い、8ビット単位でデータ復調後のセクタデータをライトする為、アクセスビット幅を8ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路Cはアドレス系列選択命令に従い復調後のセクタ系列のアドレスを生成するように設定される(ステップ14C)。メモリセルCへのアクセス準備が完了するとデータ復調後のセクタデータが送られ、アドレス生成回路Cは復調後のセクタデータ系列のロウアドレス、カラムアドレスを8ビット単位のリード毎に生成、30のアドレスデコーダCでメモリセルCのアドレスにデコードされ8ビット単位でセクタデータがメモリセルCにライトされる(ステップ14D)。

25 誤り訂正が可能な訂正ブロックがメモリセルCの容量分ライトされると(ステップ14E)、アクセス制御回路Cは各制御対象にたいしてP

I 訂正系列をメモリセルCからリードする為の命令を生成する。セレクト
CはP I, P O 訂正回路への8ビットデータバスとメモリセルCの下
位8ビットデータバスとを接続、メモリセルCはリードを選択、アドレ
ス生成回路CはP I 訂正系列のロウ、カラムアドレスを生成するように
5 設定される(ステップ14F)。P I 訂正処理の為のメモリアクセス選
択が終了すると、アドレス生成回路CはP I 訂正系列のアドレスを生成、
アドレスデコーダCでメモリセルCのアドレスにデコードされ8ビット
単位でP I 訂正系列データがメモリセルCからリードされる。リードさ
れたP I 訂正系列に対して系列中に発生したエラーの訂正が実行される
10 (ステップ14G)。

P I 訂正系列の処理が終了すると、アクセス制御回路Cは各制御対象
に対してP O 訂正系列をメモリセルCからリードする為の命令を生成す
る。アドレス生成回路CはP O 訂正系列のアドレスを生成するように設
定され(ステップ14H)、P O 訂正系列のロウ、カラムアドレスを8
15 ビット単位のリード毎に生成、アドレスデコーダCでメモリセルCのアド
レスにデコードされ8ビット単位でP O 訂正系列データがメモリセル
Cからリードされる。リードされたP O 訂正系列に対して系列中に発生
したエラーの訂正が実行される(ステップ14I)。

P O 訂正系列の訂正処理が終了すると、アクセス制御回路Cは各制御
20 対象にたいしてホスト転送データ系列をメモリセルCからリードする為
の命令を生成する。セレクトCはインターフェイス回路16への32ビ
ットバスとメモリセルCの32ビットデータバスを接続し、メモリセル
Cはアクセスビット幅を32ビットに選択、アドレス生成回路Bはホス
トへ転送すべきデータ、第13図の13Gに示すように1セクタデータ
25 中のメインデータ1~12のホスト転送データ系列のアドレスを生成す
るように設定され(ステップ14J)、ホスト転送データ系列のロウ、

5 カラムアドレスを生成、32ビット単位のデータの最初にアクセスする
16 行、カラムアドレスを指定する。アドレスデコードCは生成された3
2ビット単位の先頭アドレスをメモリセルCのアドレスにデコードし、
1回のアクセスにつき32ビット単位でリード、インターフェイス回路
5 16に転送、訂正ブロック中に含まれるメインデータに転送処理を行う
(ステップ14K)。ホストコンピュータからの転送要求セクタ数に満
たない場合(ステップ14L)、ステップ14Cから処理を繰返し、要
求セクタ数に達したのであれば、処理を終了する。

10 この第3の実施形態において、光ディスク1から読み取られ、ディジ
タル化されたシリアルデータに対する復調方法が、シリアルデータに同
期して送られてくるビットクロック16個分のシリアルデータから8ビ
ット単位の平行データにデータ復調回路で変換される場合、シリア
ルデータの転送回数を示すビットクロック数と、インターフェイス回路
15 から32ビット単位でデータ転送を行う際の転送回数との関係は、ア
クセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考
慮し冗長度が100%とすると、ビットクロック(16+16)個に対し
て、8ビットで書き込まれたメモリから32ビットのデータ量のデータ
20 転送が1回で行われるので32:1となり、また、冗長度が0の場合1
6:1の関係となる。よって、一般的に冗長度は100%より小0%よ
り大であるので、ビットクロック周波数1に対して、出力転送周波数F_o
は $1/32 < F_o < 1/16$ となる。

これに対して、インターフェイス回路からのデータ転送が1回につき
16ビット単位であれば、同じ32ビットのデータ量を転送するのに2
回転送が必要となり、上記と同様の条件の場合、ビットクロック周波数
25 1に対して、出力転送周波数F_oは $1/64 < F_o < 1/32$ となる。

更にインターフェイス回路からのデータ転送或は、メモリ手段からイ

ンターフェイス回路へのデータ転送が8ビット単位で行われるのであれば、32ビットのデータ量を転送するのにインターフェイス回路からの転送或はメモリアクセスが4回必要となり、上記と同様の条件の場合、ビットクロック周波数1に対して、出力転送周波数 F_o は $1/128 < F_o < 1/64$ となり、データ転送効率が著しく低下する。

従って第3の実施の形態においては、光ディスクから読みだされた信号に対し必要な処理を行い、インターフェイス回路を通じてホストコンピュータにデータ転送を行う際には、32ビット単位で行う事により、ホストコンピュータへのデータの転送速度が向上する。また、メモリセルCのアクセス回数が減少するので、上記した複数の訂正ブロックを一時的に記憶するのに必要な大容量のメモリセルCを含む、再生装置全体の消費電力低減につながる。

また、以上説明した再生処理に必要なメモリセルC、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、ホストコンピュータにデータ転送を行う際には、32ビット単位で行う事が可能となりデータ転送速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第15図は本発明による第4の実施の形態を示すブロック図であって、ディスク記録装置に適応した例である。参照数字1はホストコンピュータから転送されたデジタルデータを記録可能な光ディスクで、ディスクに記録する際の位置を示す為のセクタ同期信号、物理IDがあらかじめ記録されている光ディスク、2は光ディスク1に対し変調信号の読みだし、書込みが可能なピックアップ、32は光ディスク1にあらかじめ記録された物理IDを検出し、検出IDと記録を開始する物理IDとの一致を検出する物理ID検出回路、33は1訂正ブロックを構成するPI, PO訂正符号の生成を行う訂正符号生成回路、34は光ディスク1

へ記録を行う為の信号に変調を行うデータ変調回路、35は1セクタデータ中に含まれる付加データ、セクタIDをメインデータに付加する、付加データ生成回路であり、第11図と共通の部分は同一の参照数字をつけて説明を省略する。

- 5 同図において、インターフェイス回路16がホストコンピュータからの記録要求命令を受付けると、光ディスク1に記録を行う為のデータがインターフェイス回路に送られてくる。

本実施の形態におけるホストコンピュータからの転送データの配置方法、訂正系列、データ変調系列、アドレス制御方法は第3の実施の形態
10 で説明した第13図の訂正ブロックと同様の構成を取り、13Gに示すように転送データをメインデータ1～12に割当て、セクタID、付加データをそれぞれ付加し1セクタデータを構成、13Dに示す方向に配置する。これを複数集めたセクタデータに対して13Cの方向の系列に対してPO訂正符号を生成、付加を行い、13Bの方向の系列にたいして
15 PI訂正符号を生成、付加する。変調処理を行う為のデータ読み出し系列は13Aの方向に対して行われる。アドレス制御については同様に13Fのロウアドレス、13Eのカラムアドレスを指定することで行う。

第15図において、第13図を用いて説明したデータの配列方法でメモリアクセス制御を実行、メモリセルCにおいてアクセスを行い、光
20 ディスク1にホストコンピュータからの転送データの記録を行う様子を第16図のフローチャートを併せて用い説明する。

第15図、第16図において、ホストコンピュータからの記録要求命令が16のインターフェイス回路において受けられ、ホストコンピュータからの32ビット単位の転送データがインターフェイス回路に送ら
25 れてくると(ステップ16A)、記録要求命令に従い28のアクセス制御回路Cは27のセクタC、26のメモリセルC、29のアドレス生

成回路 C の各制御対象に対し、インターフェイス回路からの転送データをメモリセル C にライトする為の命令を生成、セクタ C はアクセス選択命令に従い 3 5 の付加データ生成回路からの 3 2 ビットデータバスとメモリセル C の 3 2 ビットデータバスを接続、メモリセル C は 8 ビット、

5 3 2 ビット切替命令に従い、付加データを付加後の 3 2 ビット単位で送られてくる転送データをライトする為、アクセスビット幅を 3 2 ビットに設定、リード、ライト切替命令に従いライトを選択、アドレス生成回路 C はアドレス系列選択命令に従い付加データ生成回路からのセクタデータ系列のアドレスを生成するように設定される（ステップ 1 6 B）。

10 メモリセル C へのアクセス準備が完了するとインターフェイス回路に送られた転送データに対して付加データを付加し 1 セクタデータを形成し（ステップ 1 6 C）、アドレス生成回路 C は第 1 3 図中の 1 3 D に示す系列のロウアドレス、カラムアドレスを 3 2 ビット単位のリード毎に生成、3 0 のアドレスデコーダ C でメモリセル C のアドレスにデコード

15 され 3 2 ビット単位でセクタデータがメモリセル C にライトされる（ステップ 1 6 D）。

P I, P O 訂正符号が生成可能な分のセクタデータがライトされると（ステップ 1 6 E）、アクセス制御回路 C は各制御対象に対して P O 訂正系列をメモリセル C からリードする為の命令を生成する。セクタ C

20 は訂正符号生成回路への 8 ビットデータバスとメモリセル C の下位 8 ビットデータバスとを接続、メモリセル C はリードを選択、アドレス生成回路 C は P O 訂正系列のロウ、カラムアドレスを生成するように設定される（ステップ 1 6 F）。P O 訂正処理の為のメモリアクセス選択が終了すると、アドレス生成回路 C は P O 訂正系列のアドレスを生成、アド

25 レスデコーダ C でメモリセル C のアドレスにデコードされ 8 ビット単位で P O 訂正系列データがメモリセル C からリードされる。リードされた

P O 訂正系列に対して P O 訂正符号を生成し、メモリセル C 中の P O 訂正符号の領域にあたるアドレスにたいして P O 訂正符号がライトされる (ステップ 16 G)。

5 P O 訂正符号の生成、付加が終了すると、アクセス制御回路 C は各制御対象に対して P I 訂正系列をメモリセル C からリードする為の命令を生成する。アドレス生成回路 C は P I 訂正系列のアドレスを生成するように設定され (ステップ 16 H)、P I 訂正系列のロウ、カラムアドレスを 8 ビット単位のリード毎に生成、アドレスデコーダ C でメモリセル C のアドレスにデコードされ 8 ビット単位で P I 訂正系列データがメモリセル C からリードされる。リードされた P I 訂正系列に対して P I 訂正符号を生成し、メモリセル C 中の P I 訂正符号の領域にあたるアドレスにたいして P I 訂正符号がライトされる (ステップ 16 I)。

15 P I 訂正符号の生成、付加が終了すると、アクセス制御回路 C は各制御対象にたいして変調データ系列をメモリセル C からリードする為の命令を生成する。セクタ C はデータ変調回路 34 への 8 ビットバスとメモリセル C の下位 8 ビットデータバスを接続し、アドレス生成回路 B はデータ変調回路へ転送すべき第 13 図中の 13 A に示すデータ系列のアドレスを生成するように設定される (ステップ 16 J)。

20 光ディスク 1 への記録データの準備が終了すると、光ディスク 1 から信号の読み出しを行い、あらかじめ記録されている物理 I D の検出を 32 の物理 I D 検出回路で行われる (ステップ 16 K)。光ディスク 1 上の記録を開始する物理 I D と検出された物理 I D が一致したのであれば (ステップ 16 L)、29 のアドレス生成回路 C によるアドレス制御を開始し、変調データ系列のロウ、カラムアドレスを 8 ビット単位のリード毎に生成、アドレスデコーダ C は生成された 32 ビット単位の先頭
25 アドレスをメモリセル C のアドレスにデコードし、データ復調回路 16

に転送、データ変調処理後光ディスク1に記録する（ステップ16M）。

ホストコンピュータからの記録要求セクタ数に満たない場合（ステップ16N）、ステップ16Bから処理を繰返し、要求セクタ数を記録したのであれば、処理を終了する。

- 5 この第4の実施の形態において、光ディスク1にデータを記録する際に、インターフェイス回路に1回の転送で32ビット単位でデータ転送を行ってから、記録媒体に記録を行う8ビット単位のデータに対して16ビットのデータに変調処理を行った後シリアルデータを生成し、その時の変調手段の動作クロック16個であらわされる転送回数、或はそれ
- 10 と同等の16個の転送回数が判明するような信号に従ってシリアルデータが記録媒体に記録される場合、インターフェイス手段へ1回の転送につき32ビット単位のデータ転送を行う際の転送回数と、シリアルデータの記録媒体への転送回数との関係は、アクセスビット幅可変なメモリを用いた場合、誤り訂正符号等の冗長分を考慮し冗長度が100%とす
- 15 ると、32ビットのデータ量のデータ転送1回に対して32ビットで書き込まれたメモリから8ビットのデータ量のデータ転送が4回行われるので、記録媒体へシリアルデータの転送が $(16 + 16) \times 4 = 128$ 回行われ、また、冗長度が0の場合 $16 \times 4 = 64$ 回行われる。よって、一般的に冗長度は100%より小0%より大であるので、インターフェ
- 20 イス手段へのデータ転送1回に対して、記録媒体へのシリアルデータの転送回数 S_i は $64 < S_i < 128$ となる。

- これに対して、インターフェイス回路へのデータ転送が1回につき16ビット単位であれば、同じ32ビットのデータ量を転送するのに2回の転送を必要となり、上記と同様の条件の場合、インターフェイス手段
- 25 へのデータ転送1回に対して、記録媒体へのシリアルデータの転送回数 S_i は $32 < S_i < 64$ となり、記録媒体へのデータ転送効率が低下す

る。

インターフェイス回路が32ビットでも、アクセスビット幅可変なメモリを用いず、インターフェイス回路からメモリ手段へのデータ転送が16ビット単位で行われるのであれば、32ビットのデータ量を転送するの
5 5 に16ビット単位のメモリアクセスが2回必要となり、上記と同様に、メモリアクセス1回に対して、記録媒体へのシリアルデータの転送回数 S_i は $32 < S_i < 64$ となる。

更にインターフェイス回路へのデータ転送、或はインターフェイス回路からメモリ手段へのデータ転送が8ビット単位で行われるのであれば、
10 32ビットのデータ量を転送するのに8ビット単位のインターフェイス回路への転送、或はメモリアクセスが4回必要となり、冗長度は100%の場合8ビットのデータ量のデータ転送1回に対して、記録媒体へシリアルデータの転送が $(16 + 16) \times (8 \div 8) = 32$ 回行われ、冗長度が0の場合 $16 \times (8 \div 8) = 16$ 回行われる。すなわち、上記と同様の条件の場合、インターフェイス手段へのデータ転送、或はインターフェイス
15 回路からメモリ手段へのデータ転送1回に対して、記録媒体へのシリアルデータの転送回数 S_i は $16 < S_i < 32$ となり、記録媒体へのデータ転送効率が著しく低下する。

従ってこの実施の形態においては、ホストコンピュータから転送されたデータに対して、光ディスク1に記録する為に必要なエンコード処理
20 を行い、記録を行う際には、転送データを32ビット単位でメモリセルCにライトする事によりデータ転送に必要な時間が減少し、記録を行う光ディスクに対するデジタル信号のエンコードの為の処理速度が向上する。また、アクセス回数が減少するので、生成される複数の訂正ブロックを一時的に記憶するのに必要な大容量のメモリセルCを含む、記録
25 装置全体の消費電力低減につながる。

また、以上説明した記録処理に必要なメモリセルC、各処理回路、制御回路を同一の半導体チップ上に設けた場合でも、転送データを32ビット単位でメモリセルCにライトする事によりデータ転送に必要な時間が減少し、記録を行う光ディスクに対するデジタル信号のエンコードの為の処理速度が向上すると共に、メモリアクセス回数が減少し、半導体チップ全体の消費電力低減につながる。

第17図は本発明による再生装置及び再生方法の第5の実施の形態を示すブロック図であって、第7図を用いて説明した第2の実施の形態と同一の処理を行い、1つのメモリセルDで再生装置を構成した場合を示す。参照数字36はアクセスビット幅が8ビット、16ビット、32ビットと可変にアクセス可能なメモリセルD、37はメモリセルDにアクセスする対象を制御し、8ビットアクセスの場合は、メモリセルDの32ビットデータバスの下位8ビットとアクセスする対象の8ビットデータバスをダイレクトに接続、16ビットアクセスの場合は、メモリセルDの32ビットデータバスの下位16ビットとアクセスする対象の16ビットデータバスをダイレクトに接続、32ビットアクセスの場合はメモリセルDの32ビットデータバスをそのままダイレクトに接続するセレクタD、38はメモリセルDのアクセス選択命令、リード、ライト切替命令、8ビット、16ビット、32ビットアクセスビット幅の切替命令、メモリセルDのアドレス系列（復調データ系、C1、C2訂正系、再生データフレーム系、PI、PO訂正系、ホスト転送系）の選択命令をそれぞれ生成するアクセス制御回路D、39はアドレス系列選択命令に従い、各アクセス系列のアドレスを生成するアドレス生成回路D、40は生成されたアドレスをメモリセルDのアドレスにデコードするアドレスデコーダDであり、第7図に対応する部分は同一の参照数字をつけて重複する説明を省略する。

同図において、インターフェイス回路16がホストコンピュータからのアクセス命令を受付けると、ホストコンピュータに転送を行うデータが記録されているディスク上の位置の付近から、ピックアップ2により光ディスク1に記録されている信号が読み取りが開始され、フレーム同期信号の検出を4のフレーム同期検出回路で行った後、5のEFM復調回路で8ビット単位の復調データに復調される。28のアクセス制御回路Dは、これと同時に、37のセクタD、36のメモリセルD、39のアドレス生成回路Dそれぞれの制御対象に対し、8ビット（1シンボル）単位で送られてくる復調データメモリセルDにライトするように制御する。メモリセルDにアクセスする際のアドレス制御方法は、第3図で説明した制御方法（ロウ、カラムアドレス、ロウバンク、カラムバンクアドレスを指定）で行われ、復調データ系列に対するアドレスをアドレス生成回路Dで生成、アドレスデコードDでメモリセルDの実際のアドレスにデコードされ、このデコードアドレスに従い復調データをメモリセルDにライトする。

復調データのライトをホストコンピュータへ転送する容量分、或はメモリセルDの記憶容量分先行いC2訂正が可能な復調データがライトされると、アクセス制御回路Dはそれぞれの制御対象に対し、8ビット（1シンボル）単位でC1訂正を行うデータ系列をメモリセルDからリードするように制御する。

C1訂正を行うデータ系列がリードされC1訂正処理が終了すると、アクセス制御回路Dはそれぞれの制御対象に対し、8ビット（1シンボル）単位でC2訂正を行うデータ系列をメモリセルDからリードするように制御する。

C2訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Dはそれぞれの制御対象に対し、16ビット（1ワード）単位で再生デ

ータ系列をリードするように制御し、14のセクタ同期検出回路に転送される。リードされた再生系列は第9図に示したセクタ単位のデータを構成し、再生データ系列に含まれるセクタ同期信号の検出、同期信号の直後の2ワードデータに記録されているセクタIDの検出を31のセクタID検出回路で行う。

セクタ同期信号の検出処理が終了すると、アクセス制御回路Dはそれぞれの制御対象に対し、セクタ同期信号以外のセクタデータの配列中に含まれるP訂正系列に対する誤り訂正処理を行うため、P訂正系列に対するデータ系列をメモリセルDからリードするように制御する。

10 P訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Dはそれぞれの制御対象に対し、セクタ同期信号以外のセクタデータの配列中に含まれるQ訂正系列に対する誤り訂正処理を行うため、Q訂正系列に対するデータ系列をメモリセルDからリードするように制御する。

15 Q訂正系列に対する誤り訂正処理が終了すると、アクセス制御回路Dはそれぞれの制御対象に対し、ホストコンピュータへの転送データ系列を32ビット単位でメモリセルDからリードするように制御する。ホストコンピュータのアクセス命令にはデータ転送を開始する転送開始セクタIDが含まれており、また、セクタ同期信号の検出を行った際にメモリセルDに記憶されているセクタデータに対するIDが検出されている。

20 この転送開始セクタIDと検出セクタIDが一致するセクタを含み、それ以降のセクタIDに対するセクタに含まれるホスト転送データ系列に対し、メモリセルDからリードを行い、1回のアクセスにつき32ビット(2ワード)単位でインターフェイス回路16に転送され、ホストコンピュータへ転送される。

25 ホストコンピュータからの転送要求セクタ数に満たない場合は、EFM復調回路からの8ビット(1シンボル)単位の復調データライトから

処理を再開し、要求セクタ数に達したのであれば、処理を終了する。

以上説明した処理を実行する為のメモリセルDへのアクセスは全て1
バンク単位に対するロウアドレス、カラムアドレス、バンクに対するロ
ウバンクアドレス、カラムバンクアドレスを指定する事でアドレス制御
5 が行われる。

この第5の実施の形態においても、前記した第2の実施の形態と同様
に、EFM復調回路で変換される場合、シリアルデータ（復調データ1
4ビットとマージン3ビット単位でシリアル転送）の転送回数を示すビ
ットクロックと、インターフェイス回路から32ビット単位でデータ転
10 送を行う際の転送回数との関係は、アクセスビット幅可変なメモリを用
いた場合、ビットクロック周波数1に対して、出力転送周波数 F_o は
 $1/34 < F_o < 1/17$ となる。また、インターフェイス回路からのデ
ータ転送が1回につき16ビット単位であれば、 $1/68 < F_o < 1/$
34、更にインターフェイス回路からのデータ転送或は、メモリ手段か
15 らインターフェイス回路へのデータ転送が8ビット単位で行われるので
あれば、 $1/136 < F_o < 1/68$ となり、データ転送効率が著しく
低下する。

従ってこの実施の形態においては、光ディスクからの読み出し信号に
対し、復調処理を行った8ビット単位の復調データの配列への配置を行
20 うメモリアクセス、C1、C2訂正処理を行うデータ系列に対するアク
セス、セクタ同期信号の検出を行う系列に対するアクセス、P、Q訂正
処理を行うデータ系列に対するアクセス、インターフェイス回路への転
送データ系列に対するアクセスを1つのメモリセルDにより行う事で、
第7図で説明した再生装置と同様の処理、同等のデータ転送速度を実現
25 でき、また、再生装置の構成が容易になる。

また、1つのメモリセルDで処理を実現する事により、制御回路が1

系統ですみ、このメモリセルD、処理に必要な各処理回路、制御回路を同一の半導体チップ上に設けた場合、図7の再生装置の構成を同一の半導体チップに実現した場合よりも、半導体チップ全体の消費電力の低減効果が大きく、半導体チップのサイズも押さえる事ができ、半導体の製造コストの面からも有利である。

なお以上に示した実施の形態において、データを貯える記録媒体はこの実施の形態の光ディスクに限定される物でなく、取り扱うデジタル信号をメモリ等の一時的にデータを記憶する手段に記憶し、所定の処理を行い転送データを出力するような形態のデジタル信号処理システム、例えばテープ状の記録媒体の記録再生装置、磁気ディスク記録媒体の記録再生装置、或はデータ転送システム、通信システム等にも適用でき、かつこれらのデジタル信号処理システムにおける処理に必要なアクセスビット幅可変なメモリ等の記憶手段と、所定の処理実行に必要な周辺回路、処理手段を同一の半導体チップ上に設け実現した場合にも適用できる。

また、アクセスビット幅可変なメモリを制御する制御手段は、同等の制御機能を実現する様にプログラムされたマイクロプロセッサを用い実現してもかまわず、プログラムの変更により可変なアクセスビット幅を、処理を実行するデジタル信号のビット幅に合わせ、変更できるようにして処理を実行してもよく、この場合アクセスビット幅可変なメモリとマイクロプロセッサを含む所定の処理を行う手段を同一の半導体チップ上に設ける事により実現される。

また、アクセスビット幅可変なメモリを同一の半導体チップ上に設ける場合、メモリは一定時間間隔で書換が必要なダイナミックなメモリ、あるいは書換動作の必要が無いスタティックなメモリどちらで実現しても構わない。

また、第1から第5の実施の形態で用いるメモリセルの構成はこの実施の形態に限定される物でなく、アクセスを行う処理手段に応じてアクセスビット幅を可変にできるメモリセルであればどんな構成をとっても構わない。

- 5 第1の実施の形態におけるアドレス制御の単位である1バンクの構成は、この実施の形態に限定される物でなく、メモリ等の一時記憶手段に記録、所定の処理を行った後の転送データに対するアクセスが容易になるような1バンク構成が採用される。

10 第2、第3、第4の実施の形態における、メモリセルB、メモリセルCにおいて、各処理を行う際に必要なデータ系列のアクセスに対するアドレス制御方法は、第1図の実施の形態で説明した、1バンク単位で、1バンク中のロウアドレス、カラムアドレス、バンクに対するロウバンクアドレス、カラムバンクアドレスを指定することにより行ってもよい。

15 第2、第3、第4、第5の実施の形態におけるホストコンピュータとの間でデータ転送を行うインターフェイス回路はこの実施の形態に限定される物でなく、ホストコンピュータとのアクセスバス幅が64ビットあるいはそれ以上でも構わない。この場合メモリセルはインターフェイス回路との間で64ビット単位、或はそれ以上のアクセスビット幅でデータ転送を実行し、それぞれのアクセスビット幅に対応したメモリセル、
20 アクセスの対象を制御するセレクタが用意される。

また、第4の実施の形態において記録可能な光ディスク1にあらかじめ記録されている物理IDの検出方法は、この実施の形態に限定される物でなく、光ディスク中の記録トラックをうねらせIDの代用となる物を記録した光ディスクの記録にも適応される。この場合のID検出は例
25 えば、トラックのうねりによる周波数変化を物理ID検出回路で計測し、光ディスク上のアドレスとして認識され処理が行われる。

また、説明した全ての実施の形態において用いられるメモリ手段の、可変なアクセスビット幅の種類は、この実施の形態に限定される物でなく、メモリ手段に記憶されているデータ配列に対して、処理を実行する手段が最も効率よく処理を行えるようアクセスする処理手段に応じて何
5 種類にでも切替えるようにしても良い。

また、説明した全ての実施の形態を実現する為に必要なメモリセル、各処理回路、制御回路、或は処理回路、制御回路と同等の処理をプログラム制御により実行するマイクロプロセッサを同一の半導体チップ上に設けることによっても、再生装置、記録装置と同様の処理が実現できる。

10

産業上の利用可能性

本発明によると、光ディスクから読みだされた信号に対しデータ復調処理後の1シンボル(8ビット)単位のデータ書込みから、2シンボル(16ビット)単位で再生データの読み出しを行うまでのアドレス制御を、まとまった複数シンボル単位で1バンクを構成し、1バンク中のロ
15 ウ、カラムアドレスと、バンクに対するロウバンク、カラムバンクアドレスを指定して1又は2シンボル単位のデータに対するアクセスを行う事によりアドレス制御が容易となる。

また、アドレス制御を行う際の再生データ系列の配置を工夫し、それ
20 に対するC1、C2訂正系列、復調系列の配置でアドレス制御する事により1回のアクセスで再生データを2シンボル転送する事が容易になる。

また、再生データ系列の読み出しの際のアクセスビット幅を16ビット或は32ビットで行うため、再生データを1回のアクセスにつき16
25 ビット或は32ビット単位で転送でき、再生データに対して補間、フィルタ処理を行う手段やホストコンピュータとのインターフェイス手段へのデータ転送速度が向上し、インターフェイス手段からホストコンピュ

ータへのデータ転送速度も向上する。また、一連のデジタル信号処理を行う際に必要なメモリアクセス回数を減少させる事ができる。

また、一連のデジタル信号処理に必要なメモリ手段、各処理回路、制御回路を同一の半導体チップ上に設ける際には、各処理を効率良く行うために必要なメモリ手段へのアクセスビット幅の単位で処理を行えるように構成される。例えばE F M復調回路は8ビット単位で復調データを出力するように構成され、16ビットデジタルオーディオ再生データに対する出力補間、フィルタ処理回路はデータの単位にあわせて16ビット単位で処理を行うよう構成、ホストコンピュータとの間でデータ転送を行うインターフェイス回路は、ホストコンピュータとのインターフェイスバス幅にあわせて16ビット、32ビット或はそれ以上のバス幅でメモリ手段とのデータ転送を行うように構成される。これら処理回路により異なるアクセスビット幅に対し、メモリ手段は可変なアクセスビット幅の種類に対応したアクセスが可能ないようにカスタマイズされ、アクセスする対象に従って可変にアクセスビット幅を設定できるようなメモリ手段が半導体チップ上に設けられる。

このように一連のデジタル信号処理に必要な手段とアクセスビット幅を可変に設定できるようにカスタマイズされたメモリ手段を同一の半導体チップ上に実現した場合でも、メモリアクセス回数の減少による半導体チップ全体の消費電力低減、一連のデジタル信号処理の高速処理が実現できると共に、半導体チップから出力される再生データの転送速度向上が実現できる。また、アクセスビット幅可変にカスタマイズされたメモリ手段をダイナミックなメモリで構成した場合には、大容量メモリを必要とするデジタル信号処理システムを同一の半導体チップ上に実現でき、消費電力の低減、高速な信号処理、半導体チップからのデータ転送速度の向上の効果を得る事ができる。

請求の範囲

1. 記録媒体からの読み出し信号に対し所定の信号処理を行う信号処理手段と、データを一時的に記憶するメモリ手段を有し信号処理後のデジタルデータを出力するデジタル信号再生装置であって、
- 5 有効アクセスビット幅を n ビットと $n \times m$ ビット（ n 、 m は自然数）に変更可能なバス幅可変手段と、
- 前記メモリ手段のアクセスを行う制御手段とを有し、
- 該制御手段は、前記バス幅可変手段により、前記メモリ手段の有効アクセスビット幅を n ビットと $n \times m$ ビットのバス幅に変更可能であり、
- 10 少なくとも、前記メモリ手段に対して、 n ビット単位のデジタルデータの書込みを行い、 $n \times m$ ビット単位で読出しを行うことを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。
2. 請求の範囲第1項記載のバス幅可変メモリを用いたデジタル信号再生装置において、
- 15 前記制御手段は、前記メモリ手段のアクセスとして、 n ビット単位で、デジタルデータを所定の順番に配列するためのデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、 $n \times m$ ビット単位で転送データ系列の読み出し
- 20 を行うことを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。
3. 請求の範囲第2項記載のバス幅可変メモリを用いたデジタル信号再生装置において、
- 前記バス幅可変手段と、メモリ手段と、少なくとも前記誤り訂正を行う訂正手段は、同一の半導体チップ上に設けることを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。
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4. 請求の範囲第3項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

前記メモリ手段は、一定時間で書き直し動作が必要なダイナミックなメモリを用いることを特徴とするバス幅可変メモリを用いたデジタル
5 信号再生装置。

5. 請求の範囲第1項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

前記メモリ手段は、 n ビット幅でアクセスを行う一時記憶手段 m 個からなり、

10 前記バス幅可変手段は、前記 m 個の一時記憶手段の選択を行う第1の選択手段と、

該第1の選択手段で選択された n ビットデータバスと、 m 個の一時記憶手段で構成された $n \times m$ ビットデータバスの選択を行う第2の選択手段と

15 を有することを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。

6. 請求の範囲第1項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

20 記録媒体からの読取り信号を復調し該復調データを n ビット単位で出力する復調手段と、

誤り訂正処理に対するデータ配列に対し、 n ビット単位で処理を行う誤り訂正手段と、

誤り訂正後のデータ配列に対し、 $n \times m$ ビット単位で処理を行う出力処理手段と、

25 前記メモリ手段のデータバスに対し、前記復調手段、誤り訂正手段、出力処理手段のデータバスを選択的に接続する接続手段と

前記復調手段、誤り訂正手段、出力処理手段のそれぞれの処理に必要な、データ配列のアクセスに必要なアドレスを生成するアドレス生成手段と、

- 5 生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、
前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

- 10 前記制御手段は、前記メモリ手段のアクセスとして、 n ビット単位で、復調後のデジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、 $n \times m$ ビット単位で前記出力処理手段への転送データの読み出しを行う際に、 $n \times m$ ビットのバス幅とすることを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。

7. 請求の範囲第6項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

- 15 前記アドレス生成手段は、前記復調手段からのデータ書込み、前記誤り訂正手段へのデータ読み出し、前記出力手段へのデータ読み出しを行う時、それぞれの処理の対象のデータ配列に対し $n \times i$ ビット（ i は自然数）と $(n \times m) \times j$ ビット（ j は自然数）を単位とするバンク単位でアクセスを行うために、1バンク単位の縦方向のアドレスと横方向のアドレス、及び、各バンクにおける、縦方向のバンクアドレス、横方向のバンクアドレスをそれぞれ生成することを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。
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8. 請求の範囲第1項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

- 25 記録媒体からの読取り信号を復調し該復調データを n ビット単位で出力する復調手段と、

誤り訂正処理に対するデータ配列に対し、 n ビット単位で処理を行う誤り訂正手段と、

誤り訂正後のデータ配列に対し、 $n \times m$ ビット単位でデータを受付け、 $n \times m$ ビット単位でホストコンピュータへデータ転送を行うインターフェイス手段と、

前記メモリ手段のデータバスに対し、前記復調手段、誤り訂正手段、インターフェイス手段のデータバスを選択的に接続する接続手段と

前記復調手段と前記誤り訂正手段のそれぞれの処理に必要なデータ配列及び前記インターフェイス手段へデータ転送を行う際に必要なデータ配列のアクセスに必要なアドレスを生成するアドレス生成手段と、

生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

前記制御手段は、前記メモリ手段のアクセスとして、 n ビット単位で、変調後のデジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ配列の読み出しを行い、 $n \times m$ ビット単位で前記インターフェイス手段へ転送データの読み出しを行う際に、 $n \times m$ ビットのバス幅とすることを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。

9. 請求の範囲第8項記載のバス幅可変メモリを用いたデジタル信号再生装置において、

前記復調手段へ送られるシリアルデータの復調方式が、 k ビットを n ビット (k 、 n は自然数) に復調する方式であり、シリアルデータの復調手段への転送回数を示すビットクロックの単位時間当たりのクロック数と、1回の転送につき $n \times m$ ビット単位の前記データ転送を行う際の単位時間当たりの転送回数の関係が、 $1 : 1/k \sim 1 : 1/2k$ の範囲の

関係である事の特徴とするバス幅可変メモリを用いたデジタル信号再生装置。

10. アクセスビットバス幅が可変な、データを一時的に記憶するメモリ手段を用いた、記録媒体からのデジタル信号を再生する再生装置の再生方法であって、

アクセス命令に呼応して、記録媒体からの読取り信号を復調し該復調データをnビット単位でメモリ手段に書き込むためのアドレス生成、メモリアクセスを行う第1のステップと、

10 復調データのメモリ手段への書込みが終了した事に呼応して、誤り訂正処理のために該復調データをnビット単位でメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第2のステップと、

15 誤り訂正処理が終了した事に呼応して、メモリ手段に対してはアクセスビット幅をn×mビットを指定し、誤り訂正処理後の再生データを出力するようにアドレス生成、メモリアクセスを行う第3のステップによりデジタル信号を再生することを特徴とするバス幅可変メモリを用いたデジタル信号の再生方法。

11. 請求の範囲第10項記載のバス幅可変メモリを用いたデジタル信号の再生方法において、

20 前記アクセス命令は、前記再生装置のホストコンピュータとのインターフェイス手段から受付けた命令であって、

前記第3のステップにおける再生データの出力は、インターフェイス手段を介してホストコンピュータへデータ転送することを特徴とするバス幅可変メモリを用いたデジタル信号の再生方法。

25 12. デジタルデータに対し所定の信号処理を行う信号処理手段と、データを一時的に記憶するメモリ手段を有し信号処理後のデジタルデータを記録媒体に記録するデジタル信号記録装置であって、

有効アクセスビット幅を n ビットと $n \times m$ ビット（ n 、 m は自然数）に変更可能なバス幅可変手段と、

前記メモリ手段のアクセスを行う制御手段とを有し、

5 該制御手段は、前記バス幅可変手段により、前記メモリ手段の有効アクセスビット幅を n ビットと $n \times m$ ビットのバス幅に変更可能であり、少なくとも、前記メモリ手段に対して、 $n \times m$ ビット単位でデジタルデータの書込みを行い、 n ビット単位で読出しを行うことを特徴としたバス幅可変メモリを用いたデジタル信号記録装置。

10 13. 請求の範囲第12項記載のバス幅可変メモリを用いたデジタル信号記録装置において、

前記制御手段は、前記メモリ手段のアクセスとして、 $n \times m$ ビット単位で、デジタルデータを所定の順番に配列するためデータの書込み、及び、配列中のデータに含まれる誤り訂正に必要な処理を実行する為のデータ系列の読み出しを行い、 n ビット単位で転送データ系列の読み出しを行うことを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

14. 請求の範囲第13項記載のバス幅可変メモリを用いたデジタル信号記録装置において、

20 前記バス幅可変手段と、メモリ手段と、少なくとも前記誤り訂正を行う訂正手段は、同一の半導体チップ上に設けることを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

15. 請求の範囲第14項記載のバス幅可変メモリを用いたデジタル信号記録装置において、

25 前記メモリ手段は、一定時間で書き直し動作が必要なダイナミックなメモリを用いることを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

16. 請求の範囲第12項記載のバス幅可変メモリを用いたデジタル信号記録装置において、

前記メモリ手段は、 n ビット幅でアクセスを行う一時記憶手段 m 個からなり、

5 前記バス幅可変手段は、前記 m 個の一時記憶手段の選択を行う第1の選択手段と、

該第1の選択手段で選択された n ビットデータバスと、 m 個の一時記憶手段で構成された $n \times m$ ビットデータバスの選択を行う第2の選択手段とを有することを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

17. 請求の範囲第12項記載のバス幅可変メモリを用いたデジタル信号記録装置において、

15 ホストコンピュータからの $n \times m$ ビット単位の転送データを受信し、前記メモリ手段へ $n \times m$ ビット単位でデータ転送を行うインターフェイス手段と、

該インターフェイス手段からの $n \times m$ ビット単位の転送データに対し記録媒体に記録する必要がある付加データを生成し、該付加データを付加したデータを $n \times m$ ビット単位で出力する付加データ生成手段と

20 誤り訂正処理を行うデータ配列に対し訂正符号を生成し n ビット単位で出力する訂正符号生成手段と、

変調処理を行うデータ配列を n ビット単位で入力し変調データを出力する変調手段と、

メモリ手段のデータバスに対し、前記付加データ生成手段、訂正符号生成手段、変調手段とのデータバスを選択的に接続する接続手段と、

25 前記付加データ生成手段、訂正符号生成手段、変調手段それぞれの処理に必要なデータ配列のアクセスに必要なアドレスを生成するアドレス

生成手段と、

生成されたアドレスをメモリ手段上のアドレスにデコードする手段と、
前記メモリ手段、接続手段、アドレス生成手段に対する制御命令を生成する手段とを有し、

- 5 前記制御手段は、前記メモリ手段のアクセスとして、 $n \times m$ ビット単位でホストコンピュータから転送され、記録媒体に記録する際に必要な付加データが付加された $n \times m$ ビット単位のデジタルデータを、所定の順番に配列するためデータの書込みを行う際に、 $n \times m$ ビットのバス幅とし、 n ビット単位で、配列中のデータに含まれ誤り訂正符号の付加
10 を実行するのに必要なデータ配列の読み出し、及び、変調処理を行う変調データのデータ配列に対する読み出しを行う際に、 n ビットのバス幅とすることを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

18. 請求の範囲第17項記載のバス幅可変メモリを用いたデジタル
15 信号記録装置において、

- 前記アドレス生成手段は、前記付加データ生成手段からのデータ書込み、前記訂正符号生成手段へのデータ読み出し、前記変調手段へのデータ読み出しを行う時、それぞれの処理の対象のデータ配列に対し $n \times i$ ビット（ i は自然数）と $(n \times m) \times j$ ビット（ j は自然数）を単位とするバンク単位でアクセスを行うために、1バンク単位の縦方向のアドレスと横方向のアドレス、及び、各バンクにおける、縦方向のバンクアドレス、横方向のバンクアドレスをそれぞれ生成することを特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

19. 請求の範囲第17項記載のバス幅可変メモリを用いたデジタル
25 信号記録装置において、

前記変調手段の変調方式が、 n ビットを k ビット（ n 、 k は自然数）

に変調する方式であり、1回の転送につき $n \times m$ ビット単位の前記インターフェイス手段からの前記データ転送を行う際の単位時間当たりの転送回数と、前記変調手段からのシリアルデータの転送回数を示すビットクロックの単位時間当たりのクロック数の関係が、 $1 : m k \sim 1 : 2 m$
5 k の範囲の関係である事を特徴とするバス幅可変メモリを用いたデジタル信号記録装置。

20. アクセスビットバス幅が可変な、データを一時的に記憶するメモリ手段を用いた、ホストコンピュータからの転送データを記録媒体に記録する記録装置の記録方法であって、

- 10 ホストコンピュータからの記録開始に呼応して、 $n \times m$ ビット単位のホストコンピュータからの転送データに対し記録媒体に記録する必要のある付加データを付加したデータを $n \times m$ ビット単位でメモリ手段に書き込むためのアドレス生成、メモリアクセスを行う第1のステップと、
該付加データのメモリ手段への書込みが終了した事に呼応して、メモリ手段に対しアクセスビット幅を n ビットに指定し、誤り訂正符号を付
15 加する処理のために前記付加データを n ビット単位でメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第2のステップと、
誤り訂正符号付加後データのメモリ手段への書込みが終了した事に呼
20 応して、メモリ手段に対しアクセスビット幅を n ビットに指定し、変調処理のためのメモリ手段から読み出すためのアドレス生成、メモリアクセスを行う第3のステップにより変調処理後のデータを記録媒体に記録することを特徴とするバス幅可変メモリを用いたデジタル信号の記録方法。

21. 記録媒体からの読み取り信号を復調する復調手段と、データを一
25 時的に記憶するメモリ手段と、復調後のデータを誤り訂正処理する誤り訂正手段とを有し、誤り訂正処理により再生された再生データを読み出

しデータ転送を行うデジタル信号再生装置において、

前記復調手段へ送られるシリアルデータの復調方式が、 k ビットを n ビット (k 、 n は自然数) に復調する方式であり、

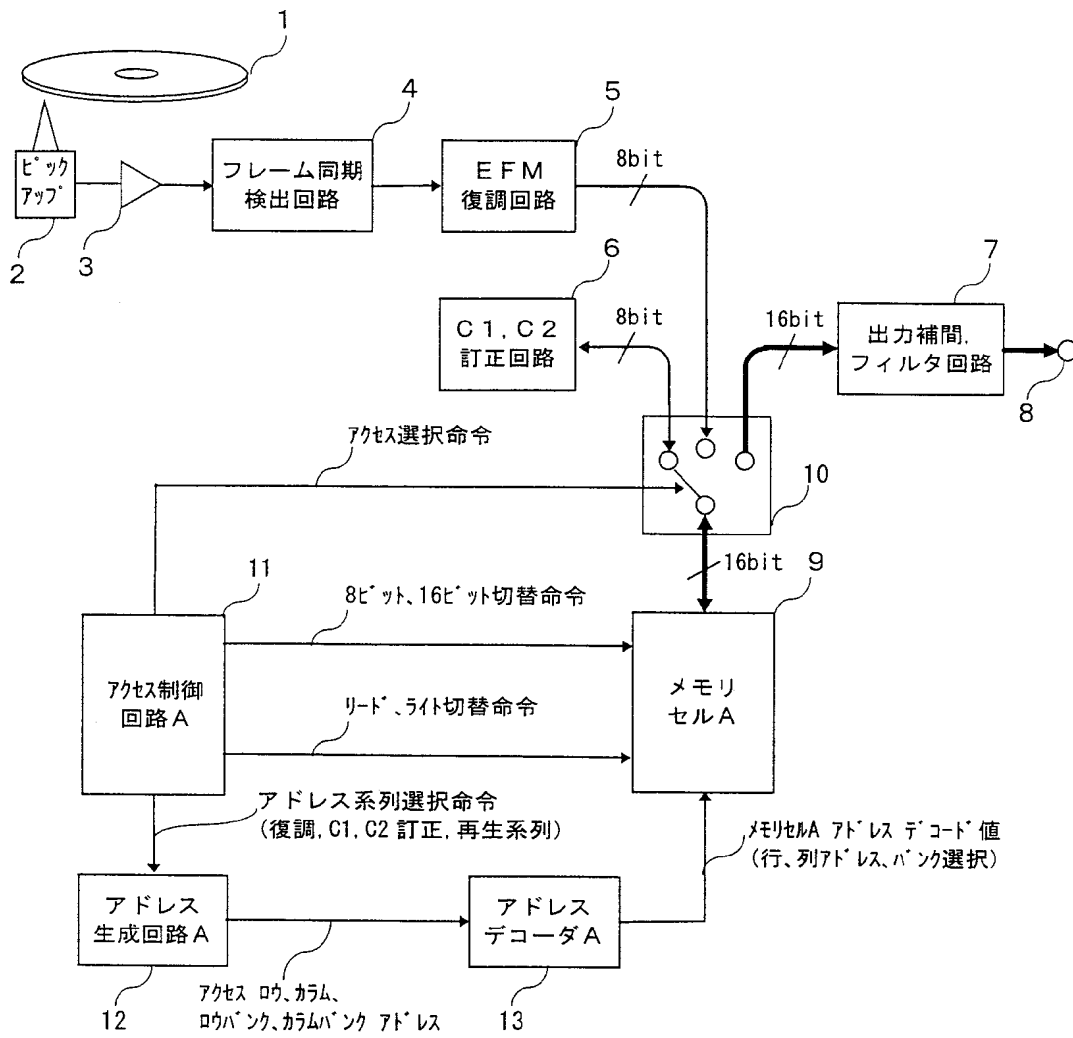
- 5 前記復調手段へのシリアルデータの転送回数を示すビットクロックの単位時間当たりのクロック数と、1回の転送につき $n \times m$ ビット単位 (m は2以上の整数) の前記データ転送を行う際の単位時間当たりの転送回数の関係が、 $1 : 1/k \sim 1 : 1/2k$ の範囲の関係であることを特徴とするデジタル信号再生装置。

- 10 2.2. 記録媒体からの読み取り信号を復調する復調手段と、復調後のデータを誤り訂正処理する誤り訂正手段と、データを一時的に記憶するメモリ手段と、誤り訂正処理により再生された再生データを読み出しデータ転送を行うデジタル信号再生装置において、

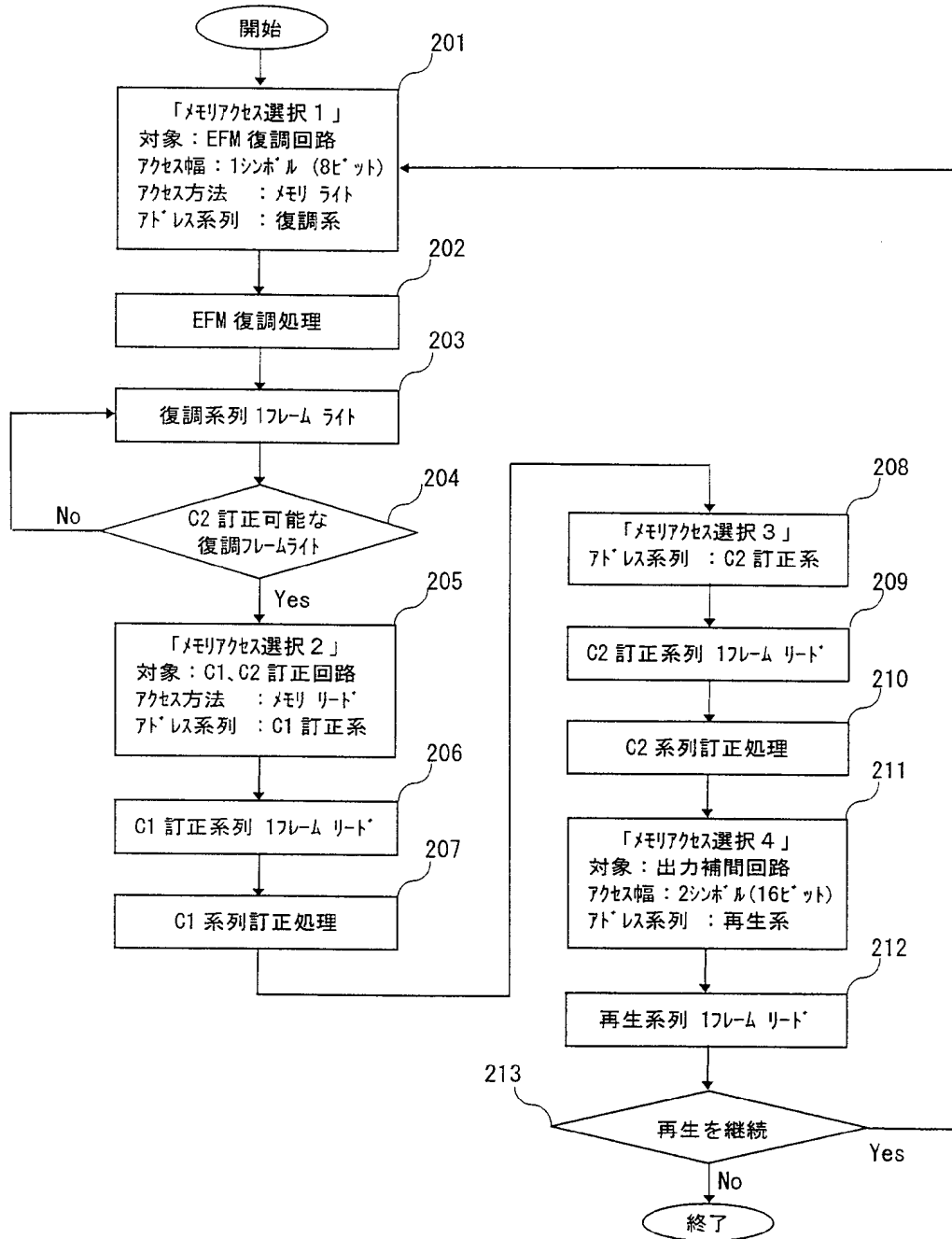
さらに、有効アクセスビット幅を n ビットと $n \times m$ ビット (n は自然数、 m は2以上の整数) に変更可能なバス幅可変手段を有し、

- 15 前記メモリ手段のアクセスバスは、前記バス幅可変手段を介して有効アクセスビット幅を可変な構成とし、かつ、前記復調、誤り訂正処理後の前記データ転送の有効アクセスビット幅と一致させたことを特徴とするバス幅可変メモリを用いたデジタル信号再生装置。

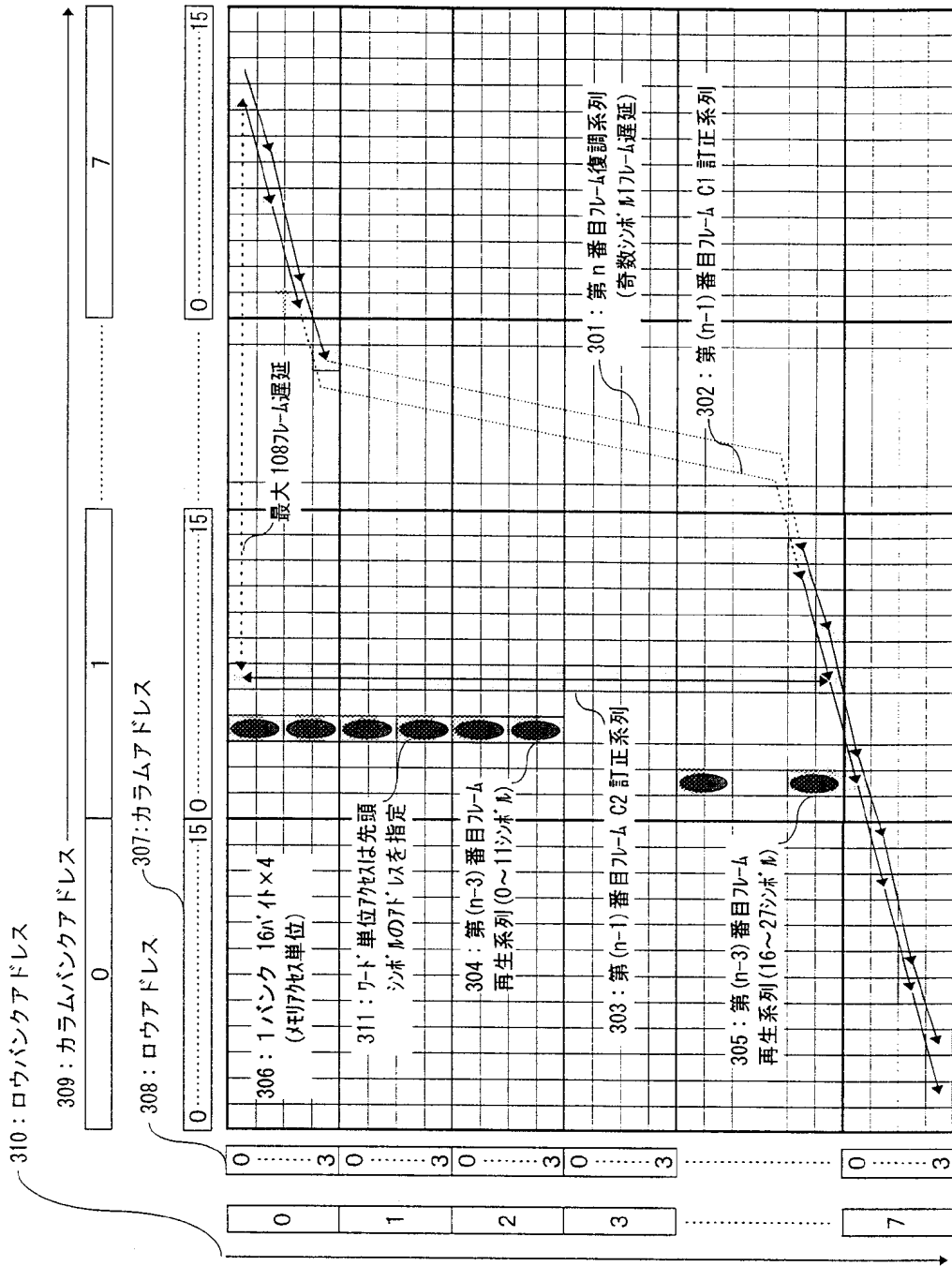
第1図



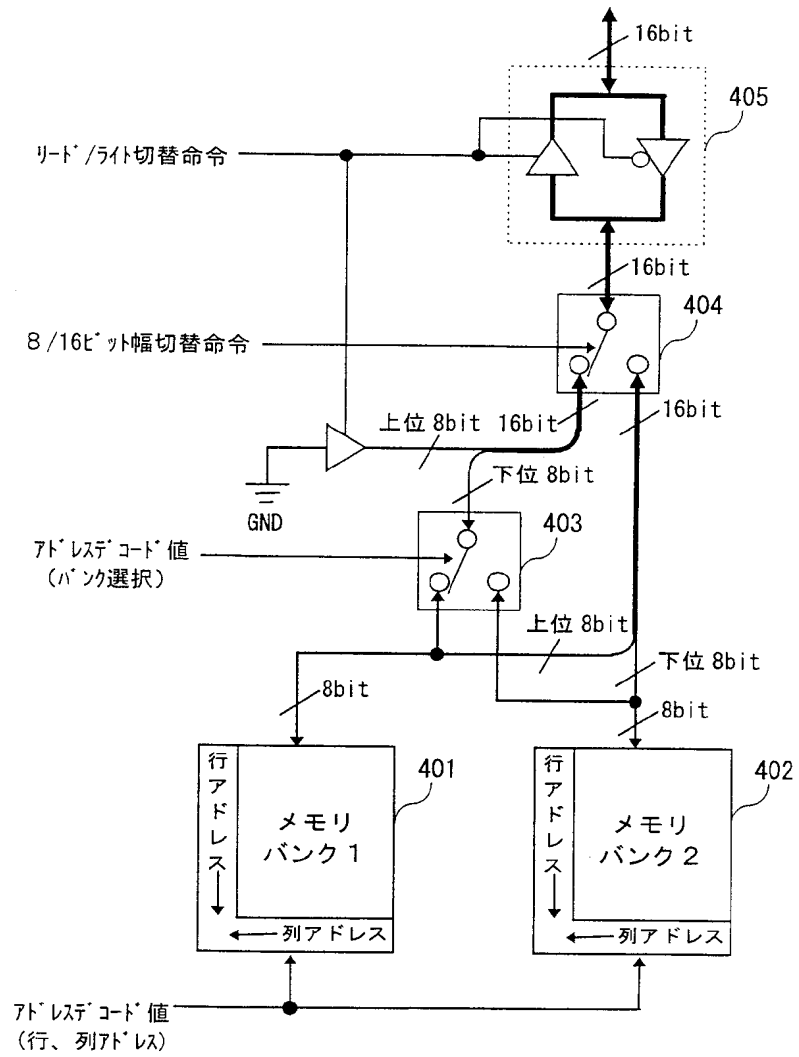
第 2 図



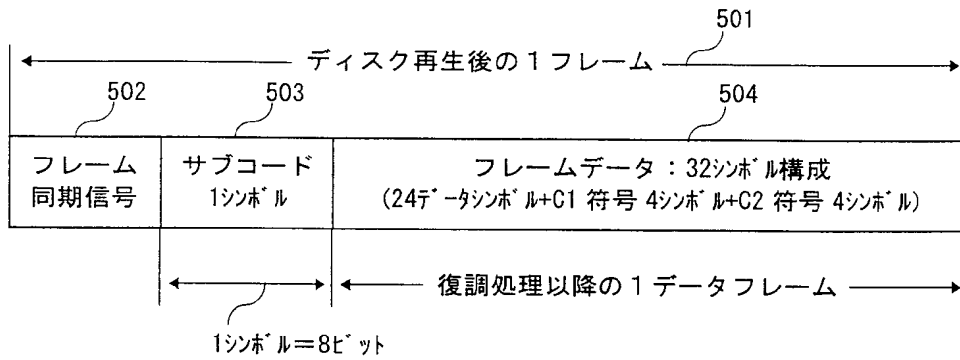
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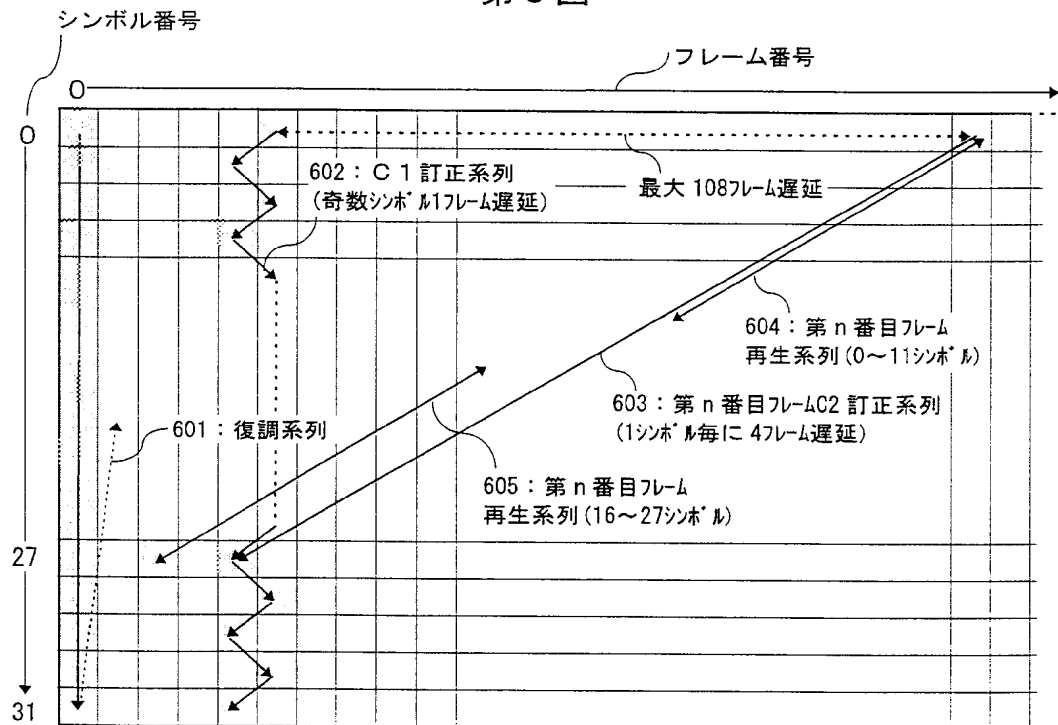
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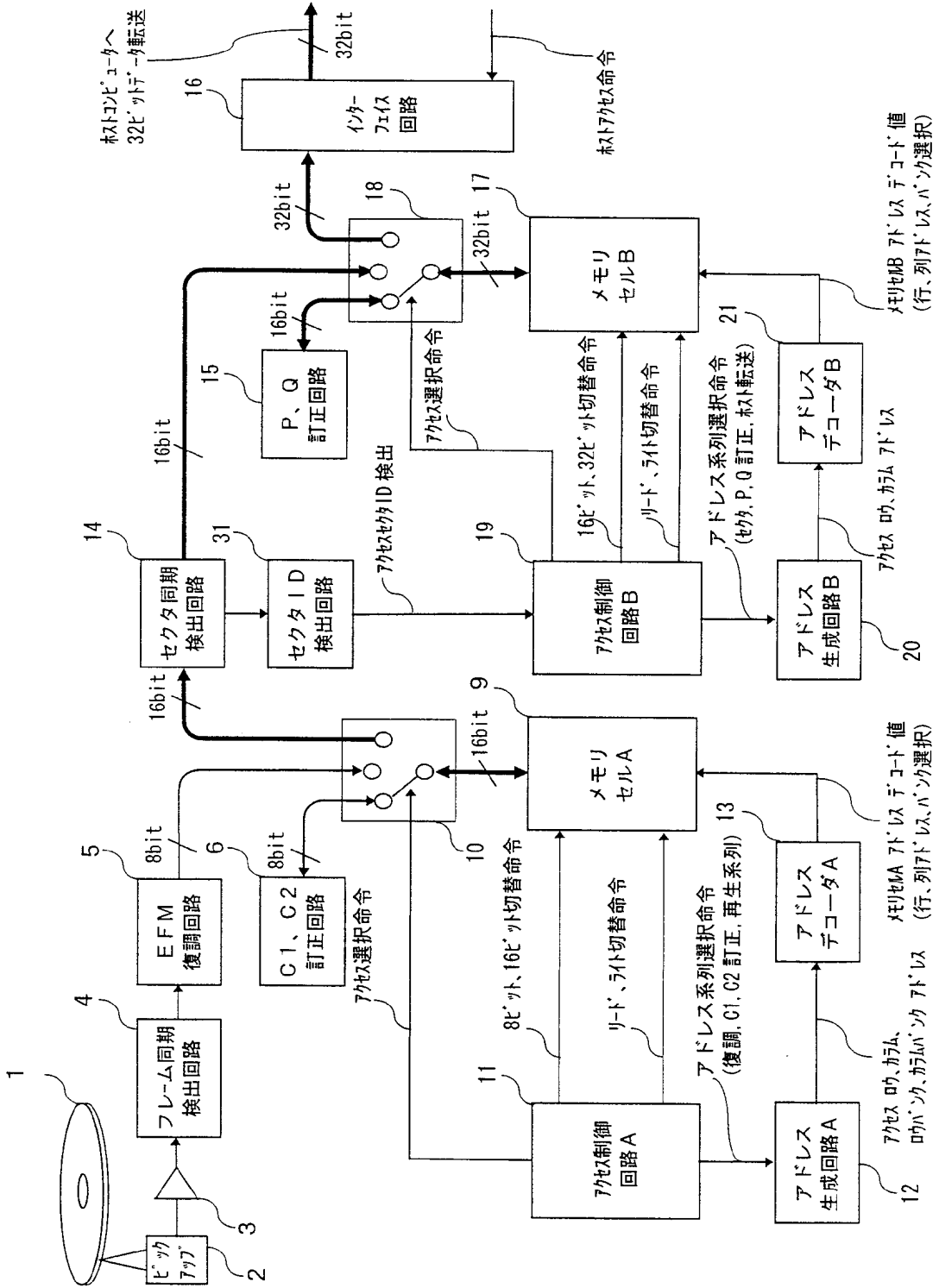
第5図



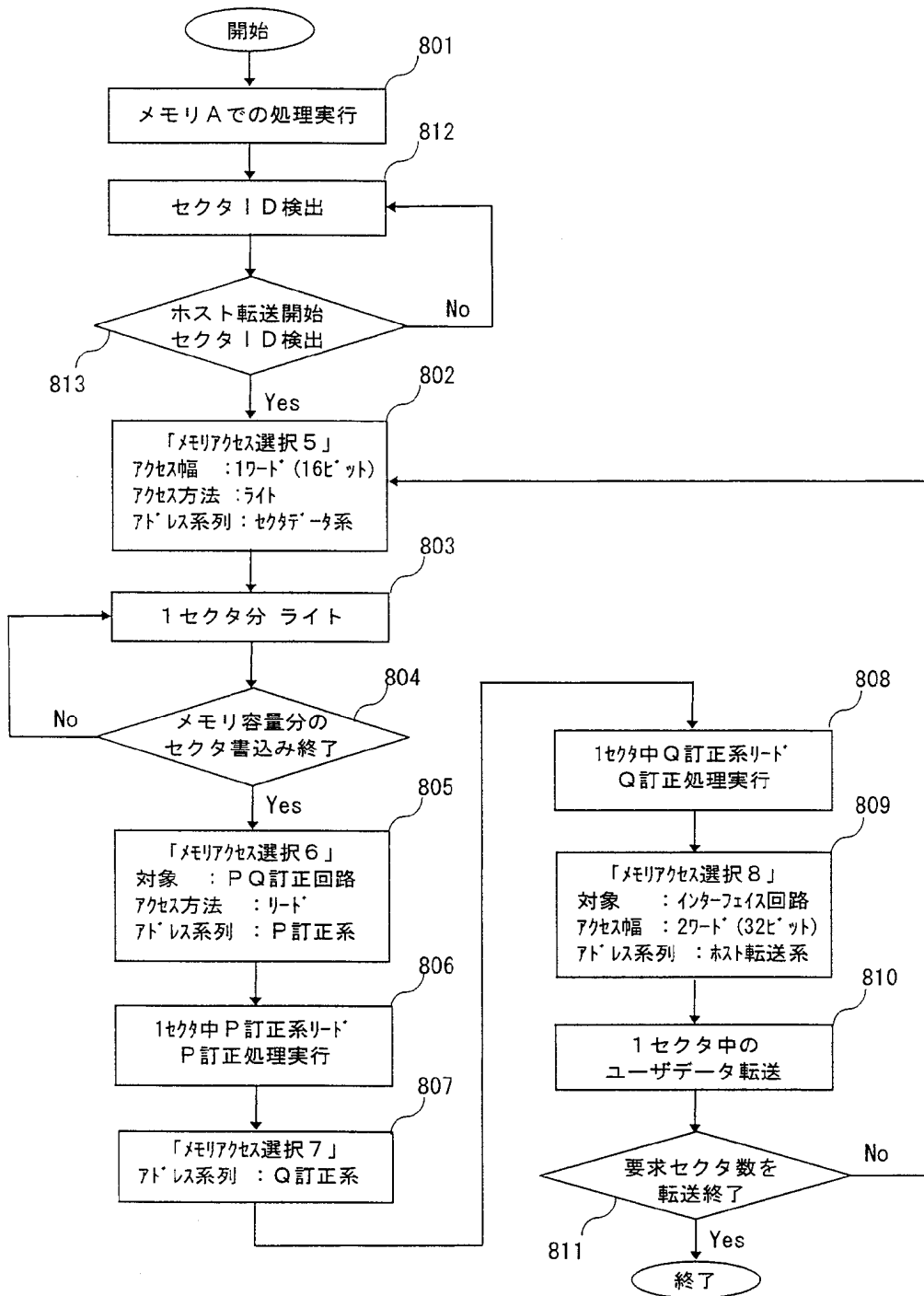
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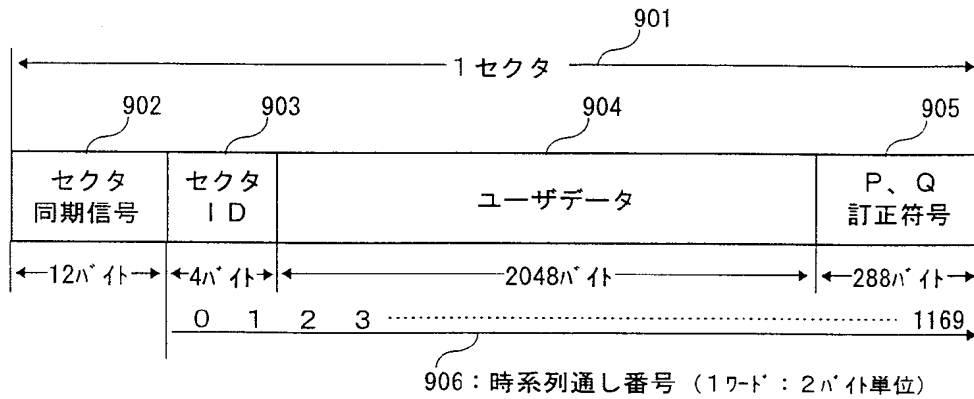
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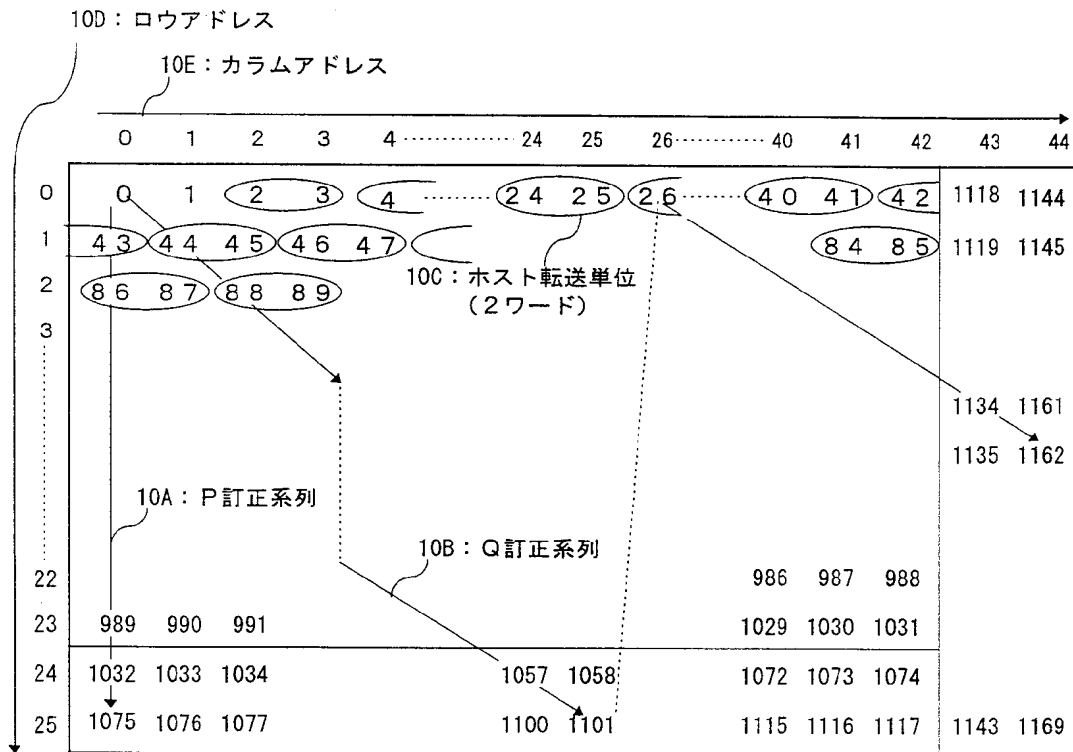
第 8 図



第9図

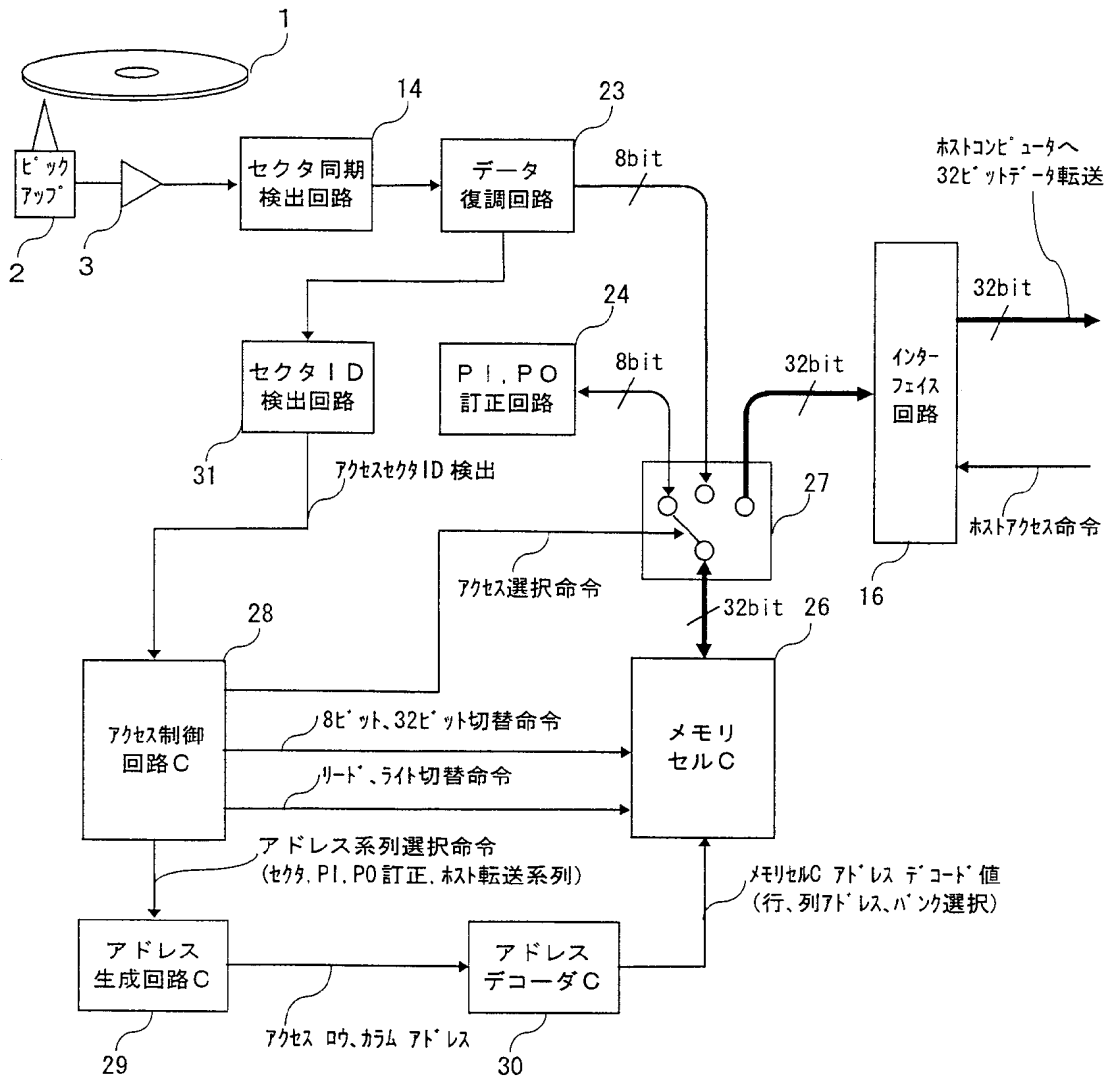


第10図

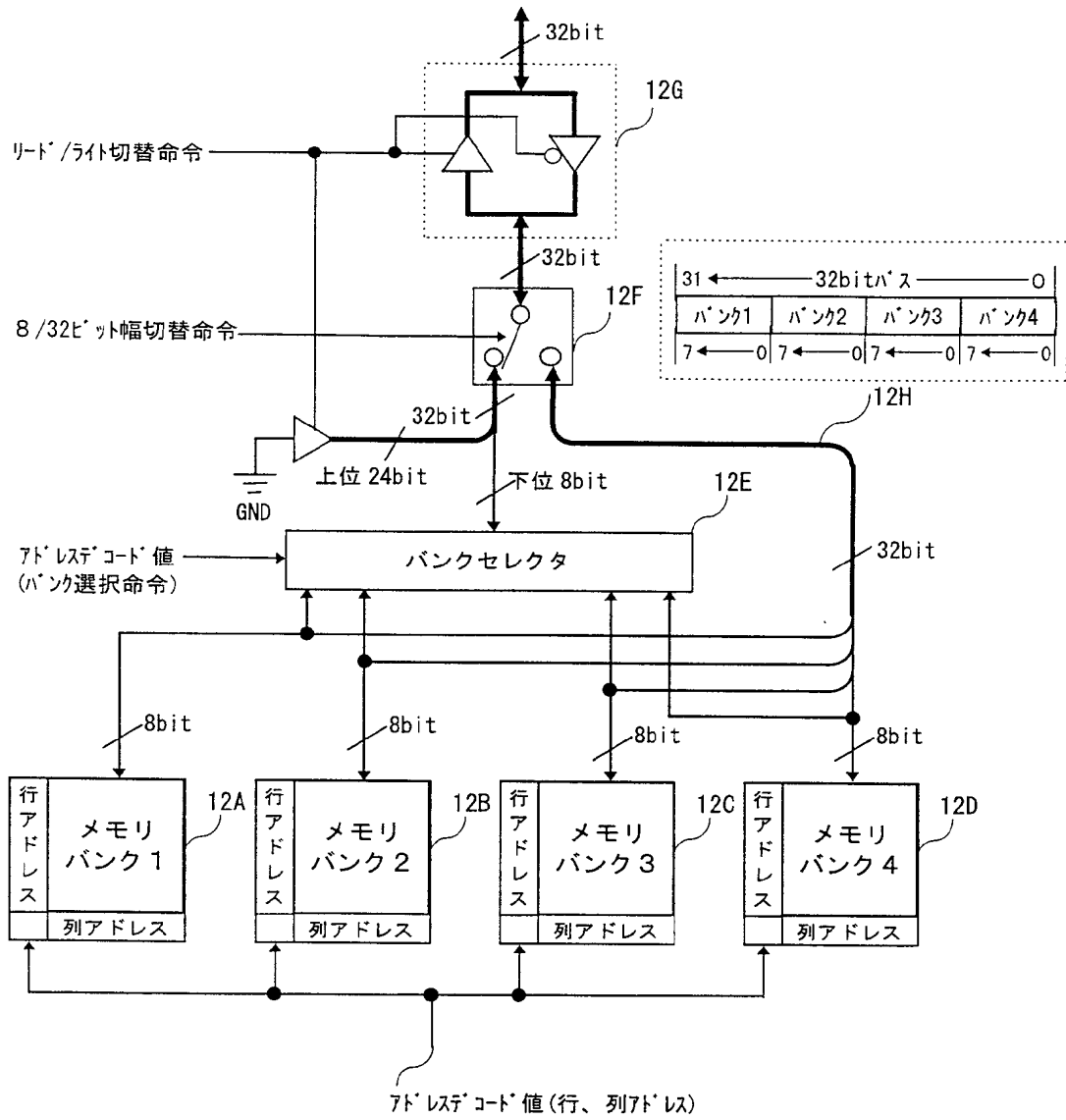


* 番号は時系列データの通し番号。(1ワード単位)
* 0~1031: データ、1032~1117: 訂正符号P、1118~1169: 訂正符号Q

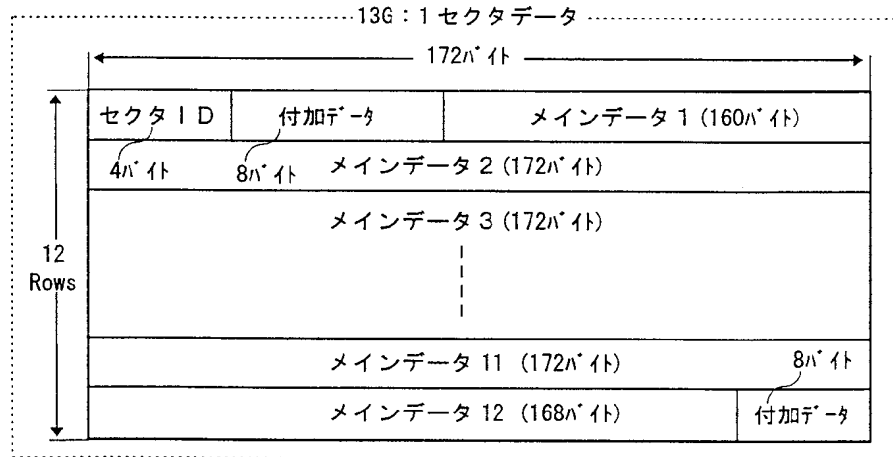
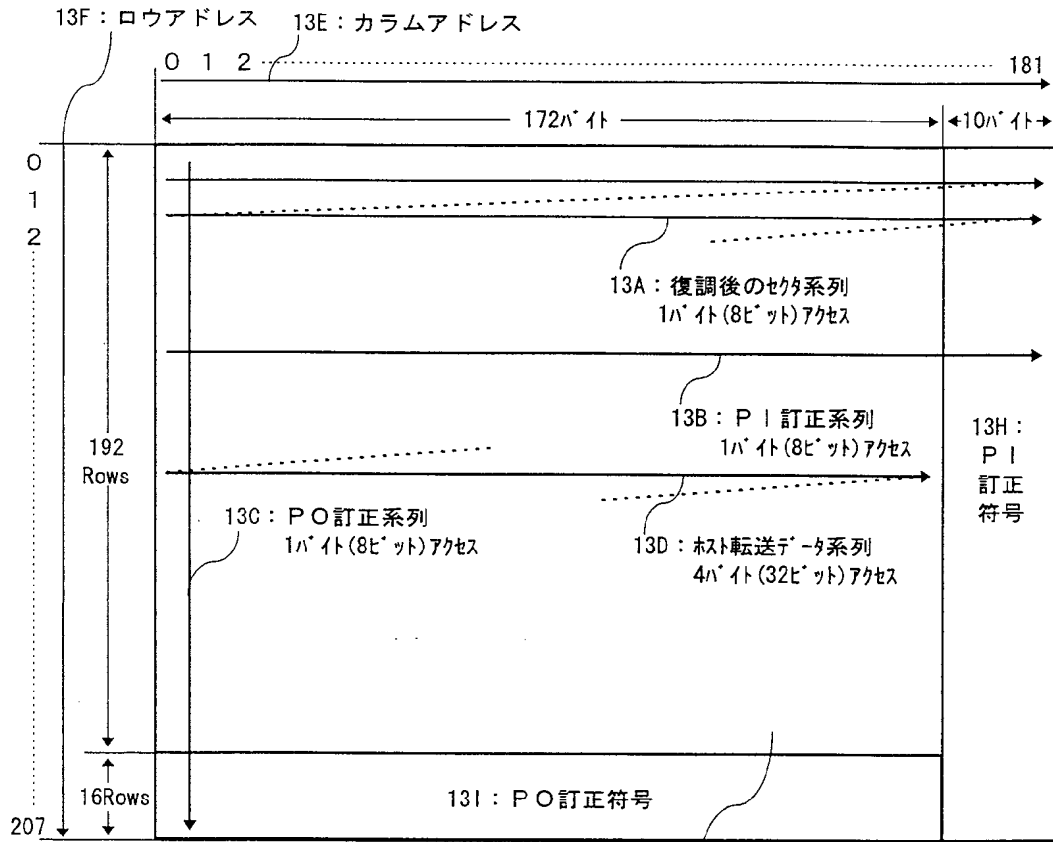
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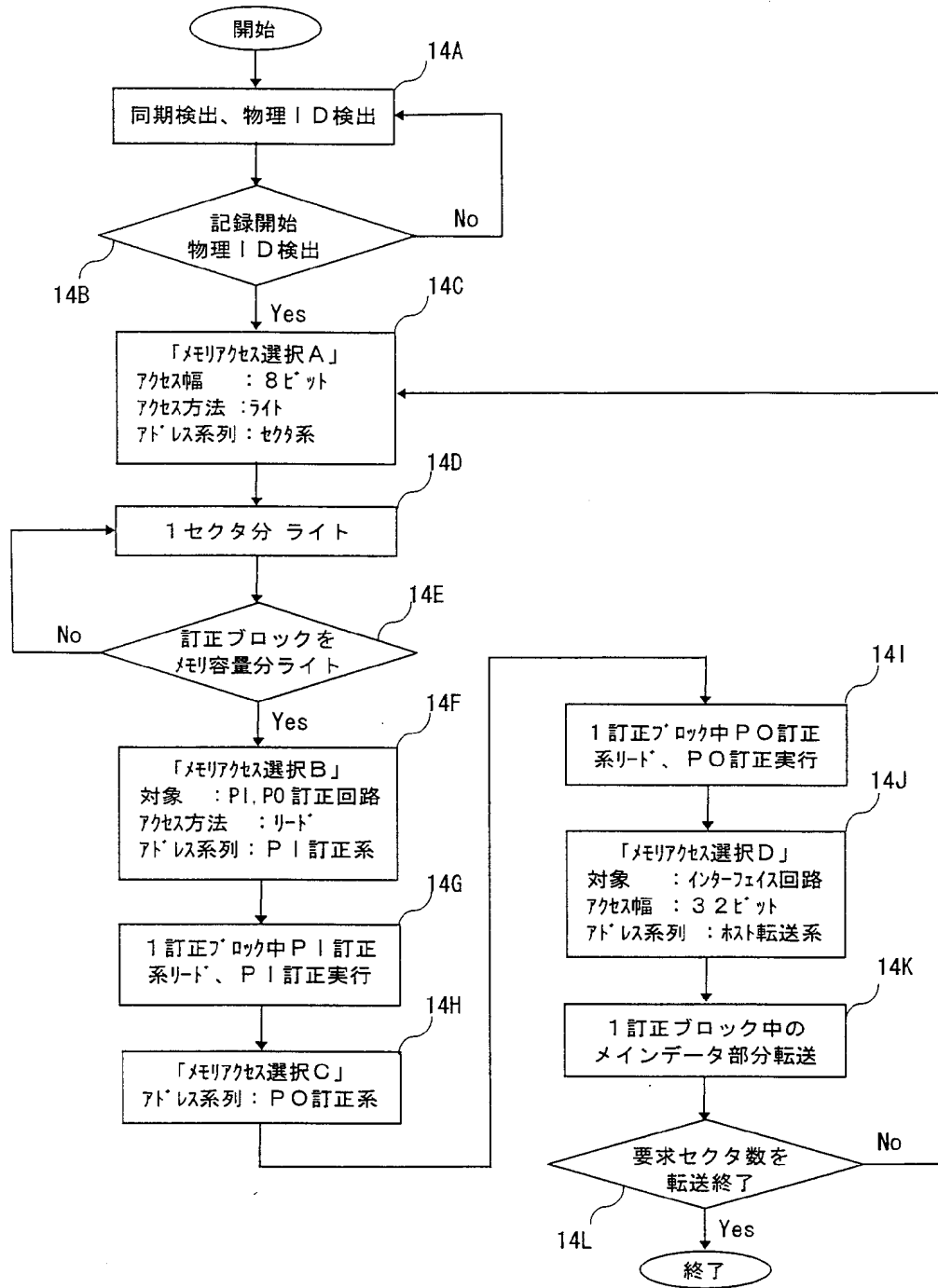
第12図



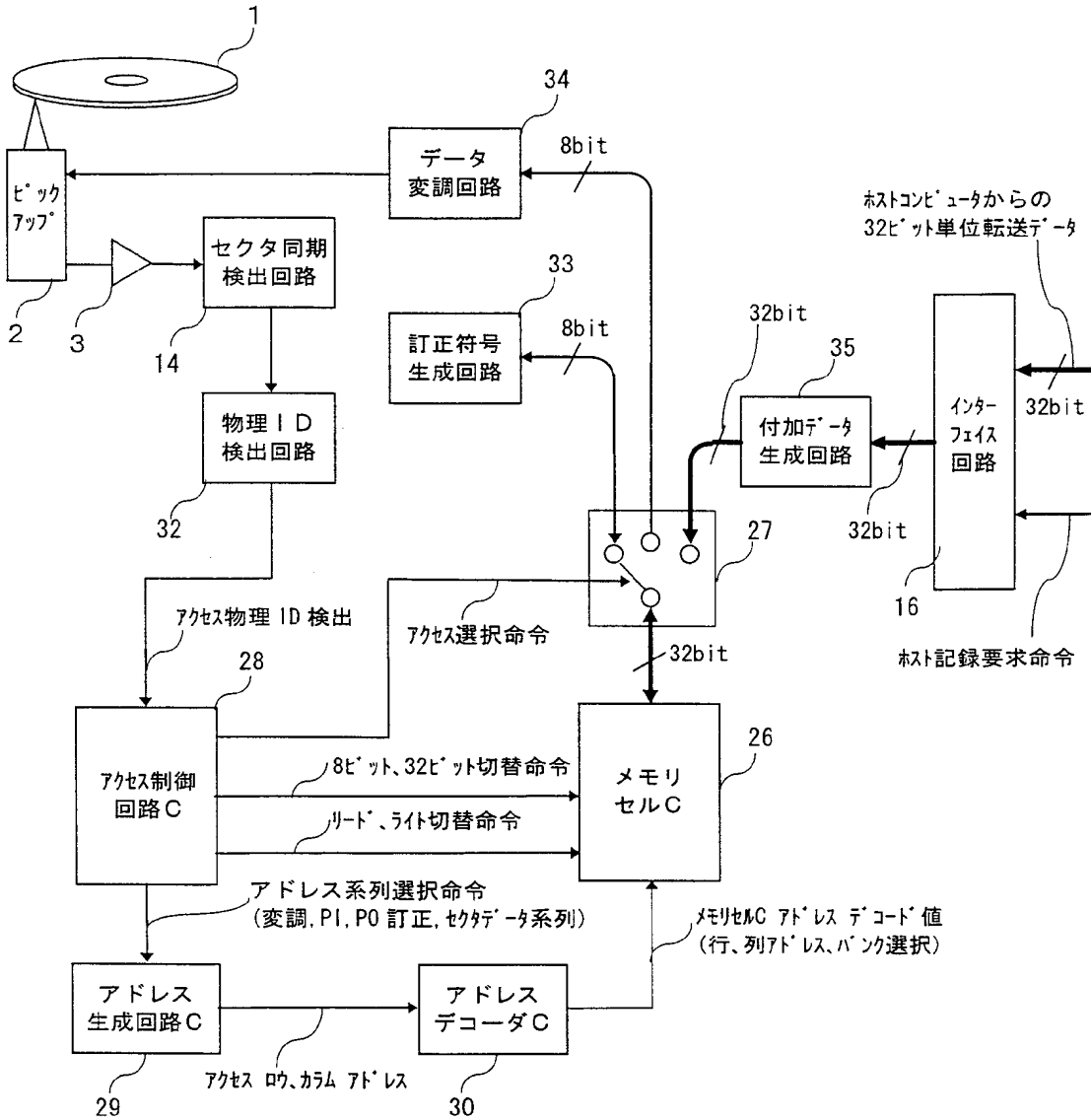
第 1 3 図



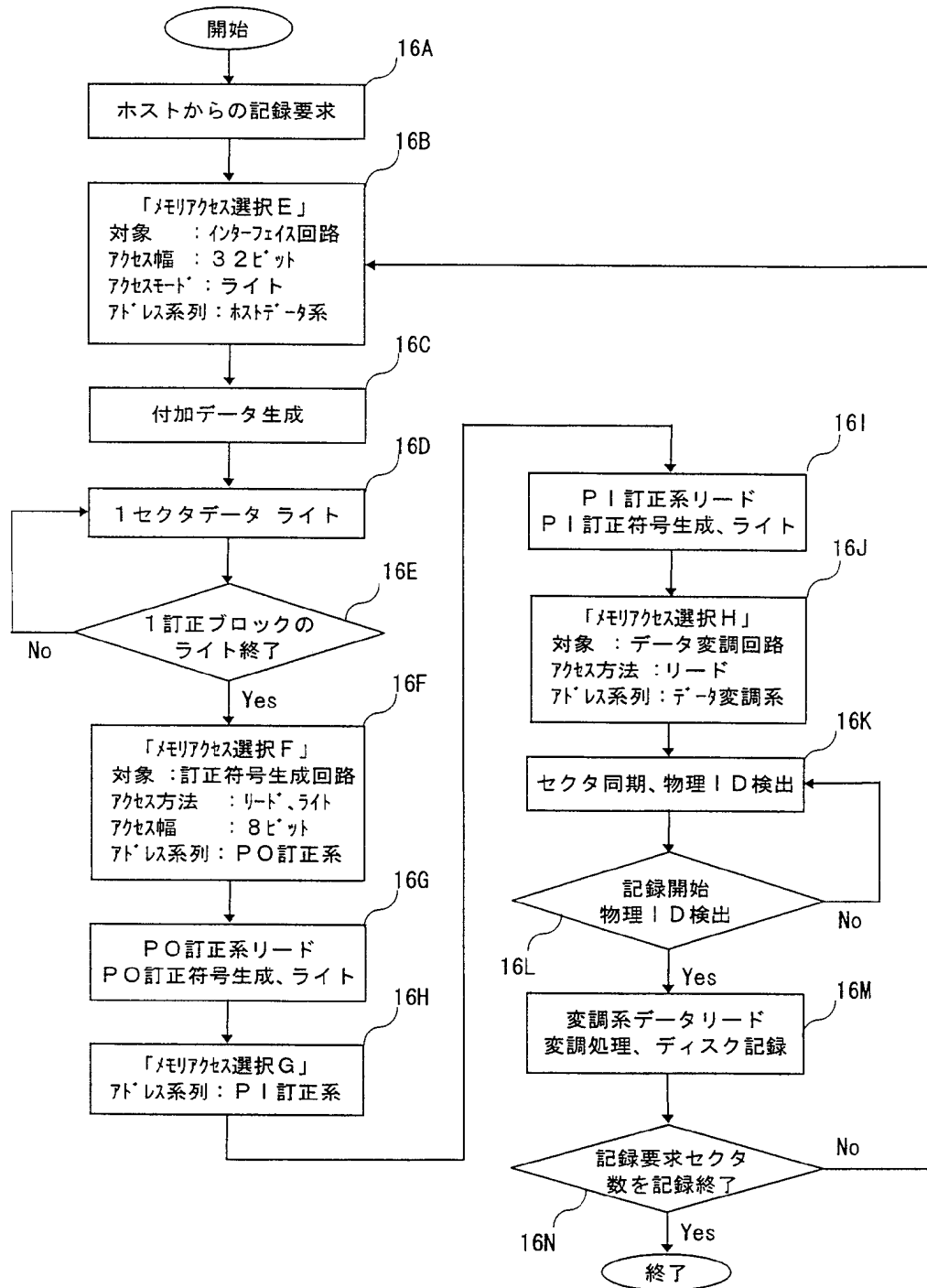
第 1 4 図



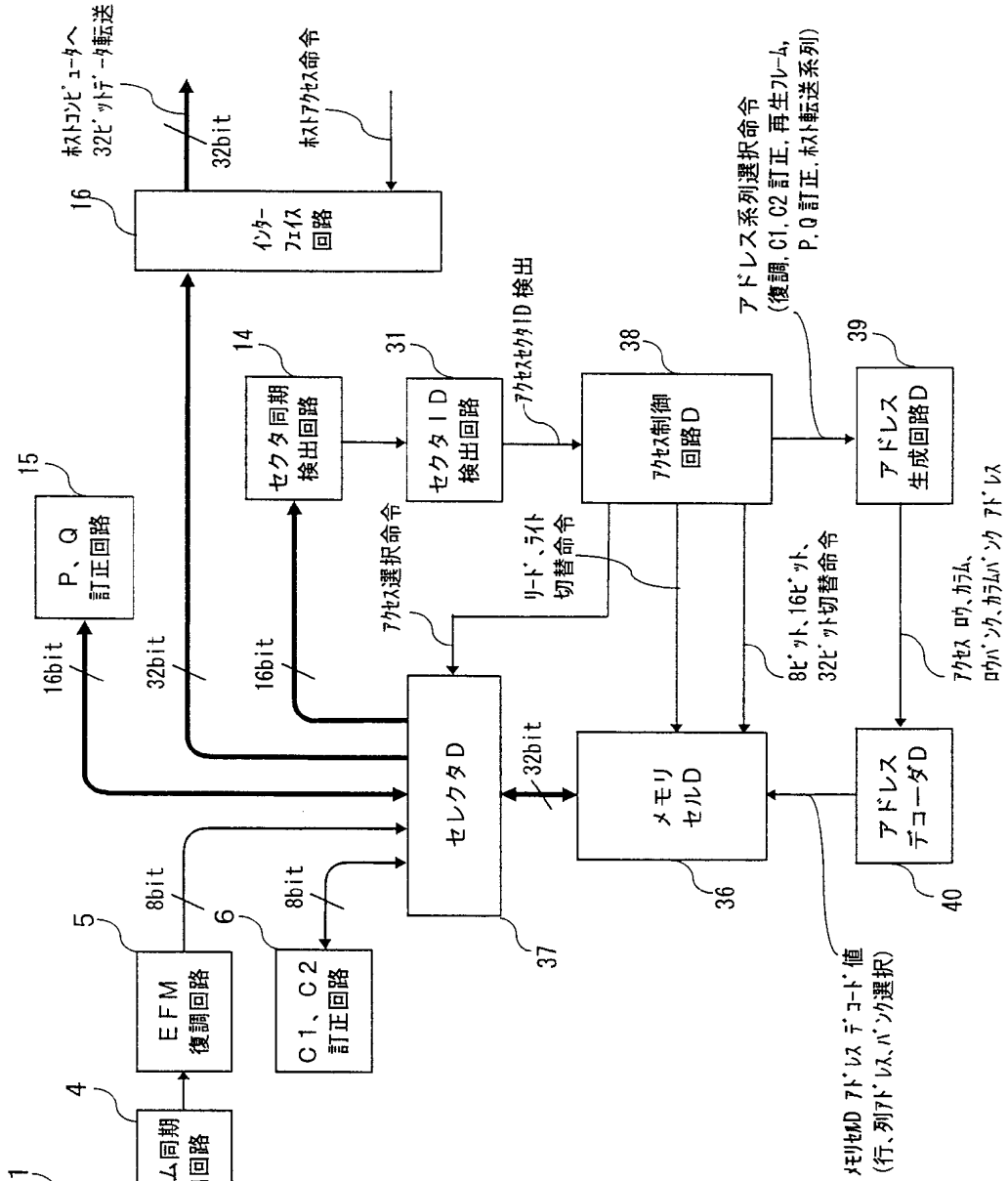
第 15 図



第16図



第 17 図



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP97/00910

A. CLASSIFICATION OF SUBJECT MATTER

Int. C1⁶ G11B20/10, G11C7/00, H03M13/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. C1⁶ G11B20/10, G11C7/00, H03M13/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1940 - 1997	Jitsuyo Shinan Toroku
Kokai Jitsuyo Shinan Koho	1971 - 1997	Koho
Toroku Jitsuyo Shinan Koho	1994 - 1997	1996 - 1997

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 5-12883, A (Nippon Steel Corp.), January 22, 1993 (22. 01. 93) (Family: none)	1 - 22
A	JP, 7-271752, A (NEC Home Electronics Ltd.), October 20, 1995 (20. 10. 95) (Family: none)	1 - 22

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
June 16, 1997 (16. 06. 97)

Date of mailing of the international search report
June 24, 1997 (24. 06. 97)

Name and mailing address of the ISA/
Japanese Patent Office
Facsimile No.

Authorized officer
Telephone No.

A. 発明の属する分野の分類 (国際特許分類 (IPC))

Int. Cl⁶ G11B20/10、G11C7/00、H03M13/22

B. 調査を行った分野

調査を行った最小限資料 (国際特許分類 (IPC))

Int. Cl⁶ G11B20/10、G11C7/00、H03M13/22

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報 1940-1997年
 日本国公開実用新案公報 1971-1997年
 日本国実用新案登録公報 1996-1997年
 日本国登録実用新案公報 1994-1997年

国際調査で使用した電子データベース (データベースの名称、調査に使用した用語)

C. 関連すると認められる文献

引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求の範囲の番号
A	J P, 5-12883, A (新日本製鐵株式会社), 22. 1月. 1993 (22. 01. 93) (ファミリーなし)	1-22
A	J P, 7-271752, A (日本電気ホームエレクトロニクス株式会社), 20. 10月. 1995 (20. 10. 95) (ファミリーなし)	1-22

C欄の続きにも文献が列挙されている。 パテントファミリーに関する別紙を参照。

* 引用文献のカテゴリー
 「A」特に関連のある文献ではなく、一般的技術水準を示すもの
 「E」先行文献ではあるが、国際出願日以後に公表されたもの
 「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献 (理由を付す)
 「O」口頭による開示、使用、展示等に言及する文献
 「P」国際出願日前で、かつ優先権の主張の基礎となる出願日の後に公表された文献
 「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
 「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
 「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
 「&」同一パテントファミリー文献

国際調査を完了した日 16. 06. 97	国際調査報告の発送日 24.06.97
国際調査機関の名称及びあて先 日本国特許庁 (ISA/J P) 郵便番号100 東京都千代田区霞が関三丁目4番3号	特許庁審査官 (権限のある職員) 小松 正 電話番号 03-3581-1101 内線 3551

(19) World Intellectual Property Organization
International Bureau



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31 January 2002 (31.01.2002)

PCT

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(51) International Patent Classification: Not classified

(74) Agent: VERMETTE & CO.; Box 40, 230-200 Granville Street, Granville Square, Vancouver, British Columbia V6C 1S4 (CA).

(21) International Application Number: PCT/CA01/00629

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(72) Inventors; and

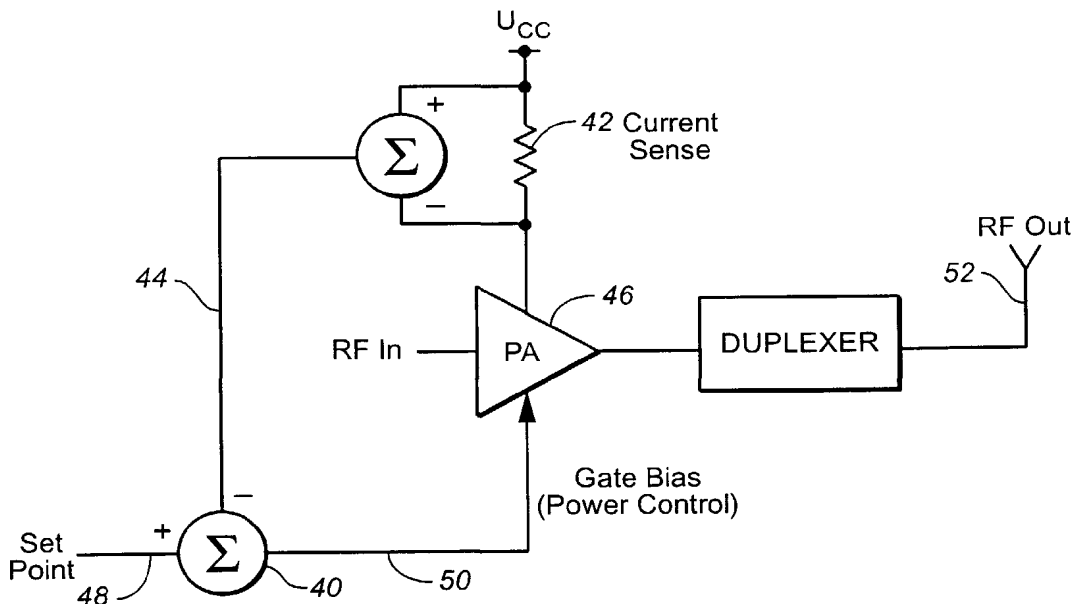
(75) Inventors/Applicants (for US only): MCKEEN, Trent [CA/CA]; 9810 Belfriar Drive, Burnaby, British Columbia V3N 4N1 (CA). LUKAS, Robert, M. [CA/CA]; 5580 Forest Street, Burnaby, British Columbia V5G 3X3 (CA). MILLER, Bruce, M. [CA/CA]; 3242 Samuels Court, Coquitlam, British Columbia V3E 1C8 (CA).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PERSONAL COMPUTER CARD RADIO MODEM USING NON-STANDARD POWER OUTPUT LEVEL



(57) Abstract: A hand-held, PCMCIA cellular radio modem card is described which uses a non-standard power output level. The non-standard power output is defined as the maximum RF power attainable such that the current drawn by the power amplifier does not exceed 400 mA. This definition permits the use of the wireless modem inside hand-held computing devices without the use of an additional battery pack extension.



WO 02/07494 A2

**PERSONAL COMPUTER CARD RADIO MODEM
USING NON-STANDARD POWER OUTPUT LEVEL**

Background of the Invention

The present invention relates to personal computer (PC) card radio modems.

5 Small hand-held personal computing devices can use Personal Computer Memory Card Interface Association (PCMCIA) radio modems to connect to a wireless network. PC card radio modems typically use battery power from the hand-held PC or from a battery pack extension.

10 A problem that exists in prior-art systems in which the wireless modem operates on a network such as the North American AMPS or CDPD network, is a battery pack extension is used to supplement the power supplied to the wireless modem. Typically, hand-held PCs use two AA batteries, which suffer from low capacity and a low peak current capability.

15 Six different standard RF power levels are required by the CDPD standard (CDPD R1.1 Part 409) and the AMPS standard (IS-19B) for a class III cellular device. With two AA batteries supplying the hand-held PC and the PCMCIA wireless card, it is difficult to achieve the highest RF power level; which, for a class III cellular device, is an output power of 28 dBm where 0 dBm is 1mW output power. Typically, prior art uses a battery pack extension on the PCMCIA card to achieve the highest RF power output.

20 This is an undesirable solution as the esthetics of the complete product are poor.

It is desirable to have an improved system, which avoids some of the problems of the prior art.

Summary of the Invention

25 In one embodiment, the present invention relates to a PC card radio transceiver which uses a non-standard power output level. The non-standard power output level is limited by the peak sustainable current available from the battery inside the hand-held PC. In one embodiment, this current is limited to 600 mA. The non-standard RF power

-2-

obtainable, given a 600mA maximum limit, is typically between 24 dBm and 28 dBm (in one implementation, 26.5 dBm). The non-standard power output level has a nominal value less than the nominal value required by the standard, yet is still within the acceptable range (+2, -4dB) specified in the standard.

5 The advantage of the present invention is that the radio transceiver in the PC card can operate while attached to a hand-held PC without requiring a battery pack extension. The system allows the two AA batteries of the hand-held PC to produce an acceptable, high-level RF output power.

10 Implementation of a non-standard RF power level, which is based on a current restriction, requires the automatic leveling circuit (ALC) of the power amplifier to be a current leveling circuit as opposed to a power leveling circuit as in prior art systems. A current leveling circuit achieves the same effect as a power leveling circuit, given the load on the power amplifier remains constant. In practice, this is a reasonable assumption.

15

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating a PCMCIA cellular modem attached to a hand-held PC.

20 Fig. 2 is a diagram illustrating the power amplifier, current leveling circuit, duplexer and antenna used in the PC card cellular radio transceiver of one embodiment of the present invention.

Fig. 3 is a diagram illustrating both the implemented and non-implemented standard power output levels as well as the non-standard power output level of one embodiment of the present invention.

25 Fig. 4 is a block diagram illustrating one embodiment of the current leveling system of the present invention.

Fig. 5 is a schematic illustrating one embodiment of the current leveling circuit for one embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Fig. 1 is a block diagram that illustrates a hand-held personal computer 20 and PC card 22. In one embodiment, the PC card is a cellular modem with a built-in radio transceiver.

5 The hand-held PC 20 sends signals to be transmitted to the PC card cellular modem 22. Additionally, the hand-held PC supplies power for the operation of the PC card cellular modem 22. Typically, two AA batteries in the hand-held PC power both the hand-held PC and the PC card cellular modem 22. Since relatively small batteries are used, the maximum current which can be drawn by the PC card cellular modem 22 is
10 limited to less than what is needed to meet the nominal output power requirements of IS-19B and CDPD Part 409 standards given present power amplifier and duplexer technologies. In one embodiment, the PC card cellular modem 22 should not draw more than 600 mA of current.

Fig. 2 is a simplified diagram of the elements in the PC card cellular modem of
15 one embodiment of the present invention. A current leveling circuit 32 controls the current supplied to power amplifier 30 and hence indirectly controls the output power of amplifier 30. In a PC card cellular modem, the current supplied to the power amplifier makes up a large percentage of the total current consumed by the device. The output of the power amplifier 30 is sent to a duplexer 34, then out the antenna 36.

20 In the present invention, the current leveling circuit 32 limits the current used by the power amplifier 30 at the highest power output level. This highest power output level is the non-standard power output level described below.

In one embodiment, the current leveling circuit 32 limits the current drawn by the power amplifier 30 to 400 mA when it is transmitting at the highest output power level. The
25 current consumption of the entire card is therefore limited to 600mA.

Fig. 3 illustrates the RF output levels for the standard and non-standard power outputs for CDPD standard R.1.1 Part 409 and AMPS standard IS-19B. There are six standard output power levels for a class III cellular device. The standard, nominal power

-4-

output levels range from 8 to 28 dBm in 4 dB steps. In one embodiment, the non-standard power output level is between the highest standard power level, which is not implemented (28 dBm), and the highest implemented power level (24 dBm). In one embodiment, by limiting the current draw by the power amplifier to 400 mA or less (the total PC card current draw to 600mA or less), the non-standard power output level is about 26.5 dBm. This level is below the nominal 28 dBm power level specified in the standard, yet still falls within the acceptable range of +2dB to -4dB from nominal specified in the standard.

Fig. 4 is a block diagram of a circuit to implement one embodiment of the present invention. A set point value 48 is sent to adder 40 and combined with a feedback value on line 44 from current-sensor 42 to produce a gate bias (power control) signal for power amplifier 46. The set point values are controlled by the micro-processor. Each set point value corresponds to a power output level for the power amplifier 46. The current leveling circuit limits the power output by the power amplifier. In a preferred embodiment, the maximum set point value is such that the current drawn by the power amplifier is less than 400 mA.

Fig. 5 illustrates details of one embodiment of the current leveling circuitry for operation with the PC card radio transceiver of the present invention.

Other modifications and implementations will occur to those skilled in the art, without departing from the spirit and scope of the present invention. Accordingly, the above description is not intended to limit the invention, which is to be limited only by the following claims.

-5-

Claims:

1. A PC radio card adapted to be connected to and powered by a hand-held personal computer, the PC radio card using a number of output power levels controlled by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.
2. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is such that the current drawn by the power amplifier is 400 mA or less.
3. The PC radio card of Claim 1 wherein the PC radio card includes a current control automatic leveling circuit, keeping the current supplied to the power amplifier less than 400 mA.
4. The PC radio card of Claim 1 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.
5. The PC radio card of Claim 1 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm, wherein an output of 0 dBm is calibrated to 1 mW of output power.
6. A PC radio card adapted to be connected to and powered by a hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-

-6-

limited power output level, the nonstandard battery-limited power output level being such that the current drawn by the power amplifier is 400mA or less.

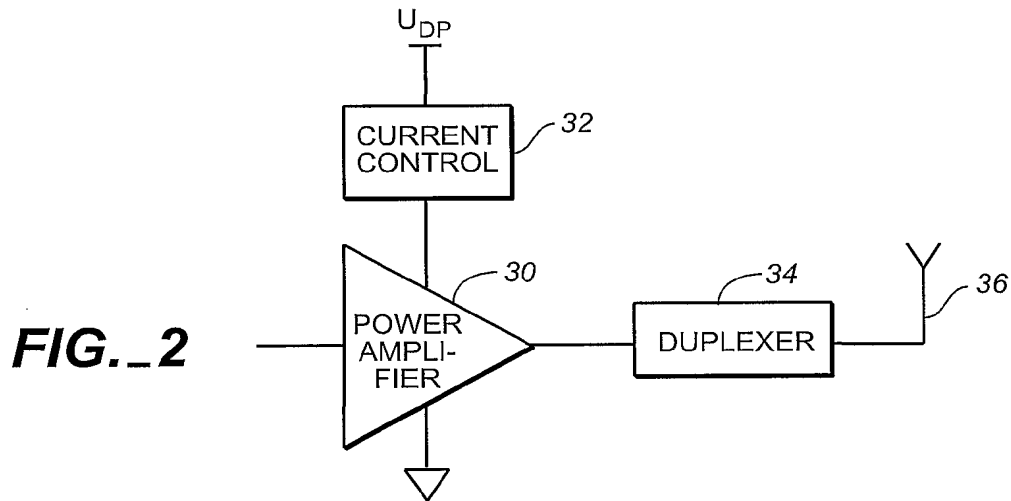
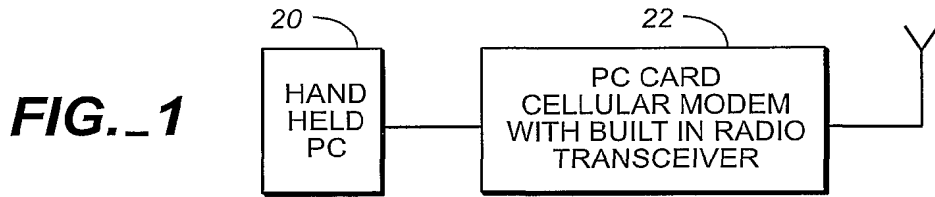
7. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.
8. The PC radio card of Claim 6 wherein the PC radio card is powered by a hand-held personal computer using two AA batteries.
9. The PC radio card of Claim 6 wherein the PC radio card has a current controlled automatic leveling circuit to limit the current supplied to the power amplifier.
10. The PC radio card of Claim 6 wherein the non-standard battery-limited power output level is less than 28 dBm and more than 24 dBm when 0 dBm is calibrated to one mW of output power.
11. A system including:
 - a battery-powered hand held personal computer; and
 - a PC radio card connected to and powered by the hand held personal computer, the PC radio card using a number of output power levels set by current supplied to power amplifier in the PC radio card, the output power levels including multiple implemented standard power output levels and a nonstandard battery-limited power output level, the nonstandard battery-limited power output level being greater than the multiple implemented standard power output levels but less than an unimplemented standard power output level.
12. The system of Claim 11 wherein the nonstandard battery-limited power level is such that the current drawn by the power amplifier is 400 mA or less.

-7-

13. The system of Claim 11 wherein the hand-held personal computer is powered two AA batteries
14. The system of Claim 11 wherein the nonstandard battery-limited power level limits the current supplied by the hand-held personal computer to the PC radio card to less than a given amount.
15. The system of Claim 11 further comprising a current controlled automatic leveling circuit in the PC radio card to limit the current supplied to the power amplifier.
16. A PC card transceiver including:
an antenna;
an amplifier operably connected to the antenna;
a current controller operably connected to the amplifier to set the power output of the transceiver, the current controller adapted to produce a number of standard transceiver power output levels and a nonstandard transceiver output power level, the nonstandard transceiver output power level being such that the amplifier current is at a level that makes efficient use of the PC card transceiver batteries.
17. The PC card of Claim 16, further comprising a duplexer operatively positioned between the amplifier and the antenna.
18. The PC card of Claim 16 wherein the non-standard battery-limited power output level is greater than the implemented standard but less than an unimplemented standard power output level.
19. The PC card transceiver of Claim 16 wherein the amplifier is limited to 400 mA of current draw.

-8-

20. The PC card transceiver of Claim 16 wherein the PC card transceiver is adapted to be powered by a hand-held personal computer.



STANDARD
POWER OUTPUT LEVELS

- | | | |
|-----------------|---|------------|
| Not Implemented | { | 0 + 28 dBm |
| | | 1 + 28 dBm |
| | | 2 + 28 dBm |
| Implemented | { | 3 + 24 dBm |
| | | 4 + 20 dBm |
| | | 5 + 16 dBm |
| | | 6 + 12 dBm |
| | | 7 + .8 dBm |

NON-STANDARD
POWER OUTPUT LEVEL

Maximun RF output power such that the power drawn by the PC card is less than 600mA. ~ 26.5 dBm

FIG._3

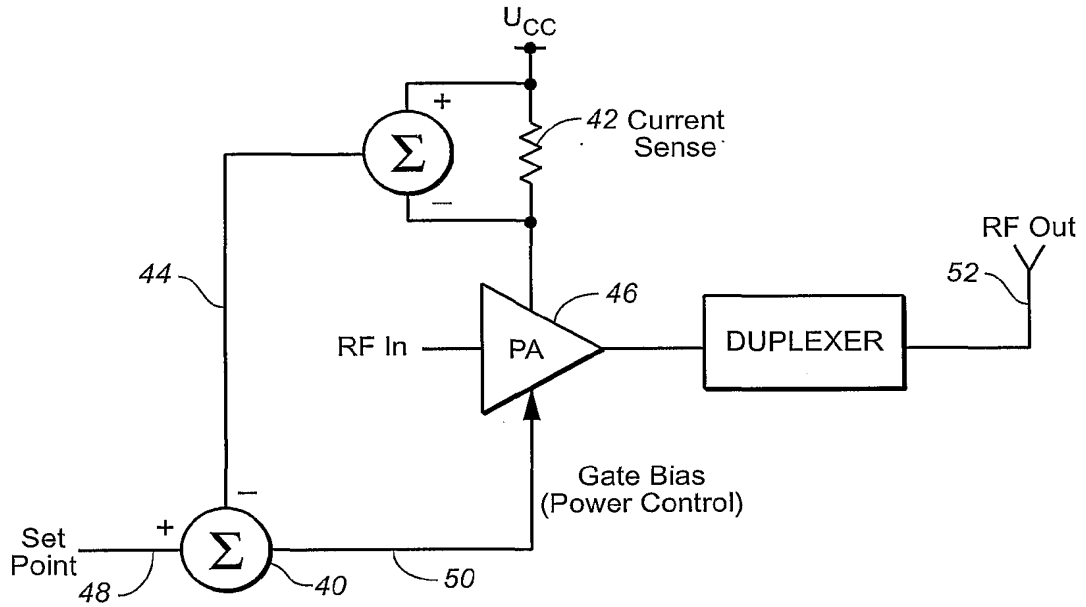


FIG. 4

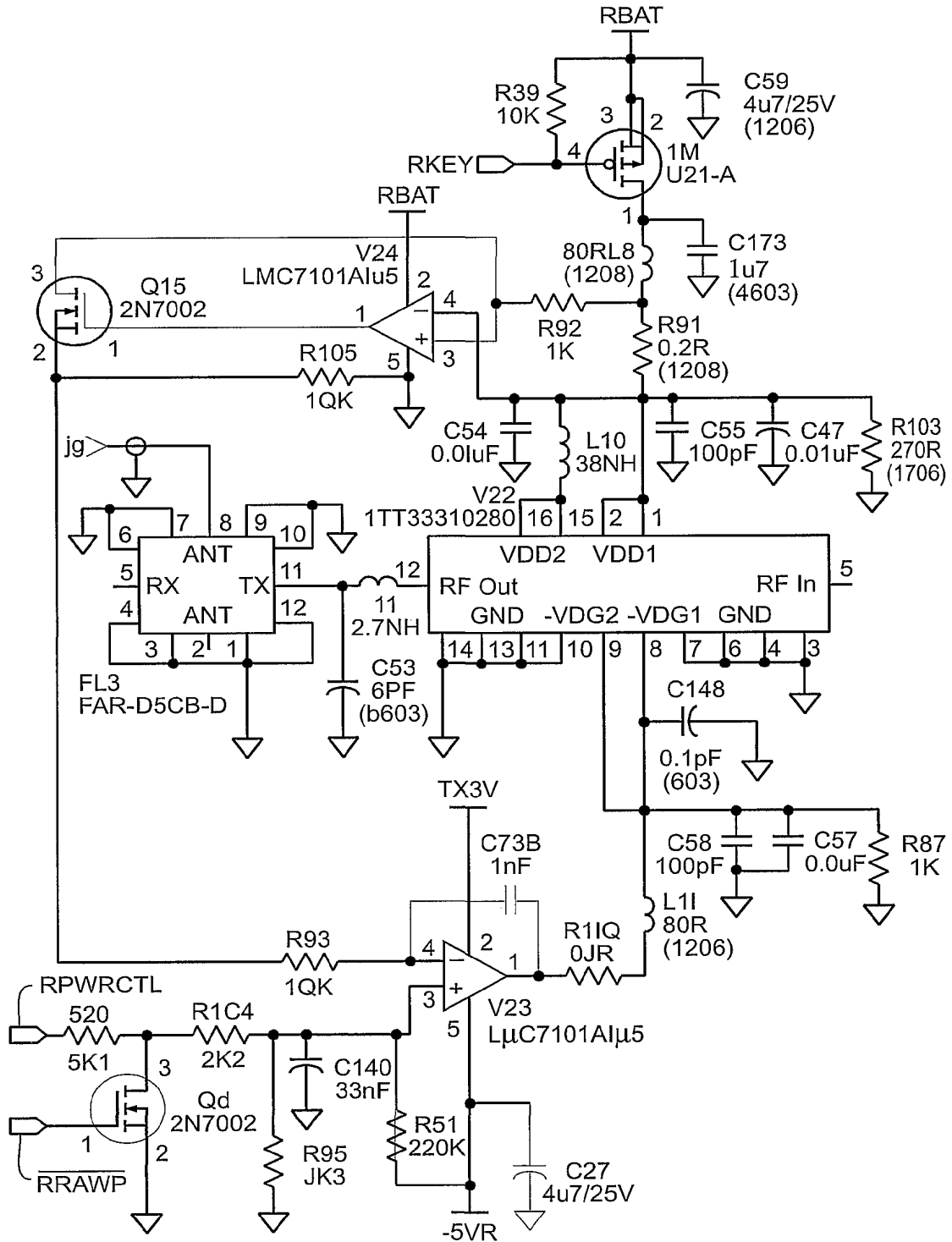


FIG. 5 Schematic for Current Control ALC

INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 03/00233

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G06F 1/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G06F, H04M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5884086 A (S.AMONI ET AL), 16 March 1999 (16.03.99), column 2, line 40 - line 44; column 7, line 15 - line 26	1-5,9-10, 14-21,25-26
Y	--	6-8,11-13, 22-24
X	WO 0207494 A2 (SIERRA WIRELESS,INC.), 31 January 2002 (31.01.02), page 1 - page 2	1-5,9-10, 14-21,25-26
X	US 5758171 A (S.RAMAMURTHY ET AL), 26 May 1998 (26.05.98), column 4, line 49 - column 5, line 32	1-5,9-10, 14-21,25-26

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search

27 June 2003

Date of mailing of the international search report

27 -06- 2003

Name and mailing address of the ISA/
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 03/00233

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6178514 B1 (B.C.WOOD), 23 January 2001 (23.01.01), column 4, line 32 - line 45; column 5 --	1-5,9-10, 14-21,25-26
Y	US 5737616 A (MITSUHIRO WATANABE), 7 April 1998 (07.04.98), column 3, line 25 - line 32 --	6,11,22
Y	GB 2235797 A (APPLE COMPUTER INC), 13 March 1991 (13.03.91), page 6 --	6,11,22
Y	US 5758108 A (AKLYOSHI NAKASMURA), 26 May 1998 (26.05.98), column 1, line 32 - line 44 --	6,7,11,12, 22,23
Y	WO 9841987 A1 (HITACHI, LTD.), 24 Sept 1998 (24.09.98), abstract --	7-8,12,13, 23,24
Y	US 4841440 A (KAZUYA YONEZU ET AL), 20 June 1989 (20.06.89), column 1, line 58 - line 68 -- -----	8,13,24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI03/00233

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

- 1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

- 2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

- 3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see extra sheet

- 1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
- 2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
- 3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

- 4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest.
- No protest accompanied the payment of additional search fees.

This International Search Authority found multiple inventions as follows:

I claims 1-5, 9-10, 14-21 and 25-26 directed to a system, a device and a method for determining levels of power consumption in an electronic device.

II claims 6-8, 11-13 and 22-24 directed to a system, a device and a method for controlling the power consumption in an electronic device.

From for instance US 5884086 a system and a method are known for supplying power to peripheral devices in a computer system. According to the document, the peripheral device communicates its power requirements to the host system. The power requirements are characterized in for instance 64 different levels (column 7, lines 15-26).

The problem solved by the first invention is an alternative arrangement for determining levels of power required.

The technical feature of invention II is characterized by three different ways of controlling the power consumption:

II:a -adjusting the frequency of at least one clock signal

II:b -controlling the bus width

II:c -controlling the number of storage blocks processed

The problem solved is alternatives in methods of controlling power consumption. The technical features of claims 6-8 and corresponding claims referring to the independent claims, are three different. However, the features could be searched without effort justifying three additional fees and are thus grouped as one additional invention having the special technical feature of controlling the power consumption.

Inventions I and II have in common only the feature of claim 1. However, a person skilled in the art, faced with the problem of determining levels, finds this information in US 5884086.

Consequently the common feature is not a special technical feature within the meaning of PCT Rule 13.2, second sentence, since it makes no contribution over prior art.

Since there exists no other common feature which can be considered as a special technical feature within the meaning of PCT Rule 13.3, second sentence, no technical relationship within the meaning of PCT Rule 13 between the different inventions can be seen.

Consequently it appears that, a posteriori, the claims of inventions I and II do not satisfy the requirement of unity of invention.

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/06/03

International application No.

PCT/FI 03/00233

Patent document cited in search report			Publication date	Patent family member(s)		Publication date
US	5884086	A	16/03/99	NONE		
WO	0207494	A2	31/01/02	AU	5809001 A	05/02/02
				EP	1301998 A	16/04/03
				NO	20030291 A	21/03/03
US	5758171	A	26/05/98	NONE		
US	6178514	B1	23/01/01	NONE		
US	5737616	A	07/04/98	CA	2176677 A	16/11/96
				JP	8314587 A	29/11/96
GB	2235797	A	13/03/91	AU	629019 B	24/09/92
				AU	6016890 A	14/03/91
				CA	2024552 A	09/03/91
				DE	4028175 A	21/03/91
				GB	9018259 D	00/00/00
				HK	36394 A	29/04/94
				JP	3171317 A	24/07/91
				SE	9002838 A	09/03/91
				SG	7294 G	10/06/94
				US	5167024 A	24/11/92
US	5758108	A	26/05/98	JP	8147076 A	07/06/96
WO	9841987	A1	24/09/98	NONE		
US	4841440	A	20/06/89	JP	1013573 B	07/03/89
				JP	1530059 C	15/11/89
				JP	59200327 A	13/11/84

PATENT COOPERATION TREATY

PCT

REC'D 24 JUN 2004

WIPO

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TP101979/TPU	FOR FURTHER ACTION See Form PCT/IPEA/416	
International application No. PCT/FI 2003/000233	International filing date (day/month/year) 26-03-2003	Priority date (day/month/year) 27-03-2002
International Patent Classification (IPC) or national classification and IPC G06F 1/26		
Applicant NOKIA CORPORATION et al		

- This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
- This REPORT consists of a total of 7 sheets, including this cover sheet.
- This report is also accompanied by ANNEXES, comprising:
 - (sent to the applicant and to the International Bureau) a total of _____ sheets, as follows:
 - sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
 - sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
 - (sent to the International Bureau only) a total of _____ (indicate type and number of electronic carrier(s)) _____, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

- | | | |
|-------------------------------------|--------------|---|
| <input checked="" type="checkbox"/> | Box No. I | Basis of the report |
| <input type="checkbox"/> | Box No. II | Priority |
| <input type="checkbox"/> | Box No. III | Non-establishment of opinion with regard to novelty, inventive step and industrial applicability |
| <input checked="" type="checkbox"/> | Box No. IV | Lack of unity of invention |
| <input checked="" type="checkbox"/> | Box No. V | Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement |
| <input type="checkbox"/> | Box No. VI | Certain documents cited |
| <input type="checkbox"/> | Box No. VII | Certain defects in the international application |
| <input type="checkbox"/> | Box No. VIII | Certain observations on the international application |

Date of submission of the demand 08-10-2003	Date of completion of this report 15-06-2004
Name and mailing address of the IPEA/SE Patent- och registreringsverket Box 5055 S-102 42 STOCKHOLM Facsimile No. +46 8 667 72 88	Authorized officer Sture Elnäs /itw Telephone No. +46 8 782 25 00

Form PCT/IPEA/409 (cover sheet) (January 2004)

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.

PCT/FI 2003/000233

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

- This report is based on a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of:
 - international search (under Rules 12.3 and 23.1(b))
 - publication of the international application (under Rule 12.4)
 - international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements** of the international application, this report is based on (*replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report*):

- the international application as originally filed/furnished
- the description:
 - pages _____ as originally filed/furnished
 - pages* _____ received by this Authority on _____
 - pages* _____ received by this Authority on _____
- the claims:
 - pages _____ as originally filed/furnished
 - pages* _____ as amended (together with any statement) under Article 19
 - pages* _____ received by this Authority on _____
 - pages* _____ received by this Authority on _____
- the drawings:
 - pages _____ as originally filed/furnished
 - pages* _____ received by this Authority on _____
 - pages* _____ received by this Authority on _____
- a sequence listing and/or any related table(s) – see Supplemental Box Relating to Sequence Listing.

3. The amendments have resulted in the cancellation of:

- the description, pages _____
- the claims, Nos. _____
- the drawings, sheets/figs _____
- the sequence listing (*specify*): _____
- any table(s) related to the sequence listing (*specify*): _____

4. This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

- the description, pages _____
- the claims, Nos. _____
- the drawings, sheets/figs _____
- the sequence listing (*specify*): _____
- any table(s) related to the sequence listing (*specify*): _____

* If item 4 applies, some or all of those sheets may be marked "superseded."

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.

PCT/FI 2003/000233

Box No. IV Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees the applicant has:

- restricted the claims.
- paid additional fees.
- paid additional fees under protest.
- neither restricted nor paid additional fees.

2. This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is:

- complied with.
- not complied with for the following reasons:

This International Preliminary Examining Authority found multiple inventions as follows:

I: claims 1-5, 9-10, 14-21 and 25-26 directed to a system, a device and a method for determining levels of power consumption in an electronic device.

II: claims 6-8, 11-13 and 22-24 directed to a system, a device and a method for controlling the power consumption in an electronic device.

From for instance US 5884086 a system and a method are known for supplying power to peripheral devices in a computer system. According to the document, the peripheral device communicates its power requirements to the host system. The power requirements are characterized in for instance 64 different levels (column 7, lines 15-26).

The problem solved by the first invention is an alternative arrangement for determining levels of power required.

The technical feature of invention II is characterized by three different ways of controlling the power consumption:

.../...

4. Consequently, this report has been established in respect of the following parts of the international application:

- all parts.
- the parts relating to claims Nos. _____

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: BOX IV

- II:a -adjusting the frequency of at least one clock signal
- II:b -controlling the bus width
- II:c -controlling the number of storage blocks processed

The problem solved is alternatives in methods of controlling power consumption. The technical features of claims 6-8 and corresponding claims referring to the independent claims, are three different. However, the features could be examined without effort justifying three additional fees and are thus grouped as one additional invention having the special technical feature of controlling the power consumption.

Inventions I and II have in common only the feature of claim 1. However, a person skilled in the art, faced with the problem of determining levels, finds this information in US 5884086.

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.

PCT/FI 2003/000233

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	<u>6-8, 11-13, 22-24</u>	YES
	Claims	<u>1-5, 9-10, 14-21, 25-26</u>	NO
Inventive step (IS)	Claims	_____	YES
	Claims	<u>6-8, 11-13, 22-24</u>	NO
Industrial applicability (IA)	Claims	<u>1-26</u>	YES
	Claims	_____	NO

2. Citations and explanations (Rule 70.7)

Invention I

The single general concept of the invention claimed in claims 1, 9, 16 and 20 is the teaching of determining and setting the power consumption of a peripheral device between two levels.

Reference is made to the following documents cited in the International Search Report:

- D1: US 5884086
- D2: WO 0207494
- D3: US 5758171
- D4: US 6178514

D1 discloses a system and a method for supplying power to peripheral devices in a computer system. According to the document, the peripheral device communicates its power requirements to the host system (column 2, lines 40-44). By communicating the power requirement, the power consumption is determined. The power requirements are characterized in, for instance, 64 different levels (column 7, lines 15-26).

D2 describes a PC card receiver where the power from the battery inside the PC is limited to 600 mA. The problem solved is that the PC card can operate without a battery pack extension (page 2 and figure 4).

D3 discloses a system for controlling and monitoring power to a device. An interface circuit transmits and receives data control signals to and from the device and the host processor (column 4, line 49 ff).

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box V

D4 discloses a method and an apparatus for connecting a device to a bus carrying power and a signal. A device input signal is created that is a function of the level of energy stored in the energy storage device. The current drawn by the device is limited to a predetermined current threshold (column 5, lines 50-56).

The general concept of the invention claimed in claims 1, 9, 16 and 20 is known from each of D1-D4. From, for instance, US 5884086, a system and a method are known for supplying power to peripheral devices in a computer system. According to the document, the peripheral device communicates its power requirements to the host system. The power requirements are characterized in, for instance, 64 different levels. For a person skilled in the art it is obvious that one or more of these values are characterized as maximum values. The statement of maximum values does not involve any unexpected technical effect. Accordingly, the claimed invention is not inventive and does not fulfil the requirement of novelty.

The inventions according to the remaining claims of invention I, claims 2-5, 10, 14-15, 17-19, 21 and 25-26, are matters of fact that are considered obvious for a person skilled in the art or are known from the cited documents. Accordingly, the invention claimed in claims 2-5, 10, 14-15, 17-19, 21 and 25-26 does not fulfil the requirement of novelty, but is industrially applicable.

Invention II

The application does not, *á posteriori*, satisfy the requirement of unity of invention, since the general concept of the independent claims lacks novelty.

The single general concept of invention II is directed to a system, a device and a method for controlling the power consumption in an electronic device. The technical feature of invention II is characterized by the way of controlling the power consumption of the peripheral devices. The problem solved is alternative methods in controlling the power consumption.

Reference is further made to the following documents cited in

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box V

the International Search Report:

D5: US 5737616 describing that the power consumption is controlled by the clock frequency.

D6: GB 2235797 describing that the power consumption is controlled by the clock frequency.

D7: US 5758108 describing that the data bus width and the clock frequency affects the power consumption.

D8: WO9841987 describing that the bus width can be controlled.

D9: US 4841440 describing that the data communication with a peripheral unit is controlled to save power.

Since all cited documents belong to the same technical field, it is considered obvious to a person skilled in the art to combine the information from the documents.

D1 is considered to be closest in describing the invention. The invention according to claims 6-8, 11-13 and 22-24 differs from D1 by stating alternative ways of controlling the powering of a peripheral device. Faced with the problem of finding alternative ways of controlling power, it is considered obvious for a person skilled in the art to select the solutions stated in claims 6-8, for instance, adjusting the frequency of at least one clock signal, controlling the bus width or controlling the number of storage blocks processed and thus arrive at the invention claimed.

Consequently, the invention claimed in claims 6-8, 11-13 and 22-24 does not fulfil the requirement of inventive step, but is industrially applicable.

Electronic Acknowledgement Receipt

EFS ID:	16021418
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Jason Daniel Eisenberg/Saqeef Ahmad
Filer Authorized By:	Jason Daniel Eisenberg
Attorney Docket Number:	3371.002REI0
Receipt Date:	12-JUN-2013
Filing Date:	
Time Stamp:	17:26:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3371002REI0_IDS_package.pdf	1355416 7a7c38794e4feb4f126e47a510cd1ed84583a071	yes	11

Multipart Description/PDF files in .zip description			
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Transmittal Letter	2	8
	Information Disclosure Statement (IDS) Form (SB08)	9	11

Warnings:

Information:

2	Foreign Reference	FP1_GB2235797_A.pdf	1012551 dbd7819ab6f70871d103d94b576a610d87f fd840	no	27
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Warnings:

Information:

3	Foreign Reference	FP2_WO9841987_A1.pdf	2721125 0f5bbe785df943cc2cda0bcb66f5c6b5e247 7201	no	68
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Warnings:

Information:

4	Foreign Reference	FP3_WO0207494_A2.pdf	417522 ad7cf050110fe5e65bda612e8f834e3ae16f a325	no	12
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Warnings:

Information:

5	Non Patent Literature	NPL1_USB_Specification_Revision_2_04272000.pdf	217580 5b1dcc2605b32751dd7c36faf283d7aed24 41fae	no	5
---	-----------------------	--	--	----	---

Warnings:

Information:

6	Non Patent Literature	NPL3_Notice_of_Allowance_mailed_June_13_2007.pdf	517334 8c1d5da8f1a46a34bef35cf9f99b1c1318bb cd44	no	12
---	-----------------------	--	--	----	----

Warnings:

Information:

7	Non Patent Literature	NPL4_Non_Final_Rejection_mailed_September_22_2005.pdf	350911 e0c4a104a3306b9f17f01937eac775cd5f35 ea1c	no	10
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Warnings:

Information:

8	Non Patent Literature	NPL5_Non_Final_Rejection_mailed_July_14_2006.pdf	313489 e17a4431ea51514616a59bc1595cd48a5ba fe008	no	8
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Warnings:

Information:					
9	Non Patent Literature	NPL2_English_Language_Abstr act_for_Japanese_Patent_Publi cation_No_WO9841987_A1_ pdf	185332 c0eac2f778099c6be9852acfaaf437edf3b8b 226	no	1
Warnings:					
Information:					
10	Non Patent Literature	NPL6_Final_Rejection_mailed_ March_23_2006.pdf	391227 09141019e1ded9d65881cae006a1b6eb51 827da4	no	11
Warnings:					
Information:					
11	Non Patent Literature	NPL7_Final_Rejection_mailed_ December_27_2006.pdf	311496 b2bfc1d231f85ce609656bce7166b5c1264 936aa	no	8
Warnings:					
Information:					
12	Non Patent Literature	NPL8_International_Search_Re port.pdf	226701 6f59f5b8dc1e047097cb75cdf75fe2130969 a0f7	no	5
Warnings:					
Information:					
13	Non Patent Literature	NPL9_Patent_Cooperation_Tre aty.pdf	385998 fa0c64971f57a8354d6eb124ac419ef1fbe9 096e	no	7
Warnings:					
Information:					
14	Non Patent Literature	NPL10_ESR_1488306_1124200 6.pdf	253413 346834b21339d729a30c71be78daee9c4ad 243d9	no	6
Warnings:					
Information:					
15	Non Patent Literature	NPL11_ESR_1488306_1220200 7.pdf	197168 20c4c35a64e2aed25b08b31d788afd936be f123a	no	5
Warnings:					
Information:					
16	Non Patent Literature	NPL12_ESR_1488306_0305200 9.pdf	151020 e3cd2fb0ef0b83481571843ef9d2cea1f424 bd7a	no	4
Warnings:					
Information:					
Total Files Size (in bytes):			9008283		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

JASON D. EISENBERG
DIRECTOR
(202) 772-8645
JASONE@SKGF.COM



June 12, 2013

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Art Unit 2184
Attn: Mail Stop Amendment

Re: U.S. Reissue Patent Application
Application No. 13/902,227; Filing Date: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002RE10

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 18 documents (US1-US15 and FP1-FP3);
3. Form PTO/SB/08b (2 sheets) listing 12 documents (NPL1-NPL12); and
4. Copies of cited documents (FP1-FP3 and NPL1-NPL12).

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jason D. Eisenberg #43447/

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/s-a
Enclosure(s)
1699246_1.DOCX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for
Determining the Power
Consumption in Connection with
an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2184

Examiner: To be assigned

Atty. Docket: 3371.002REI0

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
- a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable

inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

- c. The required fee is provided through online credit card payment authorization in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p).
4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of _____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:
- a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable

inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

5. Some documents were cited in search reports by foreign patent offices in counterpart foreign applications. Submission of English language versions of the search report that indicates the degree of relevance found by the foreign office are provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38 and MPEP 609.04(a)(III).
6. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP2** (WO 98/41987 A1) appears to describe a device and method for reproducing digital signal using bus-width memory and device and method for recording digital signal, as noted in the corresponding English-language abstract provided as document **NPL2**.

7. Copies of documents **FP1-FP3** and **NPL1-NPL12** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited as documents **US1-US15** on the attached IDS Forms are submitted.
8. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing

date under 35 U.S.C. § 120. Thus, copies of these documents are not attached.
37 C.F.R. § 1.98(d).

- 9. It is expected that the examiner will review the prosecution and cited art in the parent application no. 10/401,338, filed March 26, 2003, (now U.S. Patent No. 7,278,033) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

- 10. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from U.S. Patent Application No. 10/401,338, filed March 26, 2003 (now U.S. Patent No. 7,278,033) as documents **NPL3-NPL7**.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date:

6/2/13

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

1699303_1.DOCX

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
13/902,227

APPLICATION AS FILED - PART I

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(j))	37 minus 20 = *	17
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 = *	4
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

SMALL ENTITY

RATE(\$)	FEE(\$)
N/A	
N/A	
N/A	
TOTAL	

OR OTHER THAN SMALL ENTITY

RATE(\$)	FEE(\$)
N/A	280
N/A	600
N/A	2160
x 80 =	1360
x 420 =	1680
	0.00
	0.00
TOTAL	6080

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**
Independent (37 CFR 1.16(h))	*	Minus	***	=
Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				

SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

OR OTHER THAN SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**
Independent (37 CFR 1.16(h))	*	Minus	***	=
Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				

SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

OR OTHER THAN SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.



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Table with 7 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY. DOCKET NO, TOT CLAIMS, IND CLAIMS. Row 1: 13/902,227, 05/24/2013, 2115, 6080, 3371.002RE10, 37, 7

CONFIRMATION NO. 8765

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



Date Mailed: 09/27/2013

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections

Inventor(s)

Kimmo MYLLY, Julkujarvi, FINLAND;

Applicant(s)

Memory Technologies LLC, Las Vegas, NV

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a REI of 10/401,338 03/26/2003 PAT 7278033

Foreign Applications (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.)

FINLAND 20020594 03/27/2002 No Access Code Provided

Permission to Access - A proper Authorization to Permit Access to Application by Participating Offices (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 09/26/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 13/902,227

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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1 of 1 DOCUMENT

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

7278033

[Link to Claims Section](#)

October 2, 2007

Method and a system for determining the power consumption in connection with an electronic device, and an electronic device

REISSUE:

May 24, 2013 - Reissue Application filed, Ex. Gp.: 2115; Re. S.N. 13/902,227 , (O.G. October 22, 2013)

INVENTOR: Mylly, Kimmo - Tampere, Republic of Finland (FI), Republic of Finland ()

APPL-NO: 401338 (10)

FILED-DATE: March 26, 2003

GRANTED-DATE: October 2, 2007

ASSIGNEE-PRE-ISSUE:

March 26, 2003 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., NOKIA CORPORATION KEILALAHDENTIE 4 EPSOO FIN-02150, Reel and Frame Number: 013928/0450

ASSIGNEE-AT-ISSUE:

Nokia Corporation, Espoo, Republic of Finland (FI), Foreign company or corporation (03)

ASSIGNEE-AFTER-ISSUE:

April 10, 2013 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., MEMORY TECHNOLOGIES LLC, 6787 W. TROPICANA AVE., SUITE 238, LAS VEGAS, NEVADA, UNITED STATES OF AMERICA (US), 89103, Reel and Frame Number: 030190/0043

April 10, 2013 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., NOKIA INC., 200 S. MATHILDA AVENUE, SUNNYVALE, CALIFORNIA, UNITED STATES OF AMERICA (US), 94086, Reel and Frame Number: 030189/0381

LEGAL-STATUS:

March 26, 2003 - ASSIGNMENT

March 2, 2011 - FEE PAYMENT

April 10, 2013 - ASSIGNMENT

April 10, 2013 - ASSIGNMENT

October 22, 2013 - REISSUE APPLICATION FILED

March 2, 2011 - Payment of Maintenance Fee, 4th Year, Large Entity.
May 29, 2013 - Payor Number Assigned.

ENGLISH-ABST:

The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Signaling between the electronic device and the peripheral device sets a maximum value for the power consumption of the peripheral device which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied.

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1 of 3 DOCUMENTS

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US Fed News

October 4, 2007 Thursday 4:57 AM EST

LENGTH: 233 words

HEADLINE: Finish Inventor Develops Power Consumption Determination Method

BYLINE: US Fed News

DATELINE: Alexandria, Va.

BODY:

ALEXANDRIA, Va., Oct. 4 -- Kimmo Mylly of Tampere, Finland, has developed a method for determining power consumption.

According to the U.S. Patent & Trademark Office: "The present invention relates to a method and a system for determining the power consumption in an electronic device, to which a peripheral device is connected, to which the power is supplied from the electronic device. At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Signaling between the electronic device and the peripheral device sets a maximum value for the power consumption of the peripheral device which is between said first and second maximum values. The invention also relates to an electronic device and a peripheral device, in which the method is applied."

The inventor was issued U.S. Patent No. 7,278,033 on Oct. 2.

The patent has been assigned to Nokia Corp., Espoo, Finland.

The original application was filed on March 26, 2003, and is available at:
<http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm>

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LOAD-DATE: October 4, 2007

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Patent Search 7278033 1/7/2014

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(Charges for search still apply)

Search Strategy

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07/01/14

Number of documents: 1

FI20020594

A METHOD AND A SYSTEM FOR DETERMINING THE POWER
CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND
AN ELECTRONIC DEVICE
MEMORY TECHNOLOGIES; NOKIA

A METHOD AND A SYSTEM FOR DETERMINING THE POWER CONSUMPTION IN CONNECTION WITH AN ELECTRONIC DEVICE, AND AN ELECTRONIC DEVICE

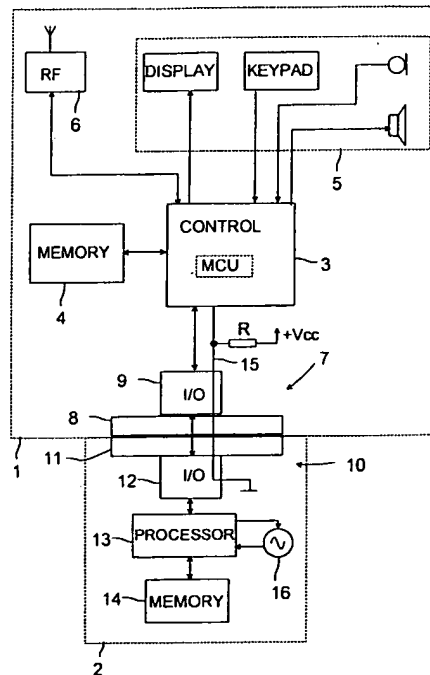
FI20020594

<ul style="list-style-type: none"> Patent Assignee MEMORY TECHNOLOGIES NOKIA Inventor MYLLY-KIMMO International Patent Classification G01R; G01R-031/00; G06F-001/00; G06F-001/04; G06F-001/26; G06F-001/28; G06F-001/32 US Patent Classification 713300000; 713320000; 713322000 ECLA Code G06F-001/26P; G06F-001/28 	<ul style="list-style-type: none"> Publication Information FI20020594 A0 20020327 [FI20020594] Priority Details 2002FI-0000594 20020327 2003WO-FI00233 20030326 																																												
<ul style="list-style-type: none"> Fampat family <table border="0" style="width: 100%;"> <tr> <td style="width: 33%;">FI20020594</td> <td style="width: 33%;">A0</td> <td style="width: 33%;">20020327</td> <td style="width: 33%;">[FI20020594]</td> </tr> <tr> <td>FI20020594</td> <td>A</td> <td>20030928</td> <td>[FI200200594]</td> </tr> <tr> <td>WO03081407</td> <td>A1</td> <td>20031002</td> <td>[WO200381407]</td> </tr> <tr> <td>US2003188205</td> <td>A1</td> <td>20031002</td> <td>[US20030188205]</td> </tr> <tr> <td>AU2003212408</td> <td>A1</td> <td>20031008</td> <td>[AU2003212408]</td> </tr> <tr> <td>KR20040097207</td> <td>A</td> <td>20041117</td> <td>[KR20040097207]</td> </tr> <tr> <td>EP1488306</td> <td>A1</td> <td>20041222</td> <td>[EP1488306]</td> </tr> <tr> <td>FI115562</td> <td>B</td> <td>20050531</td> <td>[FI-115562]</td> </tr> <tr> <td>JP2005521152</td> <td>A</td> <td>20050714</td> <td>[JP2005521152]</td> </tr> <tr> <td>CN1643478</td> <td>A</td> <td>20050720</td> <td>[CN1643478]</td> </tr> <tr> <td>US7278033</td> <td>B2</td> <td>20071002</td> <td>[US7278033]</td> </tr> </table> 		FI20020594	A0	20020327	[FI20020594]	FI20020594	A	20030928	[FI200200594]	WO03081407	A1	20031002	[WO200381407]	US2003188205	A1	20031002	[US20030188205]	AU2003212408	A1	20031008	[AU2003212408]	KR20040097207	A	20041117	[KR20040097207]	EP1488306	A1	20041222	[EP1488306]	FI115562	B	20050531	[FI-115562]	JP2005521152	A	20050714	[JP2005521152]	CN1643478	A	20050720	[CN1643478]	US7278033	B2	20071002	[US7278033]
FI20020594	A0	20020327	[FI20020594]																																										
FI20020594	A	20030928	[FI200200594]																																										
WO03081407	A1	20031002	[WO200381407]																																										
US2003188205	A1	20031002	[US20030188205]																																										
AU2003212408	A1	20031008	[AU2003212408]																																										
KR20040097207	A	20041117	[KR20040097207]																																										
EP1488306	A1	20041222	[EP1488306]																																										
FI115562	B	20050531	[FI-115562]																																										
JP2005521152	A	20050714	[JP2005521152]																																										
CN1643478	A	20050720	[CN1643478]																																										
US7278033	B2	20071002	[US7278033]																																										

Abstract:

(CN1643478)

The present invention relates to a method and a system for determining the power consumption in an electronic device (1), to which a peripheral device (2) is connected, to which the power is supplied from the electronic device (1). At least a first maximum value and a second maximum value, higher than the first maximum value, are determined for the power consumption. Between the electronic device (1) and the peripheral device (2), a maximum for the power consumption of the peripheral device (2) is set to a value which is substantially between said first and second maximum values. The invention also relates to an electronic device (1) and a peripheral device (2), in which the method is applied.



Action Taken

(EP1488306)

LEGAL DETAILS FOR EP1488306

Actual or expected expiration date=2010-01-06
Legal state=DEAD
Status=LAPSED

Event publication date=2003-03-26
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=EP EP03708304
Application date=2003-03-26
Standardized application number=2003EP-0708304

Event publication date=2004-12-22
Event code=Request for examination filed
Event indicator=Pos
Event type=Examination events

Request for examination filed

Pruefungsantrag gestellt

Effective date of the event=2004-09-29

Event publication date=2004-12-22
Event code=Application published with search report
Event indicator=Pos
Event type=Examination events

Application published with search report

Publication country=EP
Publication number=EP1488306
Publication stage Code=A1
Publication date=2004-12-22
Standardized publication number=EP1488306

Event publication date=2004-12-22
Event code=Designated contracting states:
Event indicator=Pos
Event type=Designated states

Designated contracting states:

Benannte vertragsstaaten

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

Event publication date=2004-12-22
Event code=Extension of the european patent to
Event indicator=Pos
Event type=Designated states

Extension of the european patent to

Erstreckung des europaeischen patents auf

Countries: AL LT LV MK

Event publication date=2006-12-27
Event code=First examination report
Event indicator=Pos
Event type=Examination events

First examination report

Erster pruefungsbescheid

Effective date of the event=2006-11-24

Event publication date=2010-01-06
Event code=Deemed to be withdrawn
Event indicator=Neg
Event type=Event indicating Not In Force

Deemed to be withdrawn

Als zurueckgenommen gelten

Effective date of the event=2009-07-16

Action Taken

(WO200381407)

LEGAL DETAILS FOR WO03081407

Actual or expected expiration date=2013-12-22
Legal state=DEAD
Status=LAPSED

Event publication date=2003-03-26
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=WO WOFI0300233
Application date=2003-03-26
Standardized application number=2003WO-FI00233

Event publication date=2003-10-02
Event code=Published application with search report
Event indicator=Pos
Event type=Examination events

Published application with search report

Publication country=WO
Publication number=WO03081407
Publication stage Code=A1
Publication date=2003-10-02
Standardized publication number=WO200381407

Event publication date=2003-10-02
Event code=Designated states

Event indicator=Pos
Event type=Designated states

Designated states

AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR
HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC
SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Event publication date=2003-10-02
Event code=Designated countries for regional patents
Event indicator=Pos
Event type=Designated states

Designated countries for regional patents

GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW AM AZ BY KG KZ MD RU TJ TM AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HU IE IT LU MC NL PT RO SE SI SK TR BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

Event publication date=2003-11-13
Event code=Request for preliminary examination filed prior to expiration of 19th month from priority date (pct application filed
before 20040101)
Event type=Examination events

Request for preliminary examination filed prior to expiration of 19th month from priority date (pct application filed before 20040101)

LEGAL DETAILS FOR DESIGNATED STATE AU2003212408

Actual or expected expiration date=2004-12-16
Legal state=DEAD
Status=LAPSED

Corresponding cc :
Designated or member state=AU Corresponding appl: AU2003212408
Application date in the designated or member state=2003-03-26
Application number in the designated or member state=2003AU-0212408

Corresponding cc :
Designated or member state=AU Corresponding pat: AU2003212408
Publication stage code in the designated or member state=A1
Publication date in the designated or member state=2003-10-08
Publication number in the designated or member state=AU2003212408

Event publication date=2013-12-26
Event code=Patent status changed by the national office

Patent status changed by the national office

LEGAL DETAILS FOR DESIGNATED STATE CN1643478

Actual or expected expiration date=2010-02-24
Legal state=DEAD
Status=LAPSED

Corresponding cc :
Designated or member state=CN Corresponding appl: CN03807010
Application date in the designated or member state=2003-03-26
Application number in the designated or member state=2003CN-0807010

Corresponding cc :
Designated or member state=CN Corresponding pat: CN1643478

Publication stage code in the designated or member state=A
Publication date in the designated or member state=2005-07-20
Publication number in the designated or member state=CN1643478

Event publication date=2004-09-27
Event code=Wipo information: entry into national phase
Event indicator=Pos
Event type=Entry into national phase

Wipo information: entry into national phase

Corresponding cc:Designated or member state=CN

Event publication date=2013-12-26
Event code=Patent status changed by the national office

Patent status changed by the national office

LEGAL DETAILS FOR DESIGNATED STATE EP1488306

Actual or expected expiration date=2010-01-06
Legal state=DEAD
Status=LAPSED

Corresponding cc :
Designated or member state=EP Corresponding appl: EP03708304
Application date in the designated or member state=2003-03-26
Application number in the designated or member state=2003EP-0708304

Corresponding cc :
Designated or member state=EP Corresponding pat: EP1488306
Publication stage code in the designated or member state=A1
Publication date in the designated or member state=2004-12-22
Publication number in the designated or member state=EP1488306

Event publication date=2003-11-26
Event code=EP: The EPO has been informed by wipo that ep was designated in this application
Event type=Designated states

EP: The EPO has been informed by wipo that ep was designated in this application

Corresponding cc:Designated or member state=EP

Event publication date=2004-09-27
Event code=Wipo information: entry into national phase
Event indicator=Pos
Event type=Entry into national phase

Wipo information: entry into national phase

Corresponding cc:Designated or member state=EP

Event publication date=2004-12-22
Event code=Wipo information: published in national office
Event indicator=Pos
Event type=Examination events

Wipo information: published in national office

Corresponding cc:Designated or member state=EP

Event publication date=2013-12-26
Event code=Patent status changed by the national office

Patent status changed by the national office

LEGAL DETAILS FOR DESIGNATED STATE JP2005521152

Actual or expected expiration date=2009-07-08
Legal state=DEAD
Status=REVOKED

Corresponding cc :
Designated or member state=JP Corresponding appl: JP2003579071
Application date in the designated or member state=2003-03-26
Application number in the designated or member state=2003JP-0579071

Corresponding cc :
Designated or member state=JP Corresponding pat: JP2005521152
Publication stage code in the designated or member state=A
Publication date in the designated or member state=2005-07-14
Publication number in the designated or member state=JP2005521152

Event publication date=2004-09-27
Event code=Wipo information: entry into national phase
Event indicator=Pos
Event type=Entry into national phase

Wipo information: entry into national phase

Corresponding cc:Designated or member state=JP

Event publication date=2013-12-26
Event code=Patent status changed by the national office

Patent status changed by the national office

LEGAL DETAILS FOR DESIGNATED STATE KR

Actual or expected expiration date=2012-11-17
Legal state=DEAD
Status=LAPSED

Corresponding cc :
Designated or member state=KR Corresponding appl: KR1020047015016
Application date in the designated or member state=2003-03-26

Event publication date=2004-09-22
Event code=Wipo information: entry into national phase
Event indicator=Pos
Event type=Entry into national phase

Wipo information: entry into national phase

Corresponding cc:Designated or member state=KR

Event publication date=2004-11-17
Event code=Wipo information: published in national office
Event indicator=Pos

Event type=Examination events

Wipo information: published in national office

Corresponding cc:Designated or member state=KR

Event publication date=2012-11-17

Event code=Pending application likely abandoned

Event indicator=Neg

Event type=Event indicating Not In Force

Pending application likely abandoned

LEGAL DETAILS FOR DESIGNATED STATE PH

Actual or expected expiration date=2009-02-09

Legal state=DEAD

Status=LAPSED

Corresponding cc :

Designated or member state=PH Corresponding appl: PH1-2004-501356

Application date in the designated or member state=2003-03-26

Event publication date=2004-02-09

Event code=Wipo information: entry into national phase

Event indicator=Pos

Event type=Entry into national phase

Wipo information: entry into national phase

Corresponding cc:Designated or member state=PH

Event publication date=2009-02-09

Event code=Pending application likely abandoned

Event indicator=Neg

Event type=Event indicating Not In Force

Pending application likely abandoned

Action Taken

(US20030188205)

LEGAL DETAILS FOR US2003188205

Actual or expected expiration date=2024-07-10

Legal state=ALIVE

Status=GRANTED

Event publication date=2003-03-26

Event code=Application details

Event indicator=Pos

Event type=Examination events

Application details

Application country=US US10401338

Application date=2003-03-26

Standardized application number=2003US-10401338

Event publication date=2003-03-26

Event code=Assignment

Event type=Change of name or address
Event type=Reassignment

Assignment

OWNER:NOKIA CORPORATION, FINLAND
Effective date of the event=2003-01-16

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:MYLLY, KIMMO REEL/FRAME:013928/0450.

Event publication date=2003-10-02
Event code=Application published
Event indicator=Pos
Event type=Examination events

Application published

Publication country=US
Publication number=US2003188205
Publication stage Code=A1
Publication date=2003-10-02
Standardized publication number=US20030188205

Event publication date=2007-10-02
Event code=From pub/pn
Event indicator=Pos
Event type=Event indicating In Force

Granted patent as second publication

Publication country=US
Publication number=US7278033
Publication stage Code=B2
Publication date=2007-10-02
Standardized publication number=US7278033

Event publication date=2011-03-02
Event code=Fee payment
Event indicator=Pos
Event type=Event indicating In Force
Event type=Payment or non-payment notifications

Fee payment

Year of payment of annual fees=4

Event publication date=2013-04-10
Event code=Assignment
Event type=Change of name or address
Event type=Reassignment

Assignment

OWNER:NOKIA INC., CALIFORNIA
Effective date of the event=2013-03-24

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:NOKIA CORPORATION REEL/FRAME:030189/0381.

Event publication date=2013-04-10
Event code=Assignment
Event type=Change of name or address

Event type=Reassignment

Assignment

OWNER:MEMORY TECHNOLOGIES LLC, NEVADA

Effective date of the event=2013-03-25

ASSIGNMENT OF ASSIGNORS INTEREST ASSIGNOR:NOKIA INC. REEL/FRAME:030190/0043.

Event publication date=2013-10-22

Event code=Reissue application filed

Event type=Opposition and reexamination events

Reissue application filed

Reissue appl. filed

Effective date of the event=2013-05-24

Event publication date=2007-10-02

Event code=Patent term extension under 35 U.S.C 154(b) until/for

Event indicator=Pos

Event type=Event indicating In Force

Event type=Extension of term of duration of protection

Patent term extension under 35 U.S.C 154(b) until/for:

Number of days of extension=472

Action Taken

(JP2005521152)

LEGAL DETAILS FOR JP2005521152

Actual or expected expiration date=2009-07-08

Legal state=DEAD

Status=REVOKED

Event publication date=2003-03-26

Event code=Application details

Event indicator=Pos

Event type=Examination events

Application details

Application country=JP JP2003579071

Application date=2003-03-26

Standardized application number=2003JP-0579071

Event publication date=2005-07-14

Event code=Published application

Event indicator=Pos

Event type=Examination events

Published application

Publication country=JP

Publication number=JP2005521152

Publication stage Code=A

Publication date=2005-07-14

Standardized publication number=JP2005521152

Event publication date=2006-03-16

Event code=Written amendment
Event type=Restitution or restoration

Written amendment

Effective date of the event=2006-03-15

JAPANESE INTERMEDIATE CODE: A523.

Event publication date=2006-03-16
Event code=Written request for application examination
Event indicator=Pos
Event type=Examination events

Written request for application examination

Effective date of the event=2006-03-15

JAPANESE INTERMEDIATE CODE: A621.

Event publication date=2008-10-01
Event code=Notification of reasons for refusal
Event indicator=Neg
Event type=Examination events

Notification of reasons for refusal

Effective date of the event=2008-09-30

JAPANESE INTERMEDIATE CODE: A131.

Event publication date=2008-12-26
Event code=Written amendment
Event type=Restitution or restoration

Written amendment

Effective date of the event=2008-12-25

JAPANESE INTERMEDIATE CODE: A523.

Event publication date=2009-07-08
Event code=Decision of refusal
Event indicator=Neg
Event type=Event indicating Not In Force

Decision of refusal

Effective date of the event=2009-07-07

JAPANESE INTERMEDIATE CODE: A02.

Action Taken

(FI200200594)

LEGAL DETAILS FOR FI20020594

Actual or expected expiration date=2022-03-27
Legal state=ALIVE
Status=GRANTED

Event publication date=2002-03-27

Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=FI FI20020594
Application date=2002-03-27
Standardized application number=2002FI-0000594

Event publication date=2002-03-27
Event code=FI/A0
Event indicator=Pos
Event type=Examination events

Unex. applic. open to publ. inspec.

Publication country=FI
Publication number=FI20020594
Publication stage Code=A0
Publication date=2002-03-27
Standardized publication number=FI20020594

Event publication date=2003-09-28
Event code=FI/A
Event indicator=Pos
Event type=Examination events

Unex. applic. open to publ. inspec.

Publication country=FI
Publication number=FI20020594
Publication stage Code=A
Publication date=2003-09-28
Standardized publication number=FI200200594

Event publication date=2005-05-31
Event code=Examined application
Event indicator=Pos
Event type=Examination events

Examined application

Publication country=FI
Publication number=FI115562
Publication stage Code=B
Publication date=2005-05-31
Standardized publication number=FI-115562

Action Taken

(AU2003212408)

LEGAL DETAILS FOR AU2003212408

Actual or expected expiration date=2004-12-16
Legal state=DEAD
Status=LAPSED

Event publication date=2003-03-26
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=AU AU2003212408
Application date=2003-03-26
Standardized application number=2003AU-0212408

Event publication date=2003-10-08
Event code=Open to public inspection
Event indicator=Pos
Event type=Examination events

Open to public inspection

Publication country=AU
Publication number=AU2003212408
Publication stage Code=A1
Publication date=2003-10-08
Standardized publication number=AU2003212408

Event publication date=2004-12-16
Event code=Application lapsed section 142(2)(f)/reg. 8.3(3) - pct applic. not entering national phase
Event indicator=Neg
Event type=Event indicating Not In Force

Application lapsed section 142(2)(f)/reg. 8.3(3) - pct applic. not entering national phase

Action Taken

(KR20040097207)

LEGAL DETAILS FOR KR20040097207

Actual or expected expiration date=2012-11-17
Legal state=DEAD
Status=LAPSED

Event publication date=2003-03-26
Event code=Application details
Event indicator=Pos
Event type=Examination events

Application details

Application country=KR KR20047015016
Application date=2003-03-26
Standardized application number=2004KR-7015016

Event publication date=2004-11-17
Event code=Published application
Event indicator=Pos
Event type=Examination events

Published application

Publication country=KR
Publication number=KR20040097207
Publication stage Code=A
Publication date=2004-11-17
Standardized publication number=KR20040097207

Event publication date=2012-11-17
Event code=Pending application likely abandoned
Event indicator=Neg

Event type=Event indicating Not In Force

Pending application likely abandoned

Action Taken

(CN1643478)

LEGAL DETAILS FOR CN1643478

Actual or expected expiration date=2010-02-24

Legal state=DEAD

Status=LAPSED

Event publication date=2003-03-26

Event code=Application details

Event indicator=Pos

Event type=Examination events

Application details

Application country=CN CN03807010

Application date=2003-03-26

Standardized application number=2003CN-0807010

Event publication date=2005-07-20

Event code=Published application

Event indicator=Pos

Event type=Examination events

Published application

Publication country=CN

Publication number=CN1643478

Publication stage Code=A

Publication date=2005-07-20

Standardized publication number=CN1643478

Event publication date=2005-07-20

Event code=Publication

Event indicator=Pos

Event type=Event indicating In Force

Publication

Event publication date=2005-09-14

Event code=Request of examination as to substance

Event type=Examination events

Request of examination as to substance

Event publication date=2010-02-24

Event code=Deemed withdrawal of patent application after publication (patent law 2001)

Event indicator=Neg

Event type=Event indicating Not In Force

Deemed withdrawal of patent application after publication (patent law 2001)

Deemed withdrawal of patent application after publication

(12) **EUROPÄISCHE PATENTANMELDUNG**

(43) Veröffentlichungstag: 16.07.2001 Patentblatt 2001/29 (51) Int. Cl.?: G06F 1/26

(21) Anmeldenummer: 00128577.4

(22) Anmeldetag: 27.12.2000

(84) Benannte Vertragsstaaten:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR
Benannte Erstreckungsstaaten:
AL LT LV MK RO SI

(71) Anmelder: Wincor Nixdorf GmbH & Co KG
32106 Paderborn (DE)

(72) Erfinder: Hoffmann, Stefan
12163 Berlin (DE)

(30) Priorität: 29.12.1999 DE 19963675

(74) Vertreter: Schaumburg, Thoenes & Thurn
Postfach 86 07 48
81634 München (DE)

(54) **Automatisches Erhöhen der Betriebsspannung bei Peripheriegeräten**

(57) Die Erfindung betrifft eine Einrichtung (10) zum Betreiben eines elektrischen Gerätes, die eine Anschlußeinheit (14) hat, die mindestens ein elektrisches Gerät (50, 52, 54, 56) mit elektrischer Leistung versorgt, wobei die Versorgung in einer Initialisierungsphase des elektrischen Gerätes (50, 52, 54, 56) mit einer vorbe-

stimmten ersten Spannung erfolgt. Das elektrische Gerät (50, 52, 54, 56) moduliert den Versorgungsstrom (80) abhängig von der benötigten Nennbetriebsspannung. Eine Steuerung (62) wertet den modulierten Versorgungsstrom (80) aus und stellt für die Betriebsphase die Nennbetriebsspannung in der Anschlußeinheit (14) ein.

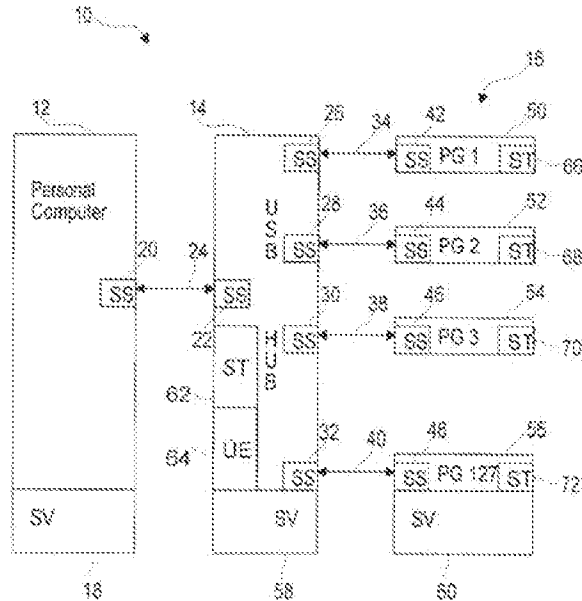


Fig. 1

EP 1 117 026 A2

Beschreibung

[0001] Die Erfindung betrifft eine Einrichtung zum Betreiben eines elektrischen Gerätes, die eine Anschlußeinheit hat, durch die mindestens ein elektrisches Gerät mit elektrischer Leistung versorgt wird.

[0002] Anschlußeinheiten, die eine Versorgungsspannung liefern und über die Daten übertragen werden, sind in Personalcomputern, Macintosh Computern, Industriecomputern und in anderen Computern sowie in Steuereinheiten angeordnet. Anschlußeinheiten in Personalcomputern arbeiten beispielsweise nach der 1985 von der Firma Intel entwickelten USB-Schnittstellenvorgabe (Universal Serial Bus). Macintosh Computer arbeiten seit den 80er Jahren gemäß einer Apple-Desktop-Bus-Schnittstellenvorgabe. Bei Industriecomputern wird als Schnittstellenvorgabe der IEEE-1394-Standard verwendet, der auch unter dem Namen "Fire Wire" bekannt ist. Die genannten Schnittstellenvorgaben gewährleisten, daß anzuschließende Geräte auch während des Betriebs der Schnittstelle angeschlossen werden können. Solche anzuschließenden Geräte werden auch als Peripheriegeräte bezeichnet. Außerdem sind die Anschlußvorrichtungen für eine Vielzahl von Peripheriegeräten einheitlich, z.B. für Computer-Maus, Tastatur, Drucker, Kamera usw. Die Versorgung der Peripheriegeräte mit elektrischer Leistung erfolgt durch eine Stromversorgungseinheit in der Anschlußeinheit.

[0003] Die Stromversorgungseinheit ist gemäß Schnittstellenvorgabe für eine maximale Leistung ausgelegt, die für die angeschlossenen Peripheriegeräte nicht überschritten werden darf. Man unterscheidet Peripheriegeräte geringer Leistung, die beispielsweise bei einer Spannung von 5 V einen Stromfluß von 100 mA hervorrufen, und Peripheriegeräte höherer Leistung, die beispielsweise bei 5 V einen Stromfluß von bis zu 500 mA hervorrufen. Eine große Menge von anzuschließenden Geräten kann mit der gemäß der Schnittstellenvorgabe maximal zulässigen Versorgungsleistung betrieben werden. Bei den genannten Schnittstellenvorgaben handelt es sich nicht um Vorgaben für ein Busesystem, bei dem mehrere Geräte auf die gleichen Leitungen zugreifen. In einigen der genannten Schnittstellenvorgaben wird zwar die Bezeichnung "Bus" verwendet, tatsächlich handelt es sich bei den Schnittstellenvorgaben aber um sternförmig ausgelegte Schnittstellen. Peripheriegeräte eines noch höheren dritten Leistungsbereichs können nicht an den genannten Schnittstellen betrieben werden. Sie benötigen eine zusätzliche separate Stromversorgungseinheit.

[0004] Aufgabe der Erfindung ist es, eine Einrichtung anzugeben, die den Betrieb von elektrischen Geräten mit erhöhter Leistung über eine Anschlußeinheit ermöglicht.

[0005] Diese Aufgabe wird für eine Einrichtung zum Betreiben von elektrischen Geräten durch die Merkmale des Anspruchs 1 gelöst. Vorteilhafte Weiterentwicklungen werden in den abhängigen Ansprüchen angege-

ben.

[0006] Die Einrichtung zum Betreiben von elektrischen Geräten hat eine Anschlußeinheit, die mindestens ein elektrisches Gerät mit elektrischer Leistung versorgt, wobei die Versorgung in einer Initialisierungsphase des elektrischen Gerätes mit einer vorbestimmten ersten Spannung erfolgt. Das elektrische Gerät moduliert den Versorgungsstrom abhängig von der benötigten Nennbetriebsspannung. Eine Steuerung wertet den modulierten Versorgungsstrom aus. Abhängig vom Informationsgehalt der Modulation wird für die Betriebsphase die Nennbetriebsspannung in der Anschlußeinheit eingestellt.

[0007] Durch die Erfindung ist es möglich, Peripheriegeräte, für die die Schnittstellenanschlußleistung nicht ausreichend ist, an einer solchen Schnittstelle zu betreiben. Solche Geräte enthalten beispielsweise LCD's (Liquid Cristal Display) mit Hintergrundbeleuchtung, wie sie an Registrierkassen in Verkaufsstellen eingesetzt werden. Das angeschlossene Gerät teilt der Anschlußeinheit die benötigte Nennspannung mit. Die durch das Gerät benötigte Leistung wird durch die Wahl einer höheren weiteren Versorgungsspannung bei gleichzeitigem Unterschreiten des maximal zulässigen Versorgungsstroms durch die Anschlußeinheit bereitgestellt. Einzelne Abschnitte der Schnittstelle werden somit bei einer sternförmig ausgelegten Schnittstellenstruktur mit der höheren Spannung versorgt.

[0008] Vorteilhaft ist es, als höhere weitere Versorgungsspannung eine Schutzkleinspannung zu nutzen, insbesondere eine Gleichspannung im Bereich von 5 V und 60 V, da somit gefährliche Körperströme bei Personen beim Berühren spannungsführender Teile vermieden sind. Bei Sicherheitskleinspannungen größer als 60 V Gleichspannung oder 25 V Wechselspannung ist eine Isolation spannungsführender Teile erforderlich. Steckverbinder von Schnittstellen sind im allgemeinen genormt und somit fest vorgegeben. Bei einer Spannungserhöhung muß sichergestellt sein, daß diese Steckverbinder und weitere spannungsführende Elemente eine ausreichende Spannungsfestigkeit haben.

[0009] In einer Weiterentwicklung enthält die Anschlußeinheit auch eine mit der Steuereinrichtung verbundene Überwachungseinrichtung zum Überwachen der Verbindung zum angeschlossenen Gerät. Der durch das angeschlossene Gerät verursachte Stromfluß wird somit überwacht. Unterschreitet der Stromfluß einen bestimmten Wert, so ist dies ein Zeichen dafür, daß das Gerät von der Anschlußeinheit getrennt worden ist. In diesem Fall wird die Versorgungsspannung der Schnittstelle wieder auf den normalen Wert gesenkt, um eine Zerstörung eines später angeschlossenen anderen Gerätes zu vermeiden, das eine geringere Versorgungsspannung benötigt. Die in der Anschlußeinheit integrierte Stromüberwachung kann auch zum Überwachen des modulierten Versorgungsstroms genutzt werden.

[0010] Weitere Merkmale und Vorteile der Erfindung ergeben sich aus der folgenden Beschreibung, welche

in Verbindung mit den beigelegten Zeichnungen die Erfindung anhand eines Ausführungsbeispiels erläutert.

[0011] Es zeigen:

Figur 1 ein Blockschaltbild einer Einrichtung zum Betreiben von elektrischen Geräten mit einer Anschlußeinheit, an der Peripheriegerä- te angeschlossen sind, und

Figur 2 ein Strom-Zeit Diagramm, in dem eine durch Über- bzw. Unterschreiten eines Grenzwertes generierte Bitfolge dargestellt ist.

[0012] In Figur 1 ist ein Blockschaltbild einer Einrichtung 10 zum Betreiben von elektrischen Geräten mit einer Anschlußeinheit 14, an der Peripheriegeräte 50, 52, 54, 56 angeschlossen sind, dargestellt. Die Einrichtung 10 hat einen Personalcomputer 12, eine Anschlußeinheit 14 und mehrere Peripheriegeräte 16. In dem Personalcomputer 12 ist eine Stromversorgungseinheit 18 und ein Schnittstellenanschluß 20 angeordnet. Dieser Schnittstellenanschluß 20 arbeitet nach der USB-Schnittstellenvorgabe. USB steht dabei für Universal Serial Bus. Der Personalcomputer 12 steuert die USB-Schnittstelle 22. Die Anschlußeinheit 14 hat einen Schnittstellenanschluß 22, der über eine Verbindungsleitung 24 mit dem Schnittstellenanschluß 20 des Personalcomputers 12 verbunden ist, und je einen Schnittstellenanschluß 26, 28, 30, 32, die über je eine Verbindungsleitung 34, 36, 38, 40 mit den Peripheriegeräten 42, 44, 46, 48 verbunden sind. Bei der USB-Schnittstellenvorgabe sind bis zu 127 Peripheriegeräte anschließbar. An der Anschlußeinheit 14 sind vier Peripheriegeräte 50, 52, 54, 56 angeschlossen. In anderen Ausführungsformen sind an einer solchen Anschlußeinheit üblicherweise zwei bis zehn Schnittstellenanschlüsse für Peripheriegeräte vorhanden. Im Bedarfsfall können auch weitere Anschlußeinheiten an den Schnittstellenanschlüssen angeschlossen werden, wobei an diese weitere Peripheriegeräte anschließbar sind. Solche Anschlußeinheiten werden auch als HUB bezeichnet. Die Anschlußeinheit 14 hat eine eigene Stromversorgungseinheit 58, die mehrere Versorgungsspannungen bereitstellt. Dadurch können die Peripheriegeräte 50, 52, 54, 56 mit verschiedenen Spannungen versorgt werden. Eine solche Anschlußeinheit 14 mit einer Stromversorgungseinheit 58 zum versorgen der Peripheriegeräte 50, 52, 54, 56 wird auch als Self-powered HUB bezeichnet.

[0013] Weiterhin ist in der Anschlußeinheit 14 eine Überwachungseinheit 64 integriert, die unter anderem die Stromaufnahme eines jeden Peripheriegerätes 50, 52, 54, 56 überwacht. Beim Überschreiten der maximal zulässigen Ströme werden Fehlermeldungen generiert. Die Überwachungseinheit erfaßt auch das Unterschreiten eines minimalen Stromwerts, z.B. wenn das Peripheriegerät 50, 52, 54, 56 von der Anschlußeinheit 14 getrennt ist.

[0014] Wird nun ein Peripheriegerät 50, 52, 54, 56 an die Anschlußeinheit 14 angeschlossen, erfolgt ein Anmeldevorgang durch eine Steuerung 76, 78, 80, 82 des Peripheriegerätes 50, 52, 54, 56 am USB-Bus. Dieser Anmeldevorgang wird auch als Enumerationsprozeß bezeichnet. Dabei wird das Peripheriegerät 50, 52, 54, 56 im Personalcomputer 12 als angeschlossen und nutzbar registriert. Die zum Betreiben des Peripheriegerätes 50, 52, 54, 56 im Personalcomputer 12 notwendigen Programmmodule werden geladen und aktiviert. Während des Anmeldevorgangs nimmt das Peripheriegerät 50, 52, 54, 56 einen Strom kleiner 100 mA auf, unabhängig davon, ob es zum späteren Betrieb mehr Leistung benötigt, und verhält sich somit als Peripheriegerät 50, 52, 54, 56 mit geringem Leistungsbedarf, als sogenanntes Low Power Peripheriegerät. Baugruppen mit hohem Leistungsbedarf sind zu diesem Zeitpunkt im Peripheriegerät 50, 52, 54, 56 abgeschaltet. Nach dem Anmeldevorgang schaltet das Peripheriegerät 50, 52, 54, 56 im Falle eines Peripheriegerätes 50, 52, 54, 56 mit hohem Leistungsbedarf, einem sogenannten High Power Peripheriegerät, die Baugruppen mit hohem Leistungsbedarf zu. Das Peripheriegerät 50, 52, 54, 56 ist betriebsbereit. An den USB-Bus können nach der USB-Bus Spezifikation nur Peripheriegeräte 50, 52, 54, 56 mit einer maximalen Stromaufnahme von 500 mA angeschlossen werden. Dies ist nicht zuletzt durch die maximale Strombelastbarkeit der Steckverbinder bedingt. Um dennoch Peripheriegeräte 50, 52, 54, 56 mit einem höherem Leistungsbedarf an der USB-Schnittstelle 26, 28, 30, 32 betreiben zu können, werden diese Peripheriegeräte 56 mit einer separaten Stromversorgungseinheit 60 am USB-Bus betrieben. Am USB-Bus verhalten sich diese Peripheriegeräte 56 wie USB-Peripheriegeräte mit geringem Leistungsbedarf.

[0015] Weiterhin besteht die Möglichkeit das USB-Peripheriegerät 50, 52, 54 mit höherer Betriebsspannung zu betreiben. Solche Peripheriegeräte 50, 52, 54 zum Betreiben am USB-Bus mit erhöhter Betriebsspannung werden auch als High Voltage Peripheriegeräte bezeichnet. Die Anschlußeinheiten 14 mit der Möglichkeit zum wahlweisen versorgen der Peripheriegeräte 50, 52, 54 mit erhöhter Betriebsspannung werden auch als High Voltage HUB's bezeichnet. Der Versorgungsstrom bleibt dabei unter 500 mA.

[0016] Ein High Voltage Peripheriegerät 50, 52, 54 verhält sich während des Anmeldevorgangs am USB-Bus gemäß USB-Spezifikation wie ein Low Power Peripheriegerät und wird durch den USB-Bus mit einer Spannung von 5 V Gleichspannung versorgt. Nach dem Anmeldevorgang schaltet die Steuerung 66, 68, 70 des Peripheriegerätes 50, 52, 54 intern eine ohmsche Last zu und ab, wodurch der Grenzwert von 100 mA sicher überschritten und unterschritten wird, jedoch wird der Grenzwert von 500 mA in keinem Fall überschritten. Durch diese Impulsfolge wird der Versorgungsstrom moduliert. Eine Steuerung 82 der Anschlußeinheit 14 vergleicht den aktuellen Stromwert mit dem Grenzwert

von 100 mA und ermittelt den Informationsgehalt der Modulation. Abhängig von dem Informationsgehalt stellt die Steuerung 62 der Anschlußeinheit 14 die Nennbetriebsspannung des Peripheriegerätes 50, 52, 54 von z. B. 60 V Gleichspannung an der USB-Schnittstelle 26, 28, 30 ein. Der Betrag der zum Betreiben des Peripheriegerätes 50, 52, 54 erforderlichen Nennbetriebsspannung wird aus dem Informationsgehalt des modulierten Stroms durch die Steuerung 62 ermittelt. Wird der Strom nicht vom Peripheriegerät 50, 52, 54 moduliert oder kann aus dem modulierten Strom keine Information ermittelt werden, wird die normale Busspannung des USB-Buses von 5 V Gleichspannung beibehalten.

[0017] Nach dem Entfernen des Peripheriegerätes 50, 52, 54, 56 vom USB-Bus, z.B. durch Trennen der Verbindung 34, 28, 38, 40 zwischen Peripheriegerät 50, 52, 54, 56 und der Anschlußeinheit 14 oder durch Abschalten des Peripheriegerätes 50, 52, 54, 56, detektiert die Überwachungseinheit 64, daß kein Stromfluß über die Schnittstelle 26, 28, 30, 32 vorhanden ist. Daraufhin werden im Personalcomputer 12 die zum Betreiben des Peripheriegerätes 50, 52, 54, 56 notwendigen Programmmodule deaktiviert. Weiterhin schaltet die Steuerung 62 der Anschlußeinheit 14 die erhöhte Spannung auf die normale Busspannung von 5 V Gleichspannung zurück, um eine Zerstörung eines im folgenden an diese Schnittstelle 26, 28, 30, 32 angeschlossenen weiteren Peripheriegerätes zu vermeiden. Das neu angeschlossene Peripheriegerät meldet sich am USB-Bus an und wird im Personalcomputer 12 registriert. Es hat danach die Möglichkeit durch eine Strommodulation die benötigte Nennbetriebsspannung der Anschlußeinheit 14 mitzuteilen. Die Anschlußeinheit 14 stellt dann die durch das neu angeschlossene Peripheriegerät benötigte Nennbetriebsspannung an der USB-Schnittstelle 26, 28, 30, 32 ein.

[0018] In Figur 2 ist ein Strom-Zeit Diagramm dargestellt, welches zeigt, daß durch Über- bzw. Unterschreiten eines Grenzwertes eine Bitfolge generiert ist. Die Zeit t ist auf der Abszissenachse und der Strom I auf der Ordinatenachse angetragen. Der modulierte Stromverlauf ist durch den mit 80 bezeichnete Graph dargestellt und der Graph des Über- bzw. unterschrittenen Grenzwert ist mit 82 bezeichnet. Je nach voreingestellter Datenübertragungsrate, die z.B. 1 bis 1200 Baud beträgt, ergeben sich unterschiedliche Zeitabstände zwischen den einzelnen Bits. Die Einteilung der Zeitachse erfolgt anhand der durch den Stromverlauf resultierenden Bitfolge. Aus der Bitfolge wird die Information über die Nennbetriebsspannung für das angeschlossene Peripheriegerät 50, 52, 54, 56 durch die Steuerung 62 der Anschlußeinheit 14 ermittelt.

Bezugszeichenliste

[0019]

10 Einrichtung zum Betreiben von elektri-

12	Personalcomputer
14	Anschlußeinheit
16	Peripheriegeräte
18	Stromversorgungseinheit
20, 22	Schnittstellenanschluß
24	Verbindungsleitung
26 bis 32	Schnittstellenanschluß
34 bis 40	Verbindungsleitung
42 bis 48	Schnittstellenanschluß
50 bis 56	Peripheriegerät
58, 60	Stromversorgungseinheit
62	Steuereinheit
64	Überwachungseinheit
66 bis 72	Steuereinheit
80	modulierter Stromverlauf
82	Grenzwert

20 Patentansprüche

1. Einrichtung zum Betreiben von elektrischen Geräten, mit einer Anschlußeinheit (14), die mindestens ein elektrisches Gerät (50, 52, 54, 56) mit elektrischer Leistung versorgt, wobei die Versorgung in einer Initialisierungsphase des elektrischen Gerätes (50, 52, 54, 56) mit einer vorbestimmten ersten Spannung erfolgt, das elektrische Gerät (50, 52, 54, 56) den Versorgungsstrom abhängig von der benötigten Nennbetriebsspannung moduliert, eine Steuerung (62) den modulierten Versorgungsstrom auswertet und abhängig vom Informationsgehalt der Modulation für die Betriebsphase die Nennbetriebsspannung in der Anschlußeinheit (14) einstellt.
2. Einrichtung nach Anspruch 1, dadurch **gekennzeichnet**, daß die Modulation durch eine Amplitudenmodulation erfolgt.
3. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Information durch eine Impulsfolge (80) des Versorgungsstroms definiert ist, wobei ein Stromgrenzwert (82) über- und unterschritten wird.
4. Einrichtung nach Anspruch 3, dadurch **gekennzeichnet**, daß der Grenzwert (82) 100 mA beträgt.
5. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Modulation des Versorgungsstroms durch Zu- und Abschalten einer ohmschen Last im Gerät (50, 52, 54, 56) erfolgt.
6. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die erste

- Spannung eine Gleichspannung von 5 V ist.
7. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Nennbetriebsspannung eine Sicherheitskleinspannung ist.
8. Einrichtung nach Anspruch 7, dadurch **gekennzeichnet**, daß die Nennbetriebsspannung eine Gleichspannung im Bereich zwischen 5 V und 60 V ist.
9. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß zwischen der Anschlußeinheit (14) und dem Gerät (50, 52, 54, 56) eine Vielzahl von Datenleitungen vorgesehen sind.
10. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß das mit der Anschlußeinheit (14) verbundene Gerät (50, 52, 54, 56) nach einer Schnittstellenvorgabe arbeitet.
11. Einrichtung nach Anspruch 10, dadurch **gekennzeichnet**, daß die Schnittstellenvorgabe eine USB (Universal Serial Bus) Schnittstellenvorgabe ist.
12. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß bei der Modulation der Strom von 500 mA durch das Gerät (50, 52, 54, 56) nicht überschritten wird.
13. Anschlußeinheit nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Anschlußeinheit (14) eine Überwachungseinrichtung (64) zum Überwachen der Verbindung zum Gerät (50, 52, 54, 56) enthält.
14. Einrichtung nach Anspruch 13, dadurch **gekennzeichnet**, daß die Überwachungseinheit (64) ein Trennen des Gerätes (50, 52, 54, 56) von der Anschlußeinheit (14) durch Überwachen des Versorgungsstroms feststellt.
15. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Steuerung (62) nach dem Trennen des Gerätes (50, 52, 54, 56) von der Anschlußeinheit (14) in der Anschlußeinheit (14) die erste Spannung wieder einstellt.
16. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß der Versorgungsstrom mit einer Datenübertragungsrate von 1 bis 1200 Baud moduliert wird.
17. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Anschlußeinheit (14) in einer Datenverarbeitungsanlage, insbesondere in einem Personalcomputer (12), angeordnet ist.
18. Anschlußeinheit, dadurch **gekennzeichnet**, daß sie mindestens ein elektrisches Gerät (50, 52, 54, 56) mit elektrischer Leistung versorgt, wobei das Versorgen in einer Initialisierungsphase mit einer ersten vorbestimmten Spannung erfolgt, daß eine Steuerung (62) in der Anschlußeinheit (14) den von dem angeschlossenen Gerät (50, 52, 54, 56) gemäß der benötigten Nennbetriebsspannung modulierten Versorgungsstroms auswertet, und daß die Steuerung (62) abhängig vom Informationsgehalt der Modulation für die Betriebsphase die Nennbetriebsspannung einstellt.

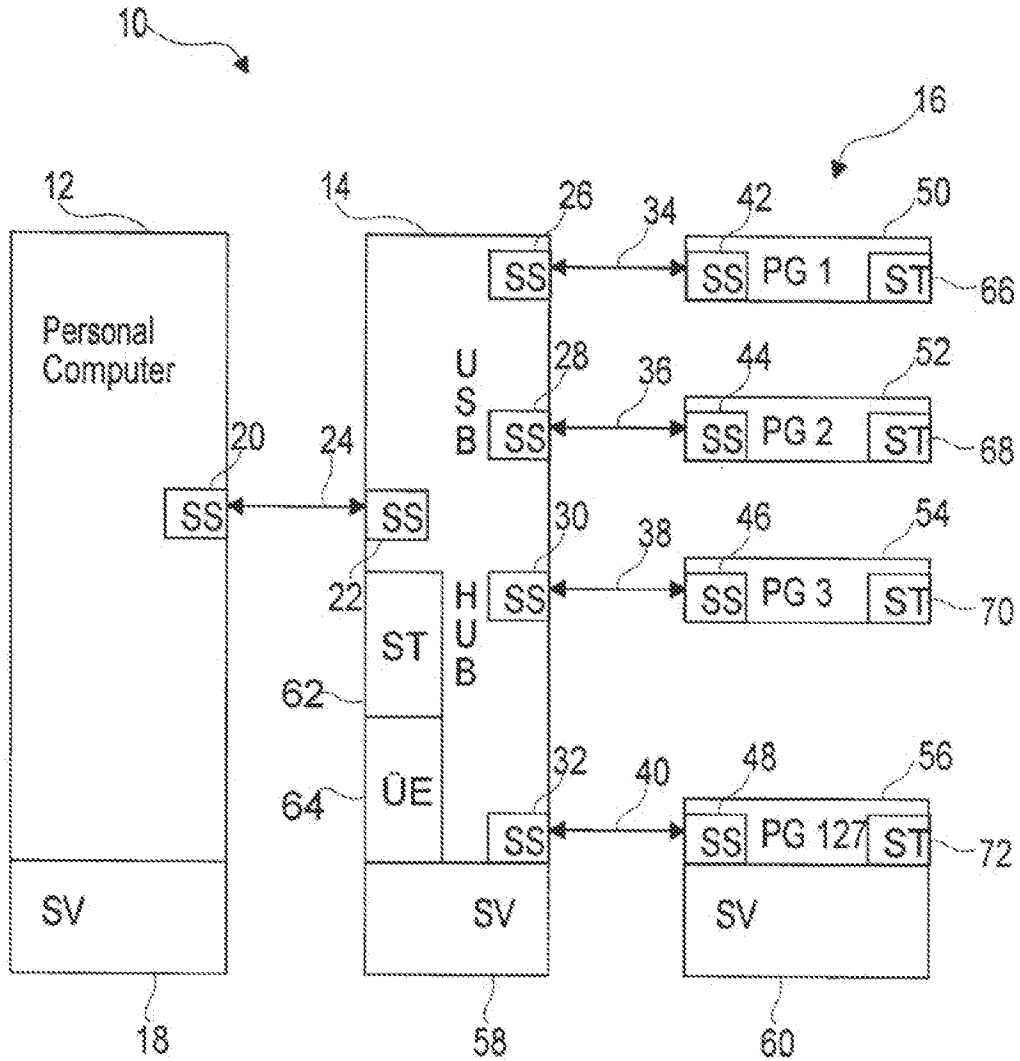
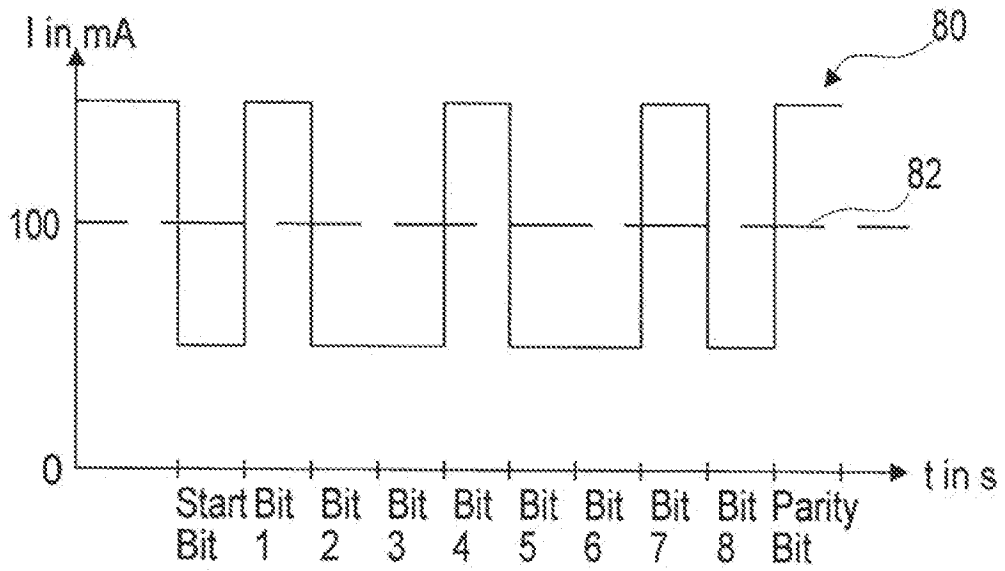


Fig. 1



Electronic Acknowledgement Receipt

EFS ID:	17904386
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Jason Daniel Eisenberg/Saqeef Ahmad
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3371_002REI0_First_Supplemental_IDS.pdf	1031644 4d2b1c59ac1d629983b9fb3e2cc2b72279fb5b7d	yes	10

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2	Foreign Reference	FP1_EP1117026A2.pdf	1327410 68c3802ad2bba2ef6c823ad0f2a7266465d9312a	no	7
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3	Non Patent Literature	NPL2_English_Language_Abst ract_EP1117026A2.pdf	147276 1ef2525c796757ba7c39c92a078ac15856655302	no	2
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4	Non Patent Literature	NPL1_SD_Association_Specific ation.pdf	1431490 862cfe29a5cf1e43756b80a8a79104e0fd91dea6	no	202
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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January 14, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Art Unit 2115
Attn: Mail Stop Amendment

Re: U.S. Reissue Patent Application
Application No. 13/902,227; Filing Date: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. First Supplemental Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 7 documents (**US1-US6** and **FP1**);
3. Form PTO/SB/08b (1 sheet) listing 2 documents (**NPL1-NPL2**); and
4. Copies of cited documents (**FP1** and **NPL1-NPL2**).

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

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Enclosure(s)
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for
Determining the Power
Consumption in Connection with
an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: Bae, JI H

Atty. Docket: 3371.002REI0

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

Atty. Dkt. No. 3371.002REI0

- c. The required fee is provided through online credit card payment authorization in the amount of \$180.00 in payment of the fee under 37 C.F.R. § 1.17(p).
4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$180.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:
- a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38 and MPEP 609.04(a)(III).

6. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP1** (EP 1 117 026 A2) appears to describe automatic increase of the operating voltage in peripheral devices, as noted in the corresponding English-language abstract provided as document **NPL2**.

7. Copies of documents **FP1** and **NPL1-NPL2** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents cited as documents **US1-US6** on the attached IDS Forms are submitted.

8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No., filed, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

9. It is requested that the examiner will review the prosecution and cited art in the parent application no. 10/401,338, filed March 26, 2003, (now U.S. Patent No. 7,278,033) in accordance with MPEP 2001.06(b), and indicate in the next

communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

10. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____.

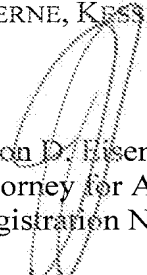
The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.


Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date:

1/14/14

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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/902,227 05/24/2013 Kimmo MYLLY 3371.002REI0 8765

26111 7590 01/29/2014
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

BAE, JI H

ART UNIT PAPER NUMBER

2115

MAIL DATE DELIVERY MODE

01/29/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Art Unit: 2115

DETAILED ACTION

The present application is being examined under the *pre-AIA* first to invent provisions.

Reissue Applications

For reissue applications filed before September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are “pre-AIA” provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the current provisions.

The Examiner notes that the Applicant has filed an AIA reissue declaration, which fails to comply with the Applicant's duty of disclosure under 37 CFR 1.63. A new, pre-AIA reissue declaration (PTO/SB/51) must be submitted, available at <http://www.uspto.gov>.

The reissue oath/declaration filed with this application, which has a filing date before September 16, 2012, is defective because:

1. It fails to identify the country of citizenship of the inventor (37 CFR 1.63(a)(3)).
2. It fails to include a statement that the person signing has reviewed and understands the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration as required by 37 CFR 1.63(b)(2).
3. It fails to include a statement that the person signing acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56 as required by 37 CFR 1.63(b)(3).

Art Unit: 2115

4. It fails to contain a statement that all errors which are being corrected in the reissue application up to the time of filing of the oath/declaration arose without any deceptive intention on the part of the applicant.

See **pre-AIA** 37 CFR 1.175 and MPEP § 1414. The Examiner notes that filing a pre-AIA reissue declaration will address the above deficiencies.

Claims 1-37 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-37 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claims 1-37 variously recite a "power consumption". However it is not always clear which power consumption is in view given that the claims recite a power consumption of a peripheral device and a power consumption of an electronic device to which the peripheral device is connected. The Examiner notes, for example, that claim 1 recites a step of

Art Unit: 2115

determining power consumption "in an electronic device", and yet the remaining steps of the method appear to be directed towards power consumption of the **peripheral device**. This ambiguity is compounded by recitations of power consumption without clarifying whether power consumption of the peripheral device or the electronic device is in view. The Examiner submits that the evidence would suggest that the invention is primarily directed towards power consumption of the peripheral device, and therefore recommends amending all instances of "power consumption" to reflect this.

Additionally, the claims variously recite a "maximum" power consumption. This language is indefinite because it uses the term "maximum" in such a manner that it conflicts with its ordinary meaning. The claims have established a default value and a limiting value which is higher than the default value, and that the power consumption of the peripheral device is set to a "maximum" which is between the default and the limiting value. The claims further establish that the limiting value is the highest allowable power consumption (claim 2). Given this, it would appear that the "maximum" power consumption is not actually the maximum. The evidence would suggest that the "maximum" value is merely an arbitrary power consumption value between the default and the limiting values, and therefore recommends deleting all instances of "maximum" to reflect this. The Examiner submits that there is no loss of meaning with this deletion, since "maximum" is not currently being used in a meaningful manner.

Claim 28 is rejected as being indefinite because it is unclear whether the Applicant intends to invoke 35 U.S.C. 112, sixth paragraph. The Examiner notes that the claim employs "means for" language which ordinarily is understood to invoke 35 U.S.C. 112, sixth paragraph. However, the newly added limitations further recite a means for setting the maximum power consumption that includes a **processor**. According to MPEP 2181, a proper invocation of 35 U.S.C. 112, sixth paragraph requires that "means for" be modified by functional language and

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not be modified by sufficient structure for achieving the function. In reciting a processor, the claim fails to clearly establish a non-structural modification of the "means for" language.

Conclusion

The Applicant is reminded that any amendments in a reissue application, including those filed in response to an Office Action, must comply with 37 CFR 1.173. In particular, all amendments must be marked in relation to the ***patented claims***, not the most recently filed claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Dunstan et al., U.S. Patent No. 5,964,879,

Saotome, U.S. Patent Application Publication No. 2004/0078498.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 9 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2115

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JI H BAE/
Primary Examiner, Art Unit 2115
U.S. Patent and Trademark Office
Phone: 571-272-7181
Fax: 571-273-7181
ji.bae@uspto.gov

Notice of References Cited	Application/Control No. 13/902,227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO	
	Examiner JI H. BAE	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-5,964,879	10-1999	Dunstan et al.	713/340
*	B US-2004/0078498	04-2004	Saotome, Makoto	710/008
C	US-			
D	US-			
E	US-			
F	US-			
G	US-			
H	US-			
I	US-			
J	US-			
K	US-			
L	US-			
M	US-			

FOREIGN PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
N					
O					
P					
Q					
R					
S					
T					

NON-PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
U	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
V					
W					
X					

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Application Number	13/902,227
			Filing Date	May 24, 2013
			First Named Inventor	Kimmo MYLLY
			Art Unit	2184
			Examiner Name	To be assigned
			Attorney Docket Number	3371.002RE10
Sheet	1	of	1	

U.S. PATENT DOCUMENTS						
Examiner initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
	US1	4,841,440		06-20-1989	Yonezu et al.	
	US2	5,483,656		01-09-1996	Ogrescu et al.	
	US3	5,532,945		07-02-1996	Robinson	
	US4	5,606,704		02-25-1997	Pierce et al.	
	US5	5,613,130		03-18-1997	Yeng et al.	
	US6	5,737,616		04-07-1998	Watanabe	
	US7	5,758,108		05-26-1998	Nakamura	
	US8	5,758,171		05-26-1998	Ramamurthy et al.	
	US9	5,884,086		03-16-1999	Amoni et al.	
	US10	5,892,729		04-06-1999	Holder, Jr.	
	US11	5,996,083		11-30-1999	Gupta et al.	
	US12	6,178,514 B1		01-23-2001	Wood	
	US13	6,477,388 B1		11-05-2002	Schmutz	
	US14	6,785,830 B1		08-31-2004	McKeen et al.	
	US15	6,859,882 B2		02-22-2005	Fung	

FOREIGN PATENT DOCUMENTS						
Examiner initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	GB 2 235 797 A		03-13-1991	Apple Computer	
	FP2	WO 98/41987 A1		09-24-1998	Hitachi LTD	
	FP3	WO 02/07494 A2		01-31-2002	Sierra Wireless Inc.	

1699182_1.DOCX

Examiner Signature	/Ji Bae/ (01/25/2014)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	13/902,227
		Filing Date	May 24, 2013
		First Named Inventor	Kimmo MYLLY
		Art Unit	2184
		Examiner Name	To be assigned
		Attorney Docket Number	3371.002REI0
		Sheet	1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	1 ²
	NPL1	USB Specification Revision, published April 27, 2000; pp.171-174	
	NPL2	English-Language Abstract for International Patent Publication No. 98/41987 A1, published September 24, 1998; 1 page	
	NPL3	Notice of Allowance mailed June 13, 2007 for U.S. Patent Application No.10/401,338, filed March 26, 2003; 12 pages	
	NPL4	Non-Final Rejection mailed September 22, 2005 for U.S. Application No.10/401,338, filed March 26, 2003; 10 pages	
	NPL5	Non-Final Rejection mailed July 14, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 8 pages	
	NPL6	Final Rejection mailed March 23, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 11 pages	
	NPL7	Final Rejection mailed December 27, 2006 for U.S. Application No.10/401,338, filed March 26, 2003; 8 pages	
	NPL8	International Search Report directed to related International Patent Application No. PCT/FI03/00233, mailed June 27, 2003; 5 pages	
	NPL9	International Preliminary Report on Patentability directed to related International Patent Application No. PCT/FI03/00233, mailed June 24, 2003; 7 pages	
	NPL10	European Search Report directed to related European Patent Application No. 03 708 304.5-1527, mailed November 24, 2006; 6 pages	

Examiner Signature	/Ji Bae/ (01/25/2014)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"7278033".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/13 17:55
S5	147	(kimmo near2 mylly).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/14 17:40
S6	12	S5 and power.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/14 17:41
S7	18152	713/3\$2.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/14 17:46
S8	4937	710/8.ccls. 710/301.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/14 17:48
S9	27	("5,752,050" "5,768,147" "6,092,209" "6,279,114" "6,697,883" "6,901,457" "4841440" "5,483,656" "5,532,945" "5,606,704" "5,613,130" "5,737,616" "5,758,108" "5,758,171" "5,884,086" "5,892,729" "5,996,083" "6'178,514" "6,477,388" "6,785,830" "6,859,882").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/14 17:50
S10	14	("4841440" "5532945" "5606704" "5613130" "5737616" "5758108" "5758171" "5884086" "5892729" "5996083" "6178514" "6477388" "6785830" "6859882").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/01/14 17:50
S11	21	S9 S10	US-PGPUB; USPAT; USOCR	OR	OFF	2014/01/14 17:51
S12	3	"8429203".pn.	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/22 21:47

			EPO; JPO; IBM_TDB			
S13	3	"8429103".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/22 21:48
S14	1649	(device peripheral) near5 (request\$3 demand\$3) with (voltage power) near5 (more additional higher greater)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/22 23:59
S15	1095	(minimum default) near4 (voltage power) with (stor\$3 read\$3) near5 (device peripheral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:00
S16	7	S14 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:00
S17	0	S16 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:00
S18	1801	(minimum default) near4 (voltage power) with (stor\$3 read\$3 memory) near5 (device peripheral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:00
S19	122	S18 and "713"/\$.cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:02
S20	17	S19 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:02
S21	434	S18 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:10
S22	6069	(peripheral card device) near5 request\$3 near5 power	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/23 00:10

			EPO; JPO; IBM_TDB			
S23	10532	(peripheral card device) with (power near5 (default minimum initial first nominal)) near5 (stor\$3 memory read\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:11
S24	6959	S22 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:12
S25	461	S22 and S23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:12
S26	127	S25 and "713"/\$.cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:12
S27	19	S26 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 00:12
S28	346	(peripheral device) near5 (send\$3 provid\$3 read\$3 stor\$3) with (power near5 (value\$1 level\$1 setting\$1 requirement\$1) near5 plurality)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 14:52
S29	48	S28 and "713"/\$.cls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 14:53
S30	9	S29 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 14:53
S31	775	(peripheral device) near6 (stor\$3 memory) with (power near5 (values levels requirements consumption) near5 (plurality maximum minimum))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 14:59
S32	132	S31 and ("713"/\$.cls. "710"/\$.cls.)	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/23 15:00

			EPO; JPO; IBM_TDB			
S33	22	S32 and @ad<"20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:00
S34	1075	(memory stor\$3) near6 plurality with (power near3 level\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:11
S35	59	S34 with (disk drive)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:11
S36	12	S35 and @ad<"20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:12
S37	1443	stor\$3 near6 plurality with (power near3 (level\$1 value\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:14
S38	466	S37 with (peripheral device disk drive flash)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:14
S39	44	S38 and ("713"/\$.cls. "710"/\$.cls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:14
S40	10	S39 and @ad<"20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/23 15:15
S41	3779	stor\$4 near5 power near5 (level\$1 value\$1 requirement\$1 consum\$5) with (read\$3 writ\$3 seek\$3 idl\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 19:51
S42	1386	S41 with (disk drive memory flash)	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/24 19:52

			EPO; JPO; IBM_TDB			
S43	18210	713/3\$2.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 19:52
S44	4942	710/8.ccls. 710/301.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 19:52
S45	110	S42 and (S43 S44)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 19:52
S46	18	S45 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 19:52
S47	56	stor\$4 near5 power near5 (level\$1 value\$1 requirement\$1 consum\$5) with read\$3 with writ\$3 with (seek\$3 idl\$3 access\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:22
S48	21	S47 with (memory table)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:23
S49	5	S48 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:23
S50	13	S47 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:24
S51	8	S50 not S49	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:24
S52	1875	(disk drive storage) with power near5 (level\$1 value\$1 requirement\$1 consum\$5) near5 plurality	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/24 20:26

			EPO; JPO; IBM_TDB			
S53	101119	power near5 (level\$1 value\$1 requirement\$1 consum\$5) with (memory table rom flash)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:26
S54	577	S52 and S53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S55	251	S52 same S53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S56	89	S55 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S57	161	S54 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S58	70	S55 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S59	21	S58 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:27
S60	8	S59 not fung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:29
S61	26	S57 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:32
S62	13	S61 not fung.in.	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2014/01/24 20:32

			EPO; JPO; IBM_TDB			
S63	101111	S63 not S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:33
S64	5	S62 not S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:33
S65	3471	(stor\$3 table memory rom flash) with power near5 (level\$1 value\$1 requirement\$1 consum\$5) near5 plurality	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:40
S66	1241	S65 same (peripheal device)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:40
S67	177	S66 and 713/3\$2.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:41
S68	20	S67 and @ad< "20030326"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2014/01/24 20:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	0	"means for setting the maximum power consumption".clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/01/13 23:19
S3	0	("maximum power consumption" with processor with indication with "received information").clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/01/13 23:20
S4	1	(maximum with "power consumption" with "default value" with "limiting value" with range).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2014/01/13 23:21

1/ 25/ 2014 12:16:05 AM

C:\Users\jbae\Documents\EAST\Workspaces\13902227_reissue.wsp




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BIB DATA SHEET

CONFIRMATION NO. 8765

SERIAL NUMBER 13/902,227	FILING or 371(c) DATE 05/24/2013 RULE	CLASS 713	GROUP ART UNIT 2115	ATTORNEY DOCKET NO. 3371.002RE10	
APPLICANTS Memory Technologies LLC, Las Vegas, NV, Assignee (with 37 CFR 1.172 Interest); INVENTORS Kimmo MYLLY, Julkujarvi, FINLAND; ** CONTINUING DATA ***** This application is a REI of 10/401,338 03/26/2003 PAT 7278033 ** FOREIGN APPLICATIONS ***** FINLAND 20020594 03/27/2002 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/26/2013					
Foreign Priority claimed <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No 35 USC 119(a-d) conditions met <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Verified and Acknowledged <u>/JI H BAE/</u> Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials _____	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 4	TOTAL CLAIMS 37	INDEPENDENT CLAIMS 7
ADDRESS STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005 UNITED STATES					
TITLE Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device					
FILING FEE RECEIVED 6080	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

Index of Claims 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed


-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
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	34	✓							
	35	✓							
	36	✓							

<i>Index of Claims</i> 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
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Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014							
	37	✓							

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO FIRST SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	13/902,227
	Filing Date	May 24, 2013
	First Named Inventor	Kimmo MYLLY
	Art Unit	2115
	Examiner Name	Bae, Ji H
Attorney Docket Number	3371.002REI0	
Sheet	1	of 1

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	5,752,050	05-12-1998	Hernandez et al.	
	US2	5,768,147	06-16-1998	Young	
	US3	6,092,209	07-18-2000	Holzhammer et al.	
	US4	6,279,114 B1	08-21-2001	Toombs et al.	
	US5	6,697,883 B1	02-24-2004	Jinnouchi	
	US6	6,901,457 B1	05-31-2005	Toombs et al.	


FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	EP 1 117 026 A2	07-18-2001	WINCOR NIXDORF GMBH & CO KG [DE]		

1797620_1

Examiner Signature	/Ji Bae/ (01/25/2014)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

Search Notes 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300, 320, 322	1/25/2014	/jb/
710	8, 301	1/25/2014	/jb/

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name search	1/25/2014	/jb/
EAST text search (see attached search history)	1/25/2014	/jb/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/JI H BAE/ Primary Examiner.Art Unit 2115
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for
Determining the Power
Consumption in Connection with
an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: BAE, Ji H

Atty. Docket: 3371.002REI0

Amendment and Reply Under 37 C.F.R. §§ 1.111 and 1.173(b)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated January 29, 2014, Applicant submits the following amendments and remarks. The remarks refer to a Declaration under 37 C.F.R. §1.132 from the inventor, Kimmo Mylly, which is submitted herewith.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19 0036.

Amendments to the Claims

Please replace the originally patented claims with the claims as shown below.

The claim identifiers, or lack thereof, below conform identically to the rules for reissue amendments set forth in 37 C.F.R. §§ 1.173(b)(2), (c), (d), and (e). (See also, M.P.E.P. §§ 1453 (II), (IV), and (V)).

1. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup state to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

2. (Amended) The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

3. (Amended) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption [set for] of the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption [set for] of the peripheral device is a value corresponding to said default value.

4. (Original Patent Claim) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

5. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

6. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

7. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup stage to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum [of the] power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

8. (Amended) The method according to claim 7, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

9. (Amended) A system comprising
a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

an electronic device with means for connecting the peripheral device and means for supplying power to the peripheral device, and

means for determining power consumption of the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is stored for the power consumption of the peripheral device,

wherein the means for determining the power consumption of the peripheral device comprise means for setting a maximum power consumption of the peripheral device to a value, which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

10. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

11. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises at least one bus, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

12. (Original Patent Claim) The system according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for controlling the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

13. (Original Patent Claim) The system according to the claim 9, wherein the electronic device is a portable electronic device.

14. (Original Patent Claim) The system according to claim 13, further comprising means for performing mobile station functions.

15. (Amended) An electronic device comprising:
means for connecting a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;
means for supplying power to the peripheral device; and
means for determining the power consumption of the peripheral device,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the means for determining the power consumption of the peripheral device comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

16. (Original Patent Claim) The electronic device according to claim 15, wherein it is a portable electronic device.

17. (Original Patent Claim) The electronic device according to claim 16, further comprising means for performing mobile station functions.

18. (Amended) A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption of the peripheral device;

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device.

19. (Original Patent Claim) The peripheral device according to claim 18, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

20. (Original Patent Claim) The peripheral device according to claim 18, further comprising
means for generating at least one clock signal and
means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

21. (Original Patent Claim) The peripheral device according to claim 18, further comprising
at least one bus and
means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

22. (Original Patent Claim) The peripheral device according to the claim 18, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for controlling the power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

23. (Original Patent Claim) The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device.

24. (Original Patent Claim) The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard.TM. peripheral device.

25. (Amended) An electronic device comprising:

a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine the power consumption of the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the means for determining the power consumption of the peripheral device comprise means for setting a maximum power consumption of the peripheral device to a value₂ which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

26. (Original Patent Claim) The electronic device according to claim 25, wherein it is a portable electronic device.

27. (Original Patent Claim) The electronic device according to claim 25, further comprising a memory configured to store the default value and the limiting value.

28. (Twice Amended) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption of the peripheral device;
a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,
wherein [the] a maximum power consumption of the peripheral device is set at a startup stage to said default value,
wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,
wherein the peripheral device comprises means for setting [a] the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, [and]
wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device, and
wherein the means for setting the maximum power consumption of the peripheral device is configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value.

29. (Original Patent Claim) The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device.

30. (New) The peripheral device of claim 28 further comprising:
a clock generator,
wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust a frequency of the clock generator in response to the received information from the electronic device.

31. (New) The peripheral device of claim 30, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the frequency of the clock generator to a first frequency corresponding to the power consumption of the peripheral device.

32. (New) The peripheral device of claim 28, wherein the peripheral device is a memory card.

33. (New) The peripheral device of claim 28, wherein the limiting value is a highest possible power consumption of the peripheral device.

34. (New) The peripheral device of claim 28 further comprising:
a plurality of memory banks configured to include at least an active mode and a power-saving mode.

35. (New) The peripheral device of claim 34, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the number of memory banks in the plurality of memory banks that are in the active mode in response to the received information from the electronic device.

36. (New) The peripheral device of claim 35, wherein the means for setting the maximum power consumption of the peripheral device is further configured to increase the number of memory banks in the plurality of memory banks that are in the active mode in response to the received information from the electronic device indicating the value for the maximum power consumption of the peripheral device being greater than the default value.

37. (New) The peripheral device of claim 28, wherein the default value is a lowest possible maximum power consumption for the peripheral device.

38. (New) The peripheral device of claim 28, wherein the means for setting the maximum power consumption of the peripheral device comprises a processor operable to set the maximum power consumption of the peripheral device to the value.

39. (New) The peripheral device of claim 32, wherein the memory card is a MultiMediaCard.

40. (New) The peripheral device of claim 28, wherein the range includes values other than the default value and the limiting value.

Remarks

Specification Amendments (37 C.F.R. § 1.173(b)(1) and (d))

No amendments are being sought in the patented specification.

Notification of Concurrent Proceeding (37 C.F.R. § 1.178(b))

Applicant has no knowledge of related concurrent proceedings.

Statement of Status of Currently Pending Claims (37 C.F.R. § 1.173(c))

Upon entry of the foregoing amendment, patent claims 1-29 and added new claims 30-40 are pending in the application, with claims 1, 7, 9, 15, 18, 25 and 28 being the independent claims. Patent claims 1-3, 7-9, 15, 18, 25 and 28 and previously presented new claims 30, 31 and 33-36 are sought to be amended. Applicant reserves the right to prosecute similar or broader claims, with respect to the amended claims, in the future. New claims 30-40 are sought to be added. New claims 30-37 were presented in the Preliminary Amendment and new claims 38-40 are presented for the first time herein. This response is believed to introduce no new matter, and its entry is respectfully requested.

A declaration under 37 C.F.R. §1.132 from the inventor, Kimmo Mylly, is submitted in support of the patentability of the claims.

Based on the following remarks and the declaration of Kimmo Mylly under 37 C.F.R. § 1.132, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Statement of Substance of Interview (37 C.F.R. § 1.133(b))

The Examiner and his QAS are thanked for their time in discussing the Office's position on the reissue declaration filed with this reissue application via multiple telephone calls and emails. The Examiner, his QAS, and the Office of Patent Legal Administration all agreed that the effective date for reissue applications with respect to the AIA rules would be the date the reissue application is filed, and not the effective date

of the underlying patent.¹ So agreement was finally reached that the reissue declaration in this application complied with all applicable rules, and the rejection would be withdrawn.

The Examiner is also thanked for extending to the Applicant (Applicant’s representative Jason Eisenberg, the patent owner, and the inventor), a telephone interview on June 25, 2014. During the interview the Examiner agreed that each of the proposed claim amendments presented via a GoToMeeting session would overcome the pending 35 U.S.C. § 112 rejections. Additionally, proposed changes were discussed by the Examiner for claim terms not explicitly rejected. Finally, the Examiner asked Applicant to provide support for arguments presented during the interview. All comments are reflected in this response, although not all proposed amendments are being sought at this time by the Applicant.

Explanation of Support for Added Claims (37 C.F.R. § 1.173(c))

Example support in the issued patent for the amended and new claims is shown in the table below.

<i>Claim</i>	<i>Example Support (Col:line or Fig./Element)</i>
28	[6:12-25]
30	[8:13-22]
31	[7:54-65]
32	[8:57-60]
33	[7:57-65]
34	[8:23-47]
35	[8:23-47]
36	[8:23-47]
37	[7:57-65]
38	[5:55-6:5]
39	[4:16-20]
40	[6:32-39]

¹ Applicant refers the Examiner a Petition Decision in 14/083,169 (June 20, 2014; p. 2) also holding that the proper rules for a reissue application is based on its filing date, and not on the effective date of any underlying patent.

Due to conformity with rules for reissue amendments, and for the convenience of the Examiner, Applicant presents the amendments to patent claim 28 and newly added claims 30, 31 and 33-36 below with markings to indicate the changes that have been made relative to these claims as filed on May 24, 2013. These annotated claims are shown with informal format as the required format is shown above. For example, the text of any added subject matter is shown by underlining the added text. The text of any deleted matter is shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters.

28. (Currently Amended) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption of the peripheral device;
a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,
wherein [the] a maximum power consumption of the peripheral device is set at a startup stage to said default value,
wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,
wherein the peripheral device comprises means for setting [a] the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value,
wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device, and
wherein the means for setting the maximum power consumption ~~includes a processor of the peripheral device is configured to read an indication of obtain~~ as indicated by from the received information₂, and to set the maximum power consumption of the peripheral device to the value ~~based on the indication~~.

30. (Currently Amended) The peripheral device of claim 28 further comprising:
a clock generator,
wherein the ~~processor~~ means for setting the maximum power consumption of the peripheral device is configured to adjust a frequency of the clock generator in response to the received information from the electronic device.

31. (Currently Amended) The peripheral device of claim 30, wherein the ~~processor~~ means for setting the maximum power consumption of the peripheral device is configured to adjust the frequency of the clock generator to a first frequency corresponding to the ~~maximum~~ power consumption of the peripheral device.

33. (Currently Amended) The peripheral device of claim 28, wherein the limiting value is a highest possible ~~maximum~~ power consumption of the peripheral device.

34. (Currently Amended) The peripheral device of claim 28 further comprising: a plurality of memory ~~blocks~~ banks, ~~wherein each of the plurality of memory banks~~ ~~blocks~~ is configured to include at least an active mode and a power-saving mode.

35. (Currently Amended) The peripheral device of claim 34, wherein the ~~processor~~ means for setting the maximum power consumption of the peripheral device is configured to adjust the number of memory banks ~~blocks~~ in the plurality of memory banks ~~blocks~~ that are in the active mode in response to the received information from the electronic device.

36. (Currently Amended) The peripheral device of claim 35, wherein the ~~processor~~ means for setting the maximum power consumption of the peripheral device is further configured to increase the number of memory banks ~~blocks~~ in the plurality of memory banks ~~blocks~~ that are in the active mode in response to the received information from the electronic device indicating the value for the maximum power consumption of the peripheral device being greater than the default value.

Rejection under 35 U.S.C. § 251

The Office Action rejected claims 1-37 under 35 U.S.C. § 251 based on an allegedly defective reissue declaration. As noted above, the Office and Examiner have agreed the declaration is in compliance with all applicable laws and rules. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 112, Second Paragraph

The Office Action rejected claims 1-37 under 35 U.S.C. § 112(b) or 35 U.S.C. § 112 (pre-AIA) second paragraph, as allegedly being indefinite. (Office Action, p. 3.) Applicant respectfully traverses without acquiescing to this rejection.

“Power Consumption”

The Office Action states that “it is not always clear which power consumption is in view given that the claims recite a power consumption of a peripheral device and a power consumption of an electronic device to which the peripheral device is connected.” (Office Action, p. 3.) Although Applicant believes the claims are definite, as discussed

and agreed to during the interview Applicant has amended claims 1-3, 7-9, 15, 18, 25 and 28 to specifically recite “power consumption” is of the peripheral device. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

“Maximum”

The Office Action also states that that “the claims variously recite a ‘maximum’ power consumption,” and that this “language is indefinite because it uses the term ‘maximum’ in such a manner that it conflicts with its ordinary meaning.” (Office Action, p. 4.) The Office Action recommends “deleting all instances of ‘maximum.’” (*Id.*) Applicant respectfully disagrees.

As discussed during the interview, the ’033 Patent teaches, *e.g.*:

The method according to the present invention is primarily characterized in determining, for the power consumption, at least a first maximum value and a second maximum value which is higher than the first maximum value, and setting, between the electronic device and the peripheral device, the maximum for the power consumption of the peripheral device to a value which is substantially between said first and second maximum values. (’033 Patent, 3:2-16.)

At least this passage from the ’033 Patent supports the definiteness of maximum as recited in the claims as patented without needing amendment. In one embodiment, the “maximum *power consumption*” is indeed a *maximum* value for the power consumption of the peripheral device between a default value and a limiting value controlled by the electronic device. Thus, Applicant disagrees with the Office Action’s statement that the claims use “the term ‘maximum’ in such a manner that it conflicts with its ordinary meaning.” (Office Action, p. 4.)

Additionally, during the interview the Examiner alleged “maximum” as claimed might be interpreted either as a threshold or a steady state value and requested clarification from Applicant. As discussed during the interview, the inventor explains in his declaration that a POSA (“person having ordinary skill in the art at the time of filing

the application”) would understand that “maximum,” as recited, at least “relates to a maximum limit on the fluctuating power consumption of a peripheral device.” (Mylly Decl. ¶8.) “[A POSA] recognized that the power consumption of a peripheral device fluctuated over the course of its operation. As a result, the ‘maximum power consumption’ recited in the claims relates to a limit on the fluctuating power consumption of the peripheral device.” (*Id.* at ¶12.) The declaration relies on multiple examples from the ’033 Patent to support the claim language. (*Id.* at ¶¶9-11 citing ’033 Patent 6:12-17 and 25-31, 8:23-47, and 10:5-14.) The Examiner is respectfully requested to contact Applicant’s representative if further explanation is required or if the Examiner intends to maintain the rejection.

Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claim 28

The Office Action rejected claim 28 as allegedly being indefinite because “a proper invocation of 35 U.S.C. 112, sixth paragraph requires that ‘means for’ be modified by functional language and *not* be modified by sufficient structure for achieving the function.” (Office Action, p. 4, emphasis in original.) Applicant respectfully traverses without acquiescing to the rejection.

Applicant has amended claim 28 to remove the reference to “a processor.” Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jason D. Eisenberg #43447/

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date: June 30, 2014

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
1871155_2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for
Determining the Power
Consumption in Connection with
an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: BAE, Ji H

Atty. Docket: 3371.002REI0

Declaration Under 37 C.F.R. § 1.132 by Kimmo Mylly

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

1. I, Kimmo Mylly, declare and state as follows:
2. I am the inventor of the claims of the above-captioned application.
3. I am the Managing Director of Helsinki Memory Technologies Oy (located in Finland), an affiliate company of Memory Technologies LLC, the assignee of United States Patent No. 7,278,033, which is in reissue under application no. 13/902,227. I am the sole inventor of the present application.
4. I hold a Bachelor of Science in computer engineering, and have over twelve years experience in the development and standardization of mobile mass storage memory sub-systems subject to standards including, *e.g.*, MMC, eMMC, SD and UFS, both as a technical contributor and as a workgroup chairman. Specifically, I have served as Chairman of several industry standard groups, including the MMCA Technical Committee (2004-2005), JEDEC JC64.1 (2005-2010), and the Joint Task Group of JEDEC and MMCA (2006-2009). I was also the Vice Chairman of the JEDEC J64 Committee from 2010-2012. In addition, I have also served as Nokia's representative to the SDA board (2008-2010).

5. I have reviewed U.S. Patent No. 7,278,033 (“the ’033 Patent”), the Reissue Application filed May 24, 2013 (“Reissue Application”), and the Non-Final Office Action dated January 29, 2014 (“Non-Final Office Action”).

6. I have been asked to explain the term “maximum power consumption” recited in the claims from the perspective of one of ordinary skill in the art at the time of the invention of the ’033 Patent.

7. I consider “one of ordinary skill in the art” in the technical field of power analysis in electronic devices, particularly, memory devices, to have a Bachelor’s Degree in electrical engineering or a related discipline, and at least three years experience working with electronic circuits. I consider myself able to interpret and understand the claims of the ’033 Patent from the perspective of “one of ordinary skill in the art.”

8. A person having ordinary skill in the art at the time of filing the application for the ’033 Patent (the “skilled artisan”) understood that the power consumption of a peripheral device fluctuates due to factors such as the type of memory access operations (*e.g.*, reads, writes), whether multiple memory banks are accessed at the same time (*e.g.*, *see* ’033 Patent, 8:23-31), the volume of data transmitted on the internal/external buses of the peripheral device, and activity inside the peripheral device controller (*e.g.*, accessing controller instructions and logical-to-physical mapping tables stored in SRAM embedded in the controller). Accordingly, the “maximum power consumption” recited in the claims relates to a maximum limit on the fluctuating power consumption of a peripheral device.

9. To further illustrate this point, the '033 Patent describes an example of setting the maximum power consumption by setting the clock frequency:

Next, the processor 13 of the peripheral device sets, for example the operating frequency of the clock generator 16 to a value corresponding to this maximum value for power consumption, for example to the highest possible frequency.

('033 Patent, 6:21-25, emphasis added.)

10. The skilled artisan knew that a memory device approached maximum power consumption at a particular clock frequency when it performed the most power-demanding operations (*e.g.*, writing multiple banks at the same time). Conversely, power consumption at that frequency setting would fluctuate below the maximum power consumption when the device performed less demanding operations (*e.g.*, accessing only one memory bank at a time). (*See, e.g.*, '033 Patent at 8:23-47.)

11. Support for “maximum power consumption” as a limit on the power consumption fluctuations of a peripheral device may be found throughout the '033 Patent specification. For example:

Moreover, the power consumption of memory cards of the MultiMediaCard™ type should thus not exceed the defined maximum limit.

('033 Patent, 2:30-32, emphasis added.)

Thus, a power control message is transmitted from the electronic device 1 to the peripheral device 2 (as indicated by a signal on a line 305). This power control message indicates the power consumption value which is to be set as the maximum value for the peripheral device 2, for example said second maximum limit.

('033 Patent, 6:12-17, emphasis added.)

In some embodiments, the bus widths within the processor can also be changed according to the maximum limit used for power consumption. Furthermore, the peripheral device 2 preferably informs the electronic device

1 that the power consumption has been limited to the requested value (as indicated by a signal on a line 307).

(’033 Patent, 6:25-31, emphasis added.)

Thus, the electronic device 1 may preferably set the power consumption of the camera used as the peripheral device 2 on the basis of how high a power can be supplied by the electronic device 1 to the peripheral device. In an advantageous embodiment of the invention, also the user of the electronic device 1 can set a maximum limit for the power consumption, wherein the user can, if necessary, e.g. reduce the maximum limit to prolong the time of operation of the electronic device.

(’033 Patent, 10:5-14, emphasis added.)

12. In summary, a person having ordinary skill in the art at the time of the invention recognized that the power consumption of a peripheral device fluctuated over the course of its operation. As a result, the “maximum power consumption” recited in the claims relates to a limit on the fluctuating power consumption of the peripheral device.

13. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the present patent application or any patent issued thereon.

Respectfully submitted,

Kimmo Mylly

Date: _____

I that the power consumption has been limited to the requested value (as indicated by a signal on a line 307).

(’033 Patent, 6:25-31, emphasis added.)

Thus, the electronic device 1 may preferably set the power consumption of the camera used as the peripheral device 2 on the basis of how high a power can be supplied by the electronic device 1 to the peripheral device. In an advantageous embodiment of the invention, also the user of the electronic device 1 can set a maximum limit for the power consumption, wherein the user can, if necessary, e.g. reduce the maximum limit to prolong the time of operation of the electronic device.

(’033 Patent, 10:5-14, emphasis added.)

12. In summary, a person having ordinary skill in the art at the time of the invention recognized that the power consumption of a peripheral device fluctuated over the course of its operation. As a result, the “maximum power consumption” recited in the claims relates to a limit on the fluctuating power consumption of the peripheral device.

13. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the present patent application or any patent issued thereon.

Respectfully submitted,



Kimmo Mylly

Date: 30.6.2014

1870834_1

Atty. Dkt. No. 3371.002REI0

Electronic Patent Application Fee Transmittal

Application Number:	13902227
Filing Date:	24-May-2013
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Filer:	Robert William Molitors/Tamara Haynesworth
Attorney Docket Number:	3371.002REI0

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	3	80	240

Miscellaneous-Filing:

Petition:

Patent-Appeals-and-Interference:

Post-Allowance-and-Post-Issuance:

Extension-of-Time:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 2 months with \$0 paid	1252	1	600	600
Miscellaneous:				
Total in USD (\$)				840

Electronic Acknowledgement Receipt

EFS ID:	19459171
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Robert William Molitors/Tamara Haynesworth
Filer Authorized By:	Robert William Molitors
Attorney Docket Number:	3371.002REI0
Receipt Date:	30-JUN-2014
Filing Date:	24-MAY-2013
Time Stamp:	18:48:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$840
RAM confirmation Number	7271
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		3371_002REI0Transmittal_EOT.pdf	1221834 89284dc18000f87e711f5dfd0ffec8a5f1dad4	yes	2
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Miscellaneous Incoming Letter	1	1	
		Extension of Time	2	2	
Warnings:					
Information:					
2		3371_002REI0AmendReply.pdf	8940850 5daa111fb63ed993fbf89132d46900918256a6f1	yes	18
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Amendment/Req. Reconsideration-After Non-Final Reject	1	1	
		Claims	2	11	
		Applicant Arguments/Remarks Made in an Amendment	12	18	
Warnings:					
Information:					
3	Affidavit-traversing rejectns or objectns rule 132	3371_002REI0Declaration132.pdf	2424389 a3b92ad2ce9de91adff6df90b12c12d9195a264cb	no	5
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Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32364 e1c1f03475a758e2b24a6743f33da1e2563a2682	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			12619437		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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June 30, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Art Unit 2115
Attn: Mail Stop Amendment

Re: U.S. Reissue Patent Application
Appl. No. 13/902,227; Filing Date: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of \$840.00 to cover:
\$600.00 Extension of Time Fee (2 Months);
\$240.00 Extra Claims Fee;
2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a);
3. Amendment and Reply Under 37 C.F.R. §§ 1.111 and 1.173(b); and
4. Declaration Under 37 C.F.R. § 1.132 by Kimmo Mylly.

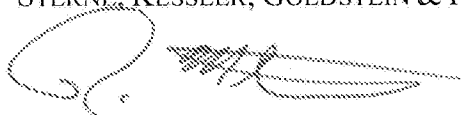
The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Robert W. Molitors
Attorney for Applicant
Registration No. 66,726

JDE/RWM/kc
Enclosure(s)
1872116_1.docx

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Docket Number (Optional)

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

3371.002REI0

Application Number
13/902,227Filed
May 24, 2013For
Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic DeviceArt Unit
2115Examiner
Bae, JI H

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
<input type="checkbox"/> One month (37 CFR 1.17(a)(1))	\$200	\$100	\$50	\$ _____
<input checked="" type="checkbox"/> Two months (37 CFR 1.17(a)(2))	\$600	\$300	\$150	\$ <u>600</u>
<input type="checkbox"/> Three months (37 CFR 1.17(a)(3))	\$1,400	\$700	\$350	\$ _____
<input type="checkbox"/> Four months (37 CFR 1.17(a)(4))	\$2,200	\$1,100	\$550	\$ _____
<input type="checkbox"/> Five months (37 CFR 1.17(a)(5))	\$3,000	\$1,500	\$750	\$ _____

 Applicant asserts small entity status. See 37 CFR 1.27. Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously. A check in the amount of the fee is enclosed. Payment by credit card. Form PTO-2038 is attached. The Director has already been authorized to charge fees in this application to a Deposit Account. The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to
Deposit Account Number 19-0036 Payment made via EFS-Web.**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

I am the

 applicant. attorney or agent of record. Registration number 66,726 attorney or agent acting under 37 CFR 1.34. Registration number _____

Signature

Robert W. Molitors

Typed or printed name

Date
June 30, 2014

Date

(202) 371-2600

Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*. * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/902,227	Filing Date 05/24/2013	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	06/30/2014	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	* 40	Minus	** 37	= 3	X \$80 = 240
	Independent (37 CFR 1.16(h))	* 7	Minus	***7	= 0	X \$420 = 0
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	240

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DORRETTA BROOKS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/902,227 05/24/2013 Kimmo MYLLY 3371.002RE10 8765

26111 7590 07/02/2014
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

BAE, JI H

ART UNIT PAPER NUMBER

2115

MAIL DATE DELIVERY MODE

07/02/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No. 13/902,227	Applicant(s) MYLLY, KIMMO	
	Examiner JI H. BAE	Art Unit 2115	

All participants (applicant, applicant's representative, PTO personnel):

- (1) JI H. BAE. (3) Tom Chia.
(2) Jason Eisenberg (reg. no. 43,447). (4) Kimmo Mylly, Rob Saltzberg.

Date of Interview: 25 June 2014.

Type: Telephonic Video Conference
 Personal [copy given to: applicant applicant's representative]

Exhibit shown or demonstration conducted: Yes No.
If Yes, brief description: _____.

Issues Discussed 101 112 102 103 Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1 and 28.

Identification of prior art discussed: n/a.

Substance of Interview

(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant proposed several amendment to overcome the rejection of claims 1-37 under 35 U.S.C. 112. The Examiner agreed that the proposals would overcome the rejections. Additionally, the applicant indicated that the means-plus-function language used in the claims was not intended to invoke 35 U.S.C. 112, sixth paragraph, thereby overcoming the rejection, and also entitling the Examiner to employ the broadest reasonable interpretation of the claim language without respect to any corresponding structure in the specification.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Attachment

/JI H BAE/
Primary Examiner, Art Unit 2115

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.



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EXAMINER

BAE, JI H

ART UNIT PAPER NUMBER

2115

MAIL DATE DELIVERY MODE

09/17/2014

PAPER

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Art Unit: 2115

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Response to Arguments

Applicant's arguments filed on June 30, 2014 have been fully considered and are persuasive. The rejection of claims 1-27 has been withdrawn. However, subsequent examination has revealed that additional rejections are necessary.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 28-37, 39, and 40 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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In the previous Office Action, the Examiner rejected claim 28 under 35 U.S.C. 112, second paragraph, on the grounds that it was unclear whether the Applicant intended to invoke 35 U.S.C. 112, sixth paragraph, due to the usage of means-plus-function language that included recitation of structure. MPEP 2181 stipulates that proper invocation of 35 U.S.C. 112, sixth paragraph, precludes the recitation of structure in means-plus-function claiming. While claim 28 seemingly appears to invoke 35 U.S.C. 112, sixth paragraph, in reciting a "means for setting the maximum power consumption", the claim introduces structure by reciting that the means comprises a **processor**. Although technically correct with respect to the embodiments taught in the specification (the specification does indeed teach that the means for carrying out the power consumption setting function is a processor programmed with the disclosed method steps), this language nevertheless runs afoul of the requirements outlined in MPEP 2181 for mean-plus-function claiming.

In the interview that took place on June 25, 2014, the grounds of rejection pertaining to 35 U.S.C. 112, second and sixth paragraphs, were discussed. Applicant clarified that the means-plus-function language employed in claim 28 was not intended to invoke 35 U.S.C. 112, sixth paragraph. In the Interview Summary mailed on July 2, 2014, the Examiner noted for the record that this admission therefore entitled the Examiner to employ the broadest reasonable interpretation of the claim language that is consistent with the specification, but without limitation to any corresponding structure in the specification. Subsequently, the Applicant filed an amendment to claim 28 that also removed the recitation of the processor, and moved the limitation to new dependent claim 38.

In removing the processor limitation from claim 28 **and** also enabling the Examiner to employ broadest reasonable interpretation for the means-plus-function limitations, claim 28 is no longer properly enabled by the current specification. The scope of enablement provided by the

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specification is not commensurate with the newly broadened scope of the claims (MPEP 2164.08). Whereas invocation of 35 U.S.C. 112, sixth paragraph, would have restricted the claim interpretation to the specific structure taught in the specification as corresponding to the recited function, Applicant's clarification as detailed in the Interview Summary now entitles the claims to be interpreted according to the broadest reasonable interpretation. Had the processor limitation been retained in claim 28, however, it would have served to control the broadest reasonable interpretation by explicitly limiting the means to a processor. But by **both** removing the processor limitation **and** not invoking 35 U.S.C. 112, sixth paragraph, the resulting claim is now purely functional, since there is no structure tied to the recited functions. In effect, the claims would read upon **any and all** apparatuses that perform the recited function, including embodiments not specifically enabled. For example, the broadest reasonable interpretation would include a circuit that is hardwired in an application-specific fashion to perform the power consumption setting functions, even though Applicant's specification only discloses a processor programmed to execute the same functions.

The Examiner recommends moving the limitations of claim 38 into claim 28 so as to limit the claims to the scope of enablement provided by the specification. Since Applicant has explicitly stated that the means-plus-function language of claim 28 is not intended to invoke 35 U.S.C. 112, sixth paragraph, such an amendment would not run afoul of MPEP 2181. Furthermore, the Examiner recommends amending claim 28 to recite that the processor is **programmed** to execute the claimed functions. A processor recited alone is merely a general purpose computer, whereas programming transforms a general purpose computer into a special purpose computer that is particularly configured for that function, thereby introducing appropriate structural limitations for an apparatus claim (MPEP 2114: apparatus claims must be distinguish from the prior art in terms of structure rather than function).

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The Examiner notes that this does not affect the interpretation of other claims that employ means-plus-function language, as the Applicant's clarification in the interview was understood to pertain solely to the means-plus-function language of claim 28 and its dependent claims.

The following is a quotation of 35 U.S.C. 112(b):

(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12 and 18-40 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 12 recites the limitation “the means for controlling the power consumption of the peripheral device” in lines 3-4. There is insufficient antecedent basis for this limitation in the claims. The Examiner notes that parent claim 9 recites a means for **determining** the power consumption of the peripheral device.

Claim 18 recites:

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device.

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Claim 18 is indefinite because the "wherein" limitations appear to further limit the previously recited means for connecting in a manner not consistent with the specification. The Examiner notes that claim 18 employs means-plus-function language where functions are recited in connection with various means which are associated with corresponding structures as disclosed in the specification. The highlighted functional limitations following "wherein" have the means for connecting as the most proximate means-plus-function limitation. However, the specification fails to disclose the recited power consumption setting features as being performed by the connecting means [**Fig. 1: connectors 8 and 11 and I/O blocks 9 and 12; col. 4, lines 39-47**]. The specification teaches that the power consumption setting features are carried out by a processor [**col. 5, lines 24-33, for example**]. This is consistent with the other claims, e.g., claim 15 recites a "means for determining the power consumption of the peripheral device" as proximate to the analogous "wherein" limitations. The "means for determining the power consumption" is understood to correspond to the processor as disclosed. The Examiner recommends amending claim 18 to include recitation of a means for determining power consumption using language similar to that of claim 15.

Claim 22 recites the limitation "the means for controlling the power consumption of the peripheral device" in lines 3-4. There is insufficient antecedent basis for this limitation in the claims. The Examiner notes that parent claim 18 lacks any recitation of a means for controlling power consumption of the peripheral device. Contingent upon amending claim 18 as recommended by the Examiner, claim 22 should also be amended to use similar language.

Claim 25 recites the limitation "the means for determining the power consumption of the peripheral device" in lines 12-13. There is insufficient antecedent basis for this limitation in the claim. There is no prior recitation of a means for determining power consumption of a

Art Unit: 2115

peripheral device. The Examiner notes that the claim previously recites a **power gauge** configured to determine the power consumption of the peripheral device.

Claim 28 is indefinite for reasons similar to claim 18, and should be amended accordingly.

Allowable Subject Matter

Claims 1-11 and 13-17 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 9 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 13/902,227

Page 8

Art Unit: 2115

/JI H BAE/


Primary Examiner, Art Unit 2115

U.S. Patent and Trademark Office

Phone: 571-272-7181

Fax: 571-273-7181

ji.bae@uspto.gov

Index of Claims 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed


-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014						
	1	✓	=						
	2	✓	=						
	3	✓	=						
	4	✓	=						
	5	✓	=						
	6	✓	=						
	7	✓	=						
	8	✓	=						
	9	✓	=						
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	26	✓	✓						
	27	✓	✓						
	28	✓	✓						
	29	✓	✓						
	30	✓	✓						
	31	✓	✓						
	32	✓	✓						
	33	✓	✓						
	34	✓	✓						
	35	✓	✓						
	36	✓	✓						

<i>Index of Claims</i> 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
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CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014						
	37	✓	✓						
	38		✓						
	39		✓						
	40		✓						



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EXAMINER

BAE, JI H

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PAPER

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	Examiner JI H. BAE	Art Unit 2115	

All participants (applicant, applicant's representative, PTO personnel):

- (1) JI H. BAE. (3) Todd Hopfinger (reg. no. 72,567).
(2) Jason Eisenberg (reg. no. 43,447). (4) _____.

Date of Interview: 22 October 2014.

Type: Telephonic Video Conference
 Personal [copy given to: applicant applicant's representative]

Exhibit shown or demonstration conducted: Yes No.
If Yes, brief description: _____.

Issues Discussed 101 112 102 103 Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 9, 12, 18, 22, 25, 28 and 38.

Identification of prior art discussed: n/a.

Substance of Interview

(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant clarified a miscommunication from the prior interview, and indicated that it was intended to invoke 112 6th in claim 28. However, since claim 38 recites structure, it was not intended to invoke 112 6th in claim 38. Based on this, Applicant argued that rejections against claim 28 should be withdrawn. Additionally, Applicant proposed amendments to claims 9, 12, 22, and 25 in order to overcome rejections, as well as arguments to show why claims 18 and 28 were definite. The Examiner agreed with the arguments and amendments of claims 9, 12, 18, 22, and 25. The Examiner further indicated that claims 28 and 38 would be deemed allowable as-is, pending consideration regarding the appropriateness of invoking 112 6th in an independent claim but not its dependent claims. The interview was additionally attended by Robert Saltzberg (reg. no. 36,910) and Tom Chia (reg. no. 63,990), representing the patent owners, as well as the inventor Kimmo Mylly.

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Attachment

/JI H BAE/
Primary Examiner, Art Unit 2115

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All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for
Determining the Power
Consumption in Connection with
an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: Bae, Ji H.

Atty. Docket: 3371.002REI0

Amendment and Reply Under 37 C.F.R. §§ 1.111 and 1.173

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated September 17, 2014, Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

Please replace the originally patented claims with the claims as shown below.

The claim identifiers, or lack thereof, below conform identically to the rules for reissue amendments set forth in 37 C.F.R. §§ 1.173(b)(2), (c), (d), and (e). (See also, M.P.E.P. §§ 1453 (II), (IV), and (V)).

1. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup state to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

2. (Amended) The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

3. (Amended) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption [set for] of the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption [set for] of the peripheral device is a value corresponding to said default value.

4. (Original Patent Claim) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

5. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

6. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

7. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup stage to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum [of the] power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

8. (Amended) The method according to claim 7, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

9. (Twice Amended) A system comprising

a peripheral device, wherein the peripheral device comprises:

a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device, and

means for setting the power consumption of the peripheral device at a startup stage to said default value and for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value,

wherein said range includes said default value and said limiting value,

wherein said limiting value is higher than said default value; and

an electronic device with means for connecting the peripheral device, [and] means for supplying power to the peripheral device, and means for determining power consumption of the peripheral device,

[wherein the power consumption of the peripheral device is set at a startup stage to said default value,]

[wherein at least said limiting value which is higher than said default value is stored for the power consumption,]

[wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and]

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

10. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein

the system comprises means for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

11. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises at least one bus, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

12. (Amended) The system according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for [controlling] setting the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

13. (Original Patent Claim) The system according to the claim 9, wherein the electronic device is a portable electronic device.

14. (Original Patent Claim) The system according to claim 13, further comprising means for performing mobile station functions.

15. (Amended) An electronic device comprising:
means for connecting a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

means for supplying power to the peripheral device; and

means for determining the power consumption of the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the means for determining the power consumption of the peripheral device comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

16. (Original Patent Claim) The electronic device according to claim 15, wherein it is a portable electronic device.

17. (Original Patent Claim) The electronic device according to claim 16, further comprising means for performing mobile station functions.

18. (Amended) A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption of the peripheral device;

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device.

19. (Original Patent Claim) The peripheral device according to claim 18, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

20. (Amended) The peripheral device according to claim 18, further comprising:
means for generating at least one clock signal and
means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

21. (Amended) The peripheral device according to claim 18, further comprising:
at least one bus and
means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

22. (Amended) The peripheral device according to the claim 18,
wherein the peripheral device is provided with two or more storage blocks, and
wherein the means for [controlling the] setting the maximum power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

23. (Original Patent Claim) The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device.

24. (Original Patent Claim) The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard.TM. peripheral device.

25. (Twice Amended) An electronic device comprising:
a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

Reply to Office Action of September 17, 2014

a power supply configured to supply power to the peripheral device; and
a power gauge configured to determine the power consumption of the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the [means for determining the power consumption comprise] power gauge comprises means for setting a maximum power consumption of the peripheral device to a value₂ which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum power [of the] consumption of the peripheral device.

26. (Original Patent Claim) The electronic device according to claim 25, wherein it is a portable electronic device.

27. (Original Patent Claim) The electronic device according to claim 25, further comprising a memory configured to store the default value and the limiting value.

28. (Twice Amended) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption of the peripheral device;

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein [the] a maximum power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value, is defined for the power consumption of the peripheral device,

wherein the peripheral device comprises means for setting [a] the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, [and]

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device, and

wherein the means for setting the maximum power consumption of the peripheral device is configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value.

29. (Original Patent Claim) The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device.

30. (New) The peripheral device of claim 28 further comprising:

a clock generator,

wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust a frequency of the clock generator in response to the received information from the electronic device.

31. (New) The peripheral device of claim 30, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the frequency of the clock generator to a first frequency corresponding to the maximum power consumption of the peripheral device.

32. (New) The peripheral device of claim 28, wherein the peripheral device is a memory card.

33. (New) The peripheral device of claim 28, wherein the limiting value is a highest possible power consumption of the peripheral device.

34. (New) The peripheral device of claim 28 further comprising:
a plurality of memory banks configured to include at least an active mode and a
power-saving mode.

35. (New) The peripheral device of claim 34, wherein the means for setting the
maximum power consumption of the peripheral device is configured to adjust the
number of memory banks in the plurality of memory banks that are in the active mode in
response to the received information from the electronic device.

36. (New) The peripheral device of claim 35, wherein the means for setting the
maximum power consumption of the peripheral device is further configured to increase
the number of memory banks in the plurality of memory banks that are in the active
mode in response to the received information from the electronic device indicating the
value for the maximum power consumption of the peripheral device being greater than
the default value.

37. (New) The peripheral device of claim 28, wherein the default value is a
lowest possible maximum power consumption for the peripheral device.

38. (New) The peripheral device of claim 28, wherein the means for setting the
maximum power consumption of the peripheral device comprises a processor operable to
set the maximum power consumption of the peripheral device to the value.

39. (New) The peripheral device of claim 32, wherein the memory card is a
MultiMediaCard.

40. (New) The peripheral device of claim 28, wherein the range includes values
other than the default value and the limiting value.

Remarks

Notification of Concurrent Proceeding (37 C.F.R. § 1.178(b))

Applicant has no knowledge of related concurrent proceedings.

Statement of Status of Currently Pending Claims (37 C.F.R. § 1.173(c))

Upon entry of the foregoing amendment, patent claims 1-29 and previously added new claims 30-40 are pending in the application, with claims 1, 7, 9, 15, 18, 25, and 28 being the independent claims. Patent claims 9, 12, 20-22, and 25 and previously presented new claim 31 are sought to be amended. Applicant reserves the right to prosecute similar or broader claims, with respect to the amended claims, in the future. This response is believed to introduce no new matter, and its entry is respectfully requested.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn. Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Statement of Substance of Interview (37 C.F.R. § 1.133(b))

The Examiner is thanked for extending the Applicant a telephone and GoToMeeting Interview held on October 23, 2014. Pursuant to 37 C.F.R. § 1.133, Applicant provides the following statement of substance of the Interview. Applicant has reviewed and agrees with the Interview Summary mailed October 27, 2014, except as may be noted herein.

As the Examiner confirms in the Interview Summary, the Applicant and Examiner agreed that there was a miscommunication in the interview held on June 25, 2014. Applicant confirmed that the means-plus-function language recited in claim 28 was intended to invoke 35 U.S.C. § 112, sixth paragraph. The Examiner agreed that claims 28 and 38 would be deemed allowable if Applicant can show “the appropriateness

of invoking 1126th [sic] in an independent claim but not its dependent claims.” (Interview Summary of October 27, 2014.)

The Federal Circuit has found this claiming scheme appropriate. For example, when asked to construe independent means claims and dependent structure claims the Court found no issues with this claiming scheme and held “[i]t is settled law, however, that independent claims containing means plus function limitations do not have the same literal scope as dependent claims reciting specifically the structure that performs the stated function.” *Medtronic, Inc. v. Advanced Cardiovascular Systems, Inc.*, 248 F.3d 1303, 1313 (Fed. Cir. 2001). In *Medtronic*, the court relied on *Laitram Corp. v. Rexnord, Inc.*, 939 F.2d 1533, 1538 (Fed. Cir. 1991), noting *Laitram* explained:

[i]n any event, [the independent and dependent claims] do not ... thereby have exactly the same scope and, thus, claim differentiation is maintained. [The independent claim] remains broader than [the dependent claim]. Literally, [the independent claim] covers the structure described in the specification and equivalents thereof. [The dependent claim] does not literally cover equivalents

Medtronic, 248 F.3d at 1313.

These holdings comport with Applicant’s arguments during the Interview. So, the Examiner should replace the tentative agreement noted during the Interview and in the Interview Summary with complete agreement, and withdraw the pending 35 U.S.C. § 112, first paragraph and second paragraph, rejections of claim 28 (and 38).

Additionally, the Examiner agreed that claim 18 met all requirements under 35 U.S.C. § 112, second paragraph. So the Examiner agreed to withdraw the rejection.

Finally, the Examiner agreed the proposed claim amendments presented via the GoToMeeting session would overcome the pending rejections of claims 12, 22, and 25 under 35 U.S.C. § 112, second paragraph.

The substance of the October 23 interview is further incorporated in the remarks below.

Explanation of Support for Amended Claims (37 C.F.R. § 1.173(c))

Example support in the issued patent for the *substantively* amended claims is shown in the table below.

Claim	Example Support (Column: Line or Figure/Element)
9	<i>e.g.</i> , [4:33-38][4:44-46][5:51-58][5:56-62][6:17-25][7:57-65][8:23-47]
12	<i>e.g.</i> , [8:23-31]
22	<i>e.g.</i> , [8:23-31]
25	<i>e.g.</i> , [4:33-38][4:44-46][5:51-58][5:56-62][6:17-25][7:57-65][8:23-47]
31	<i>e.g.</i> , [6:17-25][7:54-65]

Due to conformity with rules for reissue amendments, and for the convenience of the Examiner, Applicant presents the amendments to patent claims 9, 12, 22, and 25 and previously presented new claim 31 below with markings to indicate the changes that have been made relative to these claims as filed on June 30, 2014. These annotated claims are shown with informal format as the required format is shown above. For example, the text of any added subject matter is shown by underlining the added text. The text of any deleted matter is shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters.

Amendments to claims 9, 12, 22, 25, and 31

9. (Currently Amended) A system comprising
a peripheral device, wherein the peripheral device comprises:
a memory, said memory storing a default value and a limiting value for
power consumption of the peripheral device, and
means for setting the power consumption of the peripheral device at a
startup stage to said default value and for setting a maximum power consumption
of the peripheral device to a value which is in a range from said default value to
said limiting value,
wherein said range includes said default value and said limiting value,
wherein said limiting value is higher than said default value; and
an electronic device with means for connecting the peripheral device, ~~[[and]]~~
means for supplying power to the peripheral device, and means for determining power
consumption of the peripheral device,
~~wherein the power consumption of the peripheral device is set at a startup stage~~
~~to said default value,~~
~~wherein at least said limiting value, which is higher than said default value, is~~
~~stored for the power consumption of the peripheral device,~~
~~wherein the means for determining the power consumption of the peripheral~~
~~device comprise means for setting a maximum power consumption of the peripheral~~

~~device to a value, which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and~~

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum power consumption of the peripheral device.

12. (Currently Amended) The system according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for ~~controlling~~ setting the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

22. (Currently Amended) The peripheral device according to the claim 18, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for ~~controlling the~~ setting the maximum power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

25. (Currently Amended) An electronic device comprising:
a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for power consumption of the peripheral device;
a power supply configured to supply power to the peripheral device; and
a power gauge configured to determine the power consumption of the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,

~~wherein the means for determining the power consumption of the peripheral device comprise~~ power gauge comprises means for setting a maximum power consumption of the peripheral device to a value, which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum power consumption of the peripheral device.

31. (Currently Amended) The peripheral device of claim 30, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the frequency of the clock generator to a first frequency corresponding to the maximum power consumption of the peripheral device.

Amendments to claims 20 and 21

Claims 20 and 21 have been amended to add a colon (':') after the transitional phrase "comprising."

Rejection under 35 U.S.C. § 112, First Paragraph

Claims 28-37, 39, and 40 stand rejected under 35 U.S.C. § 112(a) or 35 U.S.C. § 112 (pre-AIA), first paragraph, as allegedly failing to comply with the enablement requirement. (Office Action, p. 2.) Applicant respectfully traverses without acquiescing to this rejection.

As noted in the Interview Summary, the Examiner has agreed to withdraw this rejection so long as Applicant demonstrates that a dependent *structure* claim properly depends from an independent *means* claim. As Applicant has shown this above, the Examiner is respectfully requested to reconsider and withdraw the rejection.

Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 12 and 18-40 stand rejected under 35 U.S.C. § 112(b) or 35 U.S.C. § 112 (pre-AIA), second paragraph, as allegedly being indefinite. (Office Action, pp. 5-7.) Applicant respectfully traverses without acquiescing to this rejection.

Claims 12, 22, and 25

Claims 12, 22, and 25 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for "antecedent basis" issues. (Office Action, pp. 5-7.) Again, Applicant respectfully disagrees without acquiescing to the rejection. Nevertheless, these claims, as well as independent claim 9, have been amended for clarity and to expedite prosecution. The Examiner agreed during the Interview that the proposed amendments, similar to the amendments above, would overcome these rejections. Accordingly, Applicant respectfully requests that the rejections be reconsidered and withdrawn.

Claims 18-40

Claims 18-40 stand rejected as allegedly being unclear as to what claim feature the “wherein” clauses were associated with in claims 18 and 28. As noted in the Interview Summary, the Examiner has agreed to withdraw this rejection based on Applicant’s explanation that the “wherein” clauses are associated with the “peripheral device” claim feature. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Other

Applicant wishes to clarify the comments regarding the pre/post AIA status of this reissue application made on pages 12 to 13 of the June 30, 2014 Office Action Reply. Applicant’s statements were only directed to post-AIA rules regarding declarations. Applicant agrees with the Office that all other aspects of the examination of this reissue application should be based on pre-AIA rules.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jason D. Eisenberg #43447/

Jason D. Eisenberg
Attorney for Applicant
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Date: November 6, 2014

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Electronic Acknowledgement Receipt

EFS ID:	20628450
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Todd Michael Hopfinger
Filer Authorized By:	
Attorney Docket Number:	3371.002REI0
Receipt Date:	06-NOV-2014
Filing Date:	24-MAY-2013
Time Stamp:	16:23:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment.pdf	978900 9b9a663248635da71bce99a18e114acdb5f2a4de	yes	18

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Transmittal Letter		1	1
Amendment/Req. Reconsideration-After Non-Final Reject		2	2
Claims		3	11
Applicant Arguments/Remarks Made in an Amendment		12	18

Warnings:

Information:

Total Files Size (in bytes):	978900
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

JASON D. EISENBERG
DIRECTOR
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November 6, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Art Unit 2115
Attn: Mail Stop Amendment

Re: U.S. Reissue Patent Application
Appl. No. 13/902,227; Filing Date: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

Transmitted herewith for appropriate action is the following document:

1. Amendment and Reply Under 37 C.F.R. §§ 1.111 and 1.173.

The above-listed document is filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/TMH/eet
Enclosure

1926396_1.DOCX

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/902,227	Filing Date 05/24/2013	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	11/06/2014	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	* 40	Minus	** 40	= 0	X \$80 = 0
	Independent <small>(37 CFR 1.16(h))</small>	* 7	Minus	***7	= 0	X \$420 = 0
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
					TOTAL ADD'L FEE	0

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	X \$ =
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	X \$ =
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/STEFANIE BRYCE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
13/902,227 05/24/2013 Kimmo MYLLY 3371.002REI0 8765

26111 7590 02/02/2015
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

BAE, JI H

ART UNIT PAPER NUMBER

2115

MAIL DATE DELIVERY MODE

02/02/2015

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Art Unit: 2115

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Reissue Applications

The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following:

The error statement provided in the original declaration filed on May 24, 2013 is no longer applicable to the claims in their present form. The error statement reads:

Applicant seeks to clarify claim 28 by additionally reciting:
"wherein means for setting the maximum power consumption includes a processor configured to read an indication of the value from the received information and to set the maximum power consumption to the value based on the indication."

Claim 28 as currently amended does not incorporate the language specified in the error statement.

Claims 1-40 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

Art Unit: 2115


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 9 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JI H BAE/
Primary Examiner, Art Unit 2115
U.S. Patent and Trademark Office
Phone: 571-272-7181
Fax: 571-273-7181
ji.bae@uspto.gov

Index of Claims 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed


-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014	01/29/2015					
	1	✓	=	✓					
	2	✓	=	✓					
	3	✓	=	✓					
	4	✓	=	✓					
	5	✓	=	✓					
	6	✓	=	✓					
	7	✓	=	✓					
	8	✓	=	✓					
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	29	✓	✓	✓					
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	31	✓	✓	✓					
	32	✓	✓	✓					
	33	✓	✓	✓					
	34	✓	✓	✓					
	35	✓	✓	✓					
	36	✓	✓	✓					

<i>Index of Claims</i> 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014	01/29/2015					
	37	✓	✓	✓					
	38		✓	✓					
	39		✓	✓					
	40		✓	✓					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for Determining
the Power Consumption in Connection
with an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: Bae, JI H

Atty. Docket: 3371.002REI0

Reply Under 37 C.F.R. § 1.116

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated February 2, 2015, Applicant submits the following Remarks. No amendments are made in this Reply. All changes shown in the claims were previously submitted and entered by the Examiner, and are being shown herein pursuant to the Rules.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Listing of the Claims

The claim identifiers, or lack thereof, below conform identically to the rules for reissue amendments set forth in 37 C.F.R. §§ 1.173(b)(2), (c), (d), and (e). (See also, M.P.E.P. §§ 1453 (II), (IV), and (V)). All amendments to the claims were made previously, and entered by the Examiner. No new changes to the claims are sought in this Reply.

1. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup state to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein information is transferred from the electronic device to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

2. (Amended) The method according to claim 1, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

3. (Amended) The method according to claim 1, wherein at least one content is stored in the peripheral device, for use in connection with the electronic device, wherein at a stage of storing the content, the power consumption [set for] of the peripheral device is a value corresponding to said limiting value, and at a stage of using the content, the power consumption [set for] of the peripheral device is a value corresponding to said default value.

4. (Original Patent Claim) The method according to the claim 1, wherein at least one clock signal is generated in the peripheral device and wherein the power consumption of the peripheral device is controlled by adjusting the frequency of at least one clock signal.

5. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device comprises at least one bus and that the power consumption of the peripheral device is controlled by controlling a width of said bus.

6. (Original Patent Claim) The method according to the claim 1, wherein the peripheral device is provided with two or more storage blocks controlled by controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

7. (Amended) A method comprising:

initiating determination of power consumption in an electronic device, to which a peripheral device is connected, and from which [the] power is supplied to the peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

setting the power consumption of the peripheral device at a startup stage to said default value;

reading from the memory at least said limiting value, which is higher than said default value; and

setting [the] a maximum [of the] power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value,

wherein messages are transferred between the electronic device and the peripheral device for setting the maximum [of the] power consumption of the peripheral device to a value in a range from said default value to said limiting value, wherein the range includes said default value and said limiting value.

8. (Amended) The method according to claim 7, wherein said limiting value is used as a highest allowable value for the power consumption of the peripheral device.

9. (Twice Amended) A system comprising
a peripheral device, wherein the peripheral device comprises:
a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device, and
means for setting the power consumption of the peripheral device at a startup stage to said default value and for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value,
wherein said range includes said default value and said limiting value,
wherein said limiting value is higher than said default value; and
an electronic device with means for connecting the peripheral device, [and] means for supplying power to the peripheral device, and means for determining power consumption of the peripheral device,

[wherein the power consumption of the peripheral device is set at a startup stage to said default value,]

[wherein at least said limiting value which is higher than said default value is stored for the power consumption,]

[wherein the means for determining the power consumption comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and]

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

10. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises means for generating at least one clock signal, and wherein the system comprises means

Reply to Office Action of February 2, 2015

for controlling the power consumption of the peripheral device by adjusting the frequency of said at least one clock signal.

11. (Original Patent Claim) The system according to claim 9, wherein the peripheral device comprises at least one bus, and wherein the system comprises means for controlling the power consumption of the peripheral device by adjusting a bus width of the peripheral device.

12. (Amended) The system according to the claim 9, wherein the peripheral device is provided with two or more storage blocks, and wherein the means for [controlling] setting the power consumption of the peripheral device comprise means for adjusting a number of storage blocks processed by the peripheral device substantially simultaneously.

13. (Original Patent Claim) The system according to the claim 9, wherein the electronic device is a portable electronic device.

14. (Original Patent Claim) The system according to claim 13, further comprising means for performing mobile station functions.

15. (Amended) An electronic device comprising:
means for connecting a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;
means for supplying power to the peripheral device; and
means for determining the power consumption of the peripheral device,
wherein the power consumption of the peripheral device is set at a startup stage to said default value,

Atty. Dkt. No. 3371.002REI0

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the means for determining the power consumption of the peripheral device comprise means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the means for supplying the power is configured to transfer information to the peripheral device for setting the maximum [of the] power consumption of the peripheral device.

16. (Original Patent Claim) The electronic device according to claim 15, wherein it is a portable electronic device.

17. (Original Patent Claim) The electronic device according to claim 16, further comprising means for performing mobile station functions.

18. (Amended) A peripheral device comprising:
a memory storing a default value and a limiting value for power consumption of the peripheral device;

means for connecting the peripheral device to an electronic device for supplying power to the peripheral device,

wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value₂ which is higher than said default value₂ is defined for the power consumption of the peripheral device,

wherein the peripheral device comprises means for setting a maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device.

19. (Original Patent Claim) The peripheral device according to claim 18, wherein at least one content is stored in the peripheral device for use in connection with the electronic device.

20. (Amended) The peripheral device according to claim 18, further comprising:
means for generating at least one clock signal and
means for controlling the power consumption of the peripheral device by frequency control of said at least one clock signal.

21. (Amended) The peripheral device according to claim 18, further comprising:
at least one bus and
means for controlling the power consumption of the peripheral device by controlling a bus width of said bus of the peripheral device.

22. (Amended) The peripheral device according to the claim 18,
wherein the peripheral device is provided with two or more storage blocks, and
wherein the means for [controlling the] setting the maximum power consumption of the peripheral device comprise means for controlling a number of storage blocks processed by the peripheral device substantially simultaneously.

23. (Original Patent Claim) The peripheral device according to the claim 18, wherein said default value and at least one limiting value are stored in the peripheral device.

24. (Original Patent Claim) The peripheral device according to the claim 18, wherein said peripheral device is a MultiMediaCard™ peripheral device.

25. (Twice Amended) An electronic device comprising:

a connector configured to connect to a peripheral device, wherein the peripheral device comprises a memory, said memory storing a default value and a limiting value for [the] power consumption of the peripheral device;

a power supply configured to supply power to the peripheral device; and

a power gauge configured to determine the power consumption of the peripheral device, wherein the power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,

wherein the [means for determining the power consumption comprise] power gauge comprises means for setting a maximum power consumption of the peripheral device to a value, which is in a range from said default value to said limiting value, said range including said default value and said limiting value, and

wherein the electronic device is configured to transfer information to the peripheral device for setting the maximum power [of the] consumption of the peripheral device.

26. (Original Patent Claim) The electronic device according to claim 25, wherein it is a portable electronic device.

27. (Original Patent Claim) The electronic device according to claim 25, further comprising a memory configured to store the default value and the limiting value.

28. (Twice Amended) A peripheral device comprising:

a memory storing a default value and a limiting value for power consumption of the peripheral device;

a connector configured to connect the peripheral device to an electronic device for supplying power to the peripheral device,

wherein [the] a maximum power consumption of the peripheral device is set at a startup stage to said default value,

wherein at least said limiting value, which is higher than said default value, is defined for the power consumption of the peripheral device,

wherein the peripheral device comprises means for setting [a] the maximum power consumption of the peripheral device to a value which is in a range from said default value to said limiting value, said range including said default value and said limiting value, [and]

wherein the peripheral device is configured to receive information from the electronic device for setting the maximum [of the] power consumption of the peripheral device, and

wherein the means for setting the maximum power consumption of the peripheral device is configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value.

29. (Original Patent Claim) The peripheral device according to the claim 28, wherein said default value and at least one limiting value are stored in the peripheral device.

30. (New) The peripheral device of claim 28 further comprising:

a clock generator,

wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust a frequency of the clock generator in response to the received information from the electronic device.

31. (New) The peripheral device of claim 30, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the frequency of the clock generator to a first frequency corresponding to the maximum power consumption of the peripheral device.

32. (New) The peripheral device of claim 28, wherein the peripheral device is a memory card.

33. (New) The peripheral device of claim 28, wherein the limiting value is a highest possible power consumption of the peripheral device.

34. (New) The peripheral device of claim 28 further comprising:
a plurality of memory banks configured to include at least an active mode and a power-saving mode.

35. (New) The peripheral device of claim 34, wherein the means for setting the maximum power consumption of the peripheral device is configured to adjust the number of memory banks in the plurality of memory banks that are in the active mode in response to the received information from the electronic device.

36. (New) The peripheral device of claim 35, wherein the means for setting the maximum power consumption of the peripheral device is further configured to increase the number of memory banks in the plurality of memory banks that are in the active mode in response to the received information from the electronic device indicating the value for the maximum power consumption of the peripheral device being greater than the default value.

37. (New) The peripheral device of claim 28, wherein the default value is a lowest possible maximum power consumption for the peripheral device.

38. (New) The peripheral device of claim 28, wherein the means for setting the maximum power consumption of the peripheral device comprises a processor operable to set the maximum power consumption of the peripheral device to the value.

Reply to Office Action of February 2, 2015

Kimmo MYLLY
Appl. No. 13/902,227

39. (New) The peripheral device of claim 32, wherein the memory card is a MultiMediaCard.

40. (New) The peripheral device of claim 28, wherein the range includes values other than the default value and the limiting value.

Atty. Dkt. No. 3371.002REI0

Remarks

Reconsideration of this Application is respectfully requested. Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejection under 35 U.S.C. § 251

Claims 1-40 stand rejected because the error statement provided in the original reissue declaration filed on May 24, 2013 is no longer applicable to claim 28 as currently amended. (Office Action, p. 2.) To comply with MPEP 1414.01, Applicant has filed a supplemental reissue declaration concurrently with this reply. Accordingly, Applicant respectfully submits that the rejection of claims 1-40 under 35 U.S.C. § 251 be reconsidered and withdrawn.

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided. Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date: 2/24/15

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
1965597_3.DOCX

Atty. Dkt. No. 3371.002REI0

Electronic Acknowledgement Receipt

EFS ID:	21585045
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Todd Michael Hopfinger
Filer Authorized By:	
Attorney Docket Number:	3371.002REI0
Receipt Date:	24-FEB-2015
Filing Date:	24-MAY-2013
Time Stamp:	15:40:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Reply.pdf	564472 <small>d88eb222ec2081d12e5df8d659901f8bb4146958</small>	yes	15

Multipart Description/PDF files in .zip description			
	Document Description	Start	End
	Transmittal Letter	1	1
	Oath or Declaration filed	2	3
	Response After Final Action	4	4
	Claims	5	14
	Applicant Arguments/Remarks Made in an Amendment	15	15

Warnings:

Information:

Total Files Size (in bytes):	564472
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

JASON D. EISENBERG
DIRECTOR
(202) 772-8645
JASONE@SKGF.COM



February 24, 2015

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Art Unit 2115
Attn: Mail Stop AF

Re: U.S. Reissue Patent Application
Appl. No. 13/902,227; Filing Date: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Reissue Application Declaration by the Assignee; and
2. Reply Under 37 C.F.R. § 1.116.

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/TMH/eet
Enclosures

1968365_1.DOCX

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE ASSIGNEE		Docket Number (optional) 3371.002RLE10	
I hereby declare that: The residence and mailing address of the inventor or joint inventors are stated below. I am authorized to act on behalf of the following assignee: <u>Memory Technologies LLC</u> The entire title to the patent identified below is vested in said assignee.			
Inventor <u>Kimmo MYLJY</u>			
Residence: City <u>Julkujärvi</u>	State	Country <u>Finland</u>	
Mailing Address			
City <u>Julkujäri</u>	State	Zip <u>FIN-39160</u>	Country <u>Finland</u>
<input type="checkbox"/> Additional inventors are named on separately numbered sheets attached hereto.			
Patent Number <u>7,278,033 B2</u>		Date of Patent Issued <u>October 2, 2007</u>	
I believe said inventor(s) to be the original inventor or original joint inventors of the subject matter which is described and claimed in said patent, for which a reissue patent is sought on the invention titled: <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device</div> the specification of which <input type="checkbox"/> is attached hereto. <input checked="" type="checkbox"/> was filed on <u>May 24, 2013</u> as reissue application number <u>13/902,227</u> . The above-identified application was made or authorized to be made by me. I hereby acknowledge that any willful false statement made in this declaration is punishable under 35 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.) <input type="checkbox"/> by reason of a defective specification or drawing. <input checked="" type="checkbox"/> by reason of the patentee claiming more or less than he had the right to claim in the patent. <input type="checkbox"/> by reason of other errors.			

[Page 1 of 2]

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

REISSUE APPLICATION DECLARATION BY THE ASSIGNEE		Docket Number (Optional) 3371.002RE10	
<p>At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified and the box below must be checked:</p> <p>Applicant seeks to clarify claim 28 by additionally reciting "wherein the means for setting the maximum power consumption of the peripheral device is configured to obtain the value, as indicated by the received information, and to set the maximum power consumption of the peripheral device to the value."</p> <p style="text-align: center;">[Attach additional sheets, if needed.]</p> <p><input type="checkbox"/> The application for the original patent was filed under 37 CFR 1.46 by the assignee of the entire interest.</p>			
I hereby appoint:			
<input checked="" type="checkbox"/> Practitioners associated with Customer Number:		26111	
OR			
<input type="checkbox"/> Practitioner(s) named below:			
Name		Registration Number	
as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.			
Correspondence Address: Direct all communications about the application to:			
<input checked="" type="checkbox"/> The address associated with Customer Number:		26111	
OR			
<input type="checkbox"/> Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		
WARNING:			
<p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p>			
Signature	<i>Robert Saltzberg</i>		Date (Optional) <i>2/17/15</i>
Full name of person signing (given name, family name) Robert Saltzberg			
Address of Assignee			
6787 W. Tropicana Ave., Suite 238 , Las Vegas, Nevada 89103, US			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/902,227	Filing Date 05/24/2013	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	02/24/2015	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	* 40	Minus	** 40	=	X \$ =
	Independent <small>(37 CFR 1.16(h))</small>	* 7	Minus	*** 7	=	X \$ =
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
					TOTAL ADD'L FEE	


	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	X \$ =
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	X \$ =
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
					TOTAL ADD'L FEE	

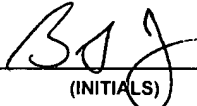
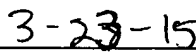
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ELMIRA HALL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Number 	Application No. 13/902,227	Applicant(s) Kimmo Mylly
	Notice of Reissue Published in OG on 10/22/13	
Original Patent Number of Patent To Be Reissued is 7278033		The Maintenance fee status is: <input checked="" type="checkbox"/> up to date. <input type="checkbox"/> not required.
This reissue patent is subject to A Terminal Disclaimer that: <input type="checkbox"/> was filed during the prosecution of the reissue application. <input type="checkbox"/> was of record prior to the filing of the reissue application.		
Physical surrender of the letters patent <input type="checkbox"/> was made. <input type="checkbox"/> was not made, but a statement of loss/inaccessibility was provided. <input checked="" type="checkbox"/> is not required		

Final SPRE Review  _____ (INITIALS)
 _____ (DATE)

U.S. Patent and Trademark Office



NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 04/02/2015
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Table with 2 columns: EXAMINER (BAE, JI H), ART UNIT (2115), PAPER NUMBER (8765)

DATE MAILED: 04/02/2015

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

TITLE OF INVENTION: Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

Table with 7 columns: APPLN. TYPE, ENTITY STATUS, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies. If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above. If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)". For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 04/02/2015
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
 1100 NEW YORK AVENUE, N.W.
 WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/902,227	05/24/2013	Kimmo MYLLY	3371.002REI0	8765

TITLE OF INVENTION: Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAE, JI H	2115	713-300000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, _____ 1</p> <p>(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. _____ 2</p> <p>_____ 3</p>
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : Individual Corporation or other private group entity Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
---	--

5. **Change in Entity Status** (from status indicated above)

Applicant certifying micro entity status. See 37 CFR 1.29

Applicant asserting small entity status. See 37 CFR 1.27

Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Values: 13/902,227, 05/24/2013, Kimmo MYLLY, 3371.002REI0, 8765

26111 7590 04/02/2015
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

BAE, JI H

ART UNIT PAPER NUMBER

2115

DATE MAILED: 04/02/2015

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/902,227	Applicant(s) MYLLY, KIMMO	
	Examiner JI H. BAE	Art Unit 2115	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to amendment filed on 2/24/2015.
 A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. The allowed claim(s) is/are 1-40. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/oph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some *c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 10/401338.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.


THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Examiner's Amendment/Comment |
| 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. <input type="checkbox"/> Other _____. |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ . | |

/JI H BAE/
Primary Examiner, Art Unit 2115

Index of Claims 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed


-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014	01/29/2015	02/28/2015				
	1	✓	=	✓	=				
	2	✓	=	✓	=				
	3	✓	=	✓	=				
	4	✓	=	✓	=				
	5	✓	=	✓	=				
	6	✓	=	✓	=				
	7	✓	=	✓	=				
	8	✓	=	✓	=				
	9	✓	=	✓	=				
	10	✓	=	✓	=				
	11	✓	=	✓	=				
	12	✓	✓	✓	=				
	13	✓	=	✓	=				
	14	✓	=	✓	=				
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	28	✓	✓	✓	=				
	29	✓	✓	✓	=				
	30	✓	✓	✓	=				
	31	✓	✓	✓	=				
	32	✓	✓	✓	=				
	33	✓	✓	✓	=				
	34	✓	✓	✓	=				
	35	✓	✓	✓	=				
	36	✓	✓	✓	=				

Index of Claims 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	01/25/2014	09/16/2014	01/29/2015	02/28/2015				
	37	✓	✓	✓	=				
	38		✓	✓	=				
	39		✓	✓	=				
	40		✓	✓	=				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	292	bae.xa.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2015/02/28 23:47
L2	19866	(713/300 713/320 713/322 710/8 710/301).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2015/02/28 23:48
L3	28458	(G06F1/26 OR G06F1/3206 OR G06F1/324 OR G06F1/266 OR G06F1/3275 OR G06F1/3225 OR G06F1/3253 OR G06F13/10 OR G06F13/38).CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2015/03/01 00:10


EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	19875	(713/300 713/320 713/322 710/8 710/301).ccls.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:10
L5	13527	(G06F1/26 OR G06F1/3206 OR G06F1/324 OR G06F1/266 OR G06F1/3275 OR G06F1/3225 OR G06F1/3253 OR G06F13/10 OR G06F13/38).CPC.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:11
L6	0	"means for setting the maximum power consumption".clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:11
L7	0	("maximum power consumption" with processor with indication with "received information").clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:11
L8	1	(maximum with "power consumption" with "default value" with "limiting value" with range).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:11
L9	0	("peripherhal device" with "power consumption" with "default value" with "limiting value").clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:11
L10	1	("peripheral device" with "power consumption" with "default value" with "limiting value").clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12
L11	0	("maximum power consumption" with range	US-	OR	OFF	2015/03/01

		with degault with "limiting value").clm.	PGPUB; USPAT; UPAD			00:12
L12	0	(information near3 transfer\$4 with "electronic device" with "periperhal device" with "maximum power consumption").clm.	US- PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12
L13	0	(information near3 transfer\$4 with "electronic device" with "periperhal device" with "maximum power consumption").clm.	US- PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12
L14	0	(message\$1 near3 transfer\$4 with "electronic device" with "periperhal device" with "maximum power consumption").clm.	US- PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12
L15	1	(memory with "power consumption" with "default value" with "limiting value").clm.	US- PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12
L16	2	("power consumption" with "startup stage" with "peripheral device" with "default value").clm.	US- PGPUB; USPAT; UPAD	OR	OFF	2015/03/01 00:12

3/ 1/ 2015 12:13:24 AM

C:\Users\jbae\Documents\EAST\Workspaces\13902227_reissue.wsp

Search Notes 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/26, 1/3206, 1/324, 1/266, 1/3275, 1/3225, 1/3253, 13/10, 13/38	3/1/2015	/jb/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300, 320, 322	1/25/2014	/jb/
710	8, 301	1/25/2014	/jb/

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name search	1/25/2014	/jb/
EAST text search (see attached search history)	1/25/2014	/jb/
EAST text search, incl. interferences (see attached search history)	3/1/2015	/jb/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	300, 320, 322	3/1/2015	/jb/
710	8, 301	3/1/2015	/jb/
G06F	1/26, 1/3206, 1/324, 1/266, 1/3275, 1/3225, 1/3253, 13/10, 13/38	3/1/2015	/jb/

	/JI H BAE/ Primary Examiner. Art Unit 2115
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kimmo MYLLY

Appl. No.: 13/902,227

Filed: May 24, 2013

For: **Method and a System for Determining
the Power Consumption in Connection
with an Electronic Device, and an
Electronic Device**

Confirmation No.: 8765

Art Unit: 2115

Examiner: Bae, JI H

Atty. Docket: 3371.002REI0

Reply Under 37 C.F.R. § 1.116

Mail Stop AF


Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated February 2, 2015, Applicant submits the following Remarks. No amendments are made in this Reply. All changes shown in the claims were previously submitted and entered by the Examiner, and are being shown herein pursuant to the Rules.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.


OK TO ENTER: /J.B./ (03/28/2015)

Issue Classification 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

CPC						
Symbol					Type	Version
G06F		1		266	F	2013-01-01
G06F		13		10	A	2013-01-01
G06F		1		3225	A	2013-01-01
G06F		1		324	A	2013-01-01
G06F		1		3275	A	2013-01-01
G06F		1		3253	I	2013-01-01
G06F		1		26	A	2013-01-01
G06F		13		38	I	2013-01-01
G06F		1		3206	A	2013-01-01

CPC Combination Sets							
Symbol				Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
		40	
(Assistant Examiner)	(Date)		
/JI H BAE/ Primary Examiner. Art Unit 2115	03/01/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	28	1

Issue Classification 	Application/Control No. 13902227	Applicant(s)/Patent Under Reexamination MYLLY, KIMMO
	Examiner JI H BAE	Art Unit 2115

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33										
	2		18		34										
	3		19		35										
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	14		30												
	15		31												
	16		32												

NONE		Total Claims Allowed:	
		40	
(Assistant Examiner)	(Date)	O.G. Print Claim(s)	O.G. Print Figure
/JI H BAE/ Primary Examiner. Art Unit 2115	03/01/2015	28	1
(Primary Examiner)	(Date)		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26131 25971 04612/2015
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
 1100 NEW YORK AVENUE, N.W.
 WASHINGTON, DC 20005

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/902,227	05/24/2013	Kimmo MYLLY	3371.002RE310	8765

TITLE OF INVENTION: Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device

APPL. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEES DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAE, H H	2115	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

Change of correspondence address (for Change of Correspondence Address form PTO/SB/122) attached.

"Fee Address" indication (for "Fee Address" indication form PTO/SB/47, Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Sterne, Kessler, Goldstein & Fox P.L.L.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **Memory Technologies LLC**

(B) RESIDENCE: (CITY and STATE OR COUNTRY) **Las Vegas, NV**

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:

Issue Fee

Publication Fee (No small entity discount permitted)

Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

A check is enclosed.

Payment by credit card. Form PTO-2038 is attached.

The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number **19-0036** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

Applicant certifying micro entity status. See 37 CFR 1.29

Applicant asserting small entity status. See 37 CFR 1.37

Applicant changing to regular undiscouted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature **Jason D. Eisenberg #43447/** Date **April 3, 2015**

Typed or printed name **Jason D. Eisenberg** Registration No. **43,447**

Electronic Patent Application Fee Transmittal

Application Number:	13902227			
Filing Date:	24-May-2013			
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device			
First Named Inventor/Applicant Name:	Kimmo MYLLY			
Filer:	Jason Daniel Eisenberg/LaTishia Tillman			
Attorney Docket Number:	3371.002REI0			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	21968083
Application Number:	13902227
International Application Number:	
Confirmation Number:	8765
Title of Invention:	Method and a System for Determining the Power Consumption in Connection with an Electronic Device, and an Electronic Device
First Named Inventor/Applicant Name:	Kimmo MYLLY
Customer Number:	26111
Filer:	Jason Daniel Eisenberg/LaTishia Tillman
Filer Authorized By:	Jason Daniel Eisenberg
Attorney Docket Number:	3371.002REI0
Receipt Date:	03-APR-2015
Filing Date:	24-MAY-2013
Time Stamp:	16:19:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	2262
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	3371002REI0SKGFCVRIssueFee.pdf	183343 e57357a2e9cb4734da4a22e1dcf7f6f850dcd13	no	1

Warnings:

Information:

2	Issue Fee Payment (PTO-85B)	3371002REI0IssueFeeTransmittal.pdf	553495 3cdd67051159fb091949cd54cf3d77e5a4a76174	no	1
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Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	32354 517fce2fb93aa42154c967c021fc9b3dc29164f	no	2
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Warnings:

Information:

Total Files Size (in bytes):			769192		
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

JASON D. EISENBERG
DIRECTOR
(202) 772-8645
JASONE@SKGF.COM



April 3, 2015

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 8765
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 13/902,227; Filed: May 24, 2013
For: **Method and a System for Determining the Power Consumption in
Connection with an Electronic Device, and an Electronic Device**
Inventor: Kimmo MYLLY
Our Ref: 3371.002REI0

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated April 2, 2015, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for \$960.00 to cover:
\$960.00 - Issue Fee; and
2. Issue Fee Transmittal (Form PTOL-85).

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Jason D. Eisenberg #43447/

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/lam
Enclosures
1985812_1



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/902,227	06/02/2015	RE45542	3371.002RE10	8765

26111 7590 05/13/2015
 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
 1100 NEW YORK AVENUE, N.W.
 WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Memory Technologies LLC, Las Vegas, NV, Assignee (with 37 CFR 1.172 Interest);
 Kimmo MYLLY, Julkujarvi, FINLAND;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.