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Garner

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[54] **METHOD AND APPARATUS FOR MANAGING ACTIVE POWER CONSUMPTION IN A MICROPROCESSOR CONTROLLED STORAGE DEVICE**

[75] Inventor: **Richard P. Garner**, Cameron Park, Calif.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **760,325**

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Related U.S. Application Data

[63] Continuation of Ser. No. 414,190, Mar. 31, 1995, abandoned.

[51] **Int. Cl.**[6] **G06F 1/32**

[52] **U.S. Cl.** **395/750.04**; 395/430; 395/494

[58] **Field of Search** 395/750, 430, 395/494; 364/707

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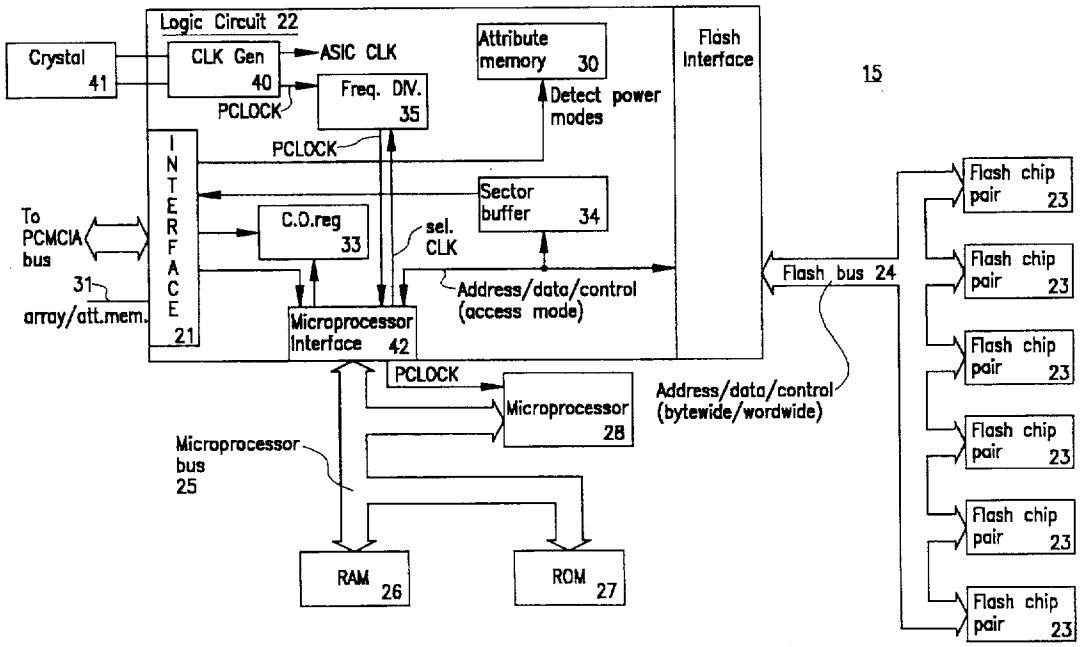
Primary Examiner—Jack B. Harvey
Assistant Examiner—Jeffrey K. Seto
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A flash electrically-erasable programmable read only memory (EEPROM) array and a method for allowing a host computer to detect a plurality of different power-expending modes into which a storage device may be placed for operation, to select a particular one of those modes to match the power abilities of the host computer, and then to place the storage device in the proper power mode of operation to best function with the host system.

23 Claims, 3 Drawing Sheets



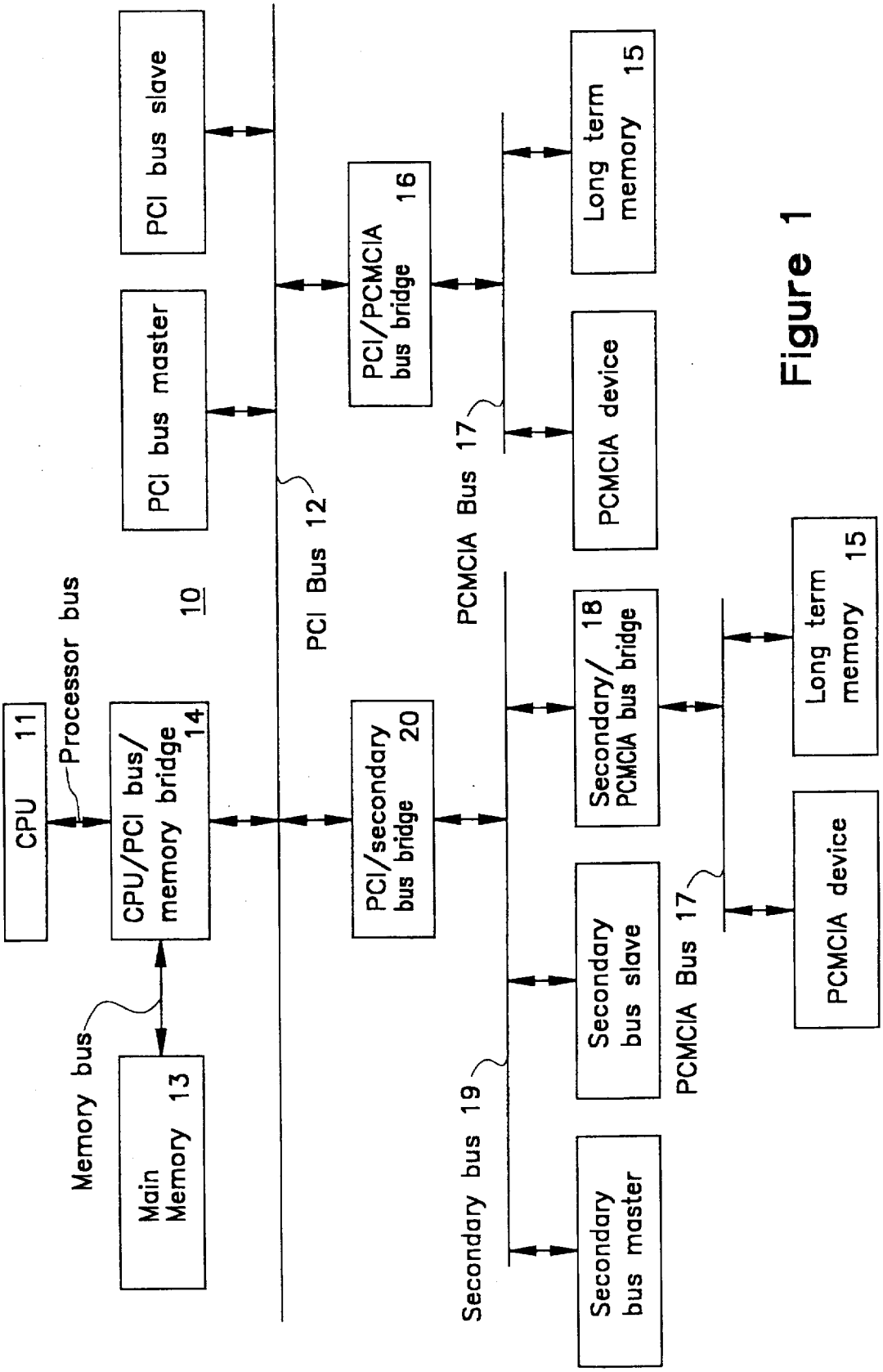


Figure 1

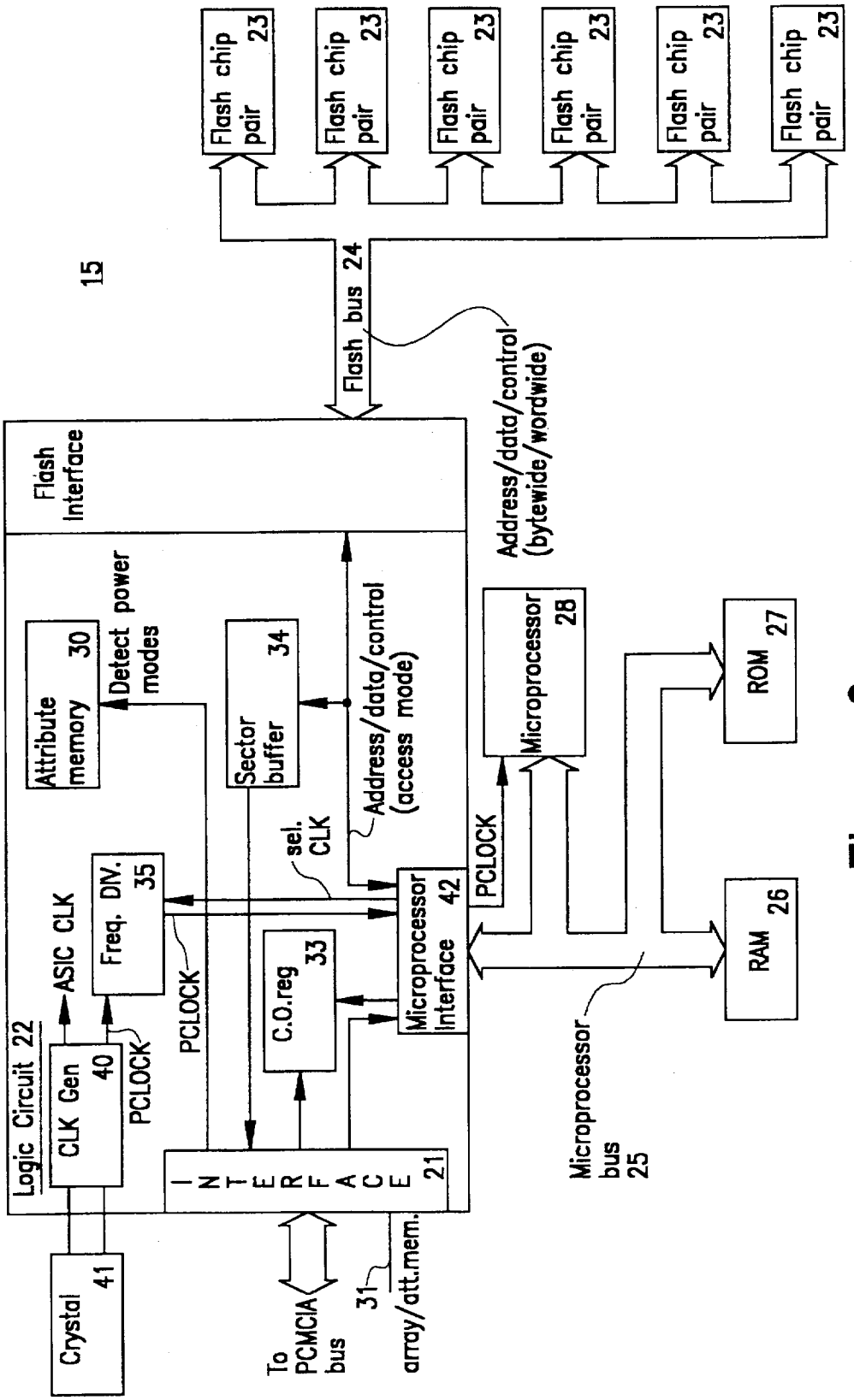


Figure 2

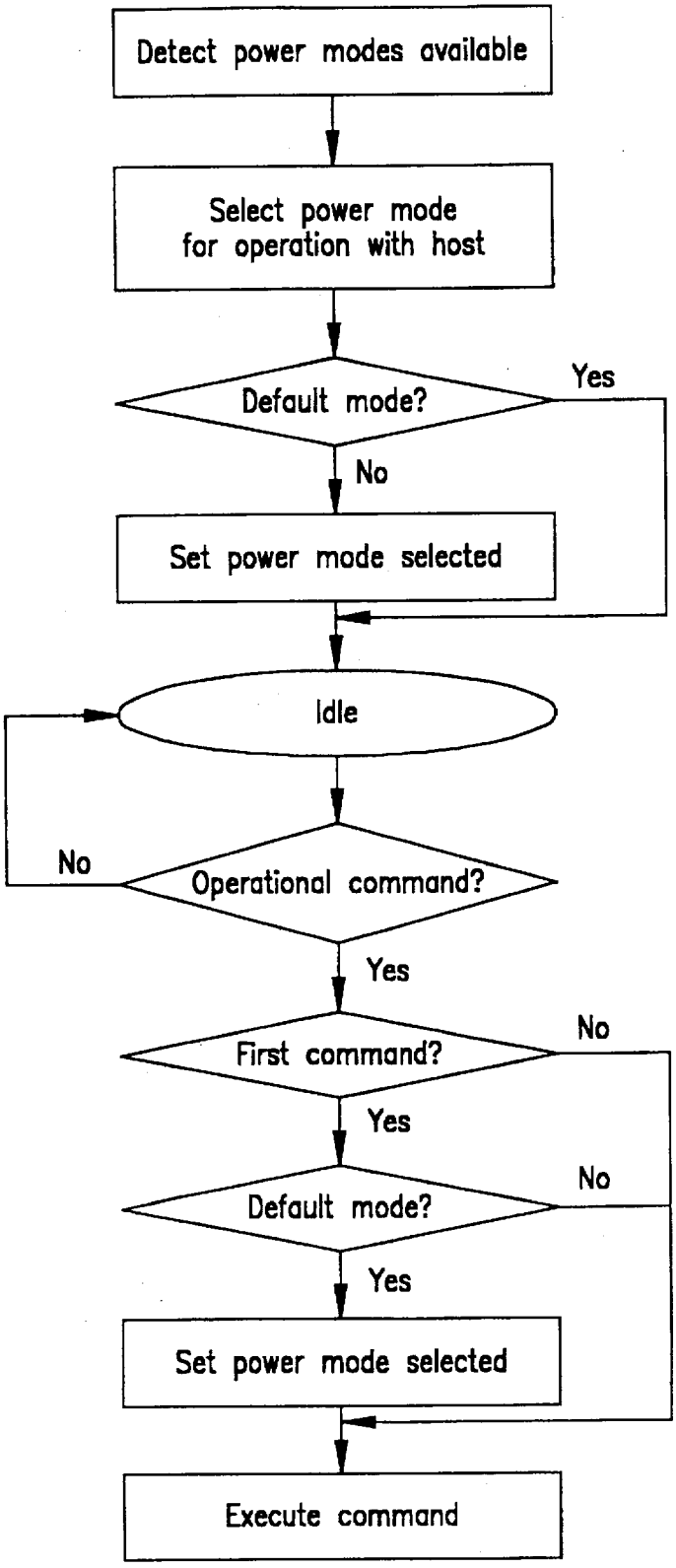


Figure 3

METHOD AND APPARATUS FOR MANAGING ACTIVE POWER CONSUMPTION IN A MICROPROCESSOR CONTROLLED STORAGE DEVICE

This is a continuation of application Ser. No. 08/414,190, filed Mar. 31, 1995, now abandoned.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

This invention relates to microprocessor controlled storage devices such as flash EEPROM memory arrays, and more particularly, to methods and apparatus for managing power consumption in such storage devices.

2. History Of The Prior Art

Recently, microprocessor controlled storage devices such as flash EEPROM memory arrays have been used as a new form of long term storage. A flash EEPROM memory array is constructed of a large plurality of floating-gate metal-oxide-silicon field effect transistor devices arranged as memory cells in typical row and column fashion with circuitry for accessing individual cells and placing the memory transistors of those cells in different memory conditions. Such memory transistors may be programmed by storing a charge on the floating gate. This charge remains when power is removed from the array. The charge level may be detected by interrogating the devices. These arrays may be designed to provide a smaller lighter functional equivalent of a hard disk drive which operates more rapidly and is not as sensitive to physical damage. Flash EEPROM memory arrays are especially useful in portable computers where space is at a premium and weight is extremely important.

In order to allow flash EEPROM memory arrays to accomplish the storage functions normally accomplished by electro-mechanical hard disk drives, one type of flash memory manufactured by Intel Corporation of Santa Clara, Calif., includes a microprocessor which controls many of the functions of the storage device such as loading commands and data which are used by the storage device for accomplishing various housekeeping, setup, and other functions. The same storage device also includes hardware apart from the microprocessor which is especially designed to respond to the commands and utilize the data to accomplish the various read, write, and erase functions necessary to the storage of data in the memory array. Power must be supplied for operating all of these components.

Although these memory arrays were initially designed for use in portable computers, their desirable characteristics has allowed their use to expand into other forms of digital devices such a desktop computers and personal digital assistants (PDAs). To a great extent, this expansion has occurred along with the expansion of the PCMCIA bus into these other forms of digital devices. One problem created by this expansion has been that the sources of power available in these different uses vary widely. Thus, with PDAs and very small portable computers, a few double A batteries may supply the power; while desktop computers may provide very large amounts of power.

It is desirable to allow any storage device designed for portable, PCMCIA, or removable use to function with as many different types of digital systems as possible. However, in order to accomplish this, it is necessary that the storage device be capable of utilizing as little power as possible when functioning with low powered systems. To accomplish this, it is desirable to allow such storage devices to function at the lowest level of power possible.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide apparatus and a method for managing the power used by microprocessor controlled storage devices so that the storage device may be used in a plurality of different digital systems.

It is another object of the present invention to reduce automatically the power used by components of flash EEPROM memory arrays to a level compatible with a particular host system.

These and other objects of the present invention are realized in a flash EEPROM memory array by circuitry and a method for allowing a host computer to detect a plurality of different power-expending modes into which a storage device may be placed for operation, to select a particular one of those modes to match the power abilities of the host computer, and then to place the storage device in the proper power mode of operation to best function with the host system.

These and other objects and features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a computer system which may utilize the present invention.

FIG. **2** is a block diagram of a flash EEPROM memory array constructed in accordance with the present invention.

FIG. **3** is a flow chart describing the operation of a portion of the memory array in carrying out the present invention.

NOTATION AND NOMENCLATURE

Some portions of the detailed descriptions which follow are presented in terms of symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. The operations are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary or desirable in most cases in any of the operations described herein which form part of the present invention; the operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases the distinction between the method operations in operating a computer and the method of computation itself should be borne in mind. The present invention relates to a method and apparatus for operating a computer in processing electrical or other (e.g. mechanical, chemical) physical signals to generate other desired physical signals.

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