United States Patent [19]

Shimoda et al.

[54] VITERBI EQUALIZER AND RECORDING/REPRODUCING DEVICE USING THE SAME

- [75] Inventors: Kaneyasu Shimoda; Hideto Furukawa, both of Kawasaki, Japan
- [73] Assignee: Fujitsu Limited, Kawasaki, Japan
- [21] Appl. No.: 705,065

[56]

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[22] Filed: May 23, 1991

[30] Foreign Application Priority Data

- May 25, 1990 [JP] Japan 2-136226
- [51] Int. Cl.⁵ G06F 11/10

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[11] Patent Number: 5,341,386

[45] Date of Patent: Aug. 23, 1994

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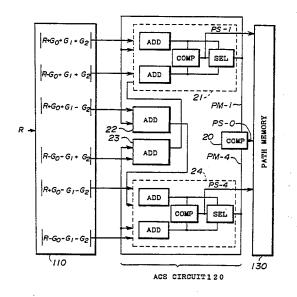
Primary Examiner—Robert W. Beausoliel, Jr. Assistant Examiner—Joseph E. Palys Attorney, Agent, or Firm—Staas & Halsey

[57] ABSTRACT

A viterbi equalizer includes a distributor for receiving a run length limited code and for calculating branch metrics responsive to the run length limited code. The branch metrics are related to only nodes and branches in a trellis state transition diagram based on a viterbi decoding algorithm defined for the run length limited code. The viterbi equalizer also includes a path metric calculating circuit, operatively coupled to the distributor, for generating path metrics on the basis of the branch metrics and for generating path select signals indicative of surviving paths coupling the nodes and branches. Further, the viterbi equalizer includes a path memory, operatively coupled to the path metric calculating circuit, for determining a maximum likelihood path on the basis of the path select signals output by the path metric calculating circuit.

10 Claims, 12 Drawing Sheets

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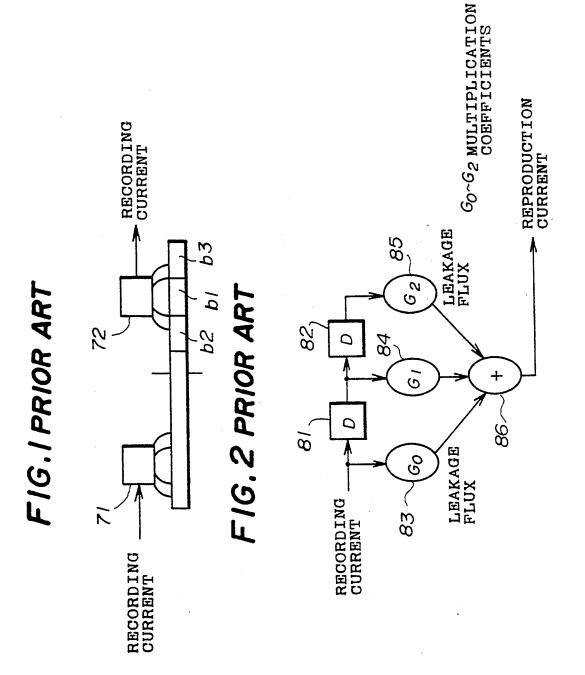


FIG.3 PRIOR ART

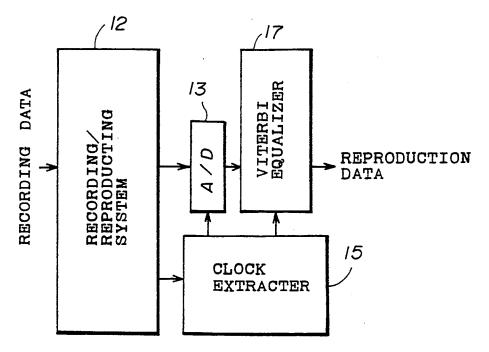
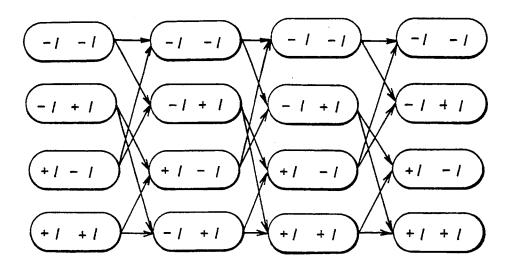
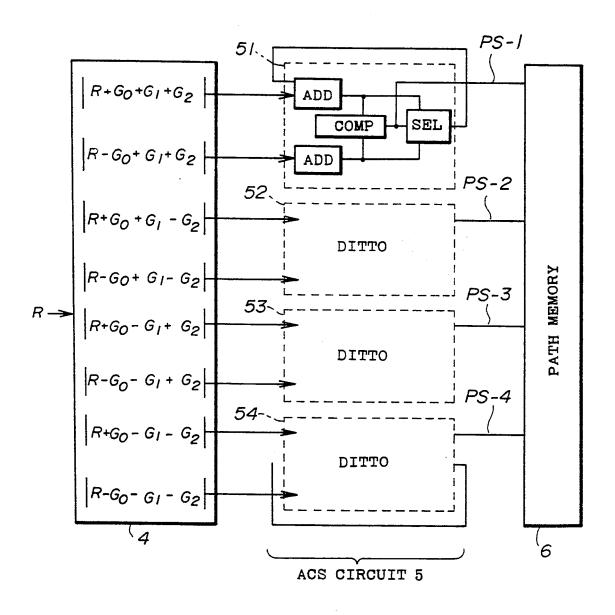


FIG.4 PRIOR ART



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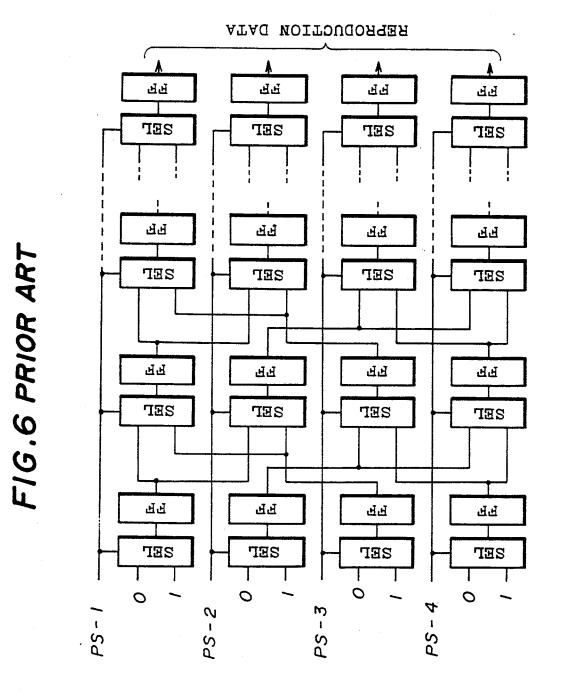
FIG.5 PRIOR ART



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