demonstrated to consist of write patterns that contain three or more unspaced consecutive transitions. A class of block codes that limits the number of consecutive symbol transitions, typically representing binary "1's", are known as maximum transition run (MTR) codes. To avoid three or more consecutive transitions, codes with MTR values (no more than two successive binary "1's" in the coding result) equal to two are desirable.

(*Id.* at 2:14-27.) Both embodiments of Tsang involve a MTR value of 2, and thereby "limits the number of consecutive symbol transitions" and eliminates the "most likely error sequence" in recorded data. (*See id.*) Tsang therefore discloses facilitation of "the reduction of a probability of a detection error" in the receiver means, as recited in claim 1 [D].

141.　Tsang also claims "an encoder coupled to said encoding receiver for providing a corresponding said code block for each said data block," such that "each said code block and any concatenations of said code blocks are without more than a preselected first symbol number of successive repetitions of a first symbol throughout, and without more than a preselected second symbol number of successive repetitions of a second symbol throughout." (Ex. 1009 at 19:41-57) (claim 1). Claim 2 recites the apparatus of claim 1 wherein "said first symbol is a '0' and said second is a '1.'" (*Id.*, 19:58-60.) Claim 3 recites the apparatus of claim 1 wherein "said first symbol number equals nine," *i.e.*, k = 9. (*Id.*, 19:61-

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62.) Claim 4 recites the apparatus of claim 1 wherein "said second symbol number equals two," *i.e.*, j = 2. (*Id.*, 19:63-64.)

142. Thus, Tsang discloses claim limitation 1 [D]

5. Claim 1[E]: "said sequences generating no more than j consecutive transitions in the recorded waveform such that j is an integer equal to or greater than 2; and"

143. As discussed above with respect to claim 1 [D], Tsang discloses apparatuses having an MTR ("j") value of 2. As also discussed above with respect to claim 1 [D], Claim 4 of Tsang specifically claims j = 2. A value of j=2 ensures that the recorded waveform "avoid[s] three or more consecutive transitions." (Ex. 1009 at 2:25-28. Tsang thus discloses claim element 1 [E].

6. Claim 1[F]: "said sequences generating no more than k consecutive sample periods without a transition in the recorded waveform."

144. As discussed above with respect to claim element 1 [D], Tsang discloses apparatuses having a constraint k of 9, which ensures generation of no more than 9 consecutive sample periods without a transition in the recorded waveform. (*See* Ex. 1009 at 2:3-5; 5:25-39) And as also discussed above with respect to claim element 1 [D], claim 3 of Tsang specifically claims k = 9. Tsang thus discloses claim element 1 [F].

B. Claim 2 is anticipated by Tsang

145. Claim 2 recites "Apparatus as in claim 1 wherein the j consecutive transition limit is defined by the relationship $2 \leq j < 10$."

146. As shown above, Tsang anticipates claim 1 from which claim 2 depends. As to the additional limitation of claim 2, Tsang discloses and claims apparatuses and methods wherein $j = 2$. (*See* the discussion of claims 1 [D] and 1 [E], *supra*.) Tsang thus anticipates claim 2.

C. Claim 8 is anticipated by Tsang

147. Claim 8 recites "Apparatus as in claim 2 wherein the consecutive transition limit is defined by the relationship j=2."

148. As shown above, Tsang anticipates claims 1 and 2 from which claim 8 depends. As to the additional limitation of claim 8, Tsang discloses and claims apparatuses and methods wherein $j = 2$. (*See* the discussion of claims 1 [D] and 1 [E], *supra*.) Tsang thus anticipates claim 8.

D. Claim 9 is anticipated by Tsang

149. Claim 9 recites "Apparatus as in claim 2 wherein the binary sequences produced by combining codewords have no more than j consecutive 1's and no more than k consecutive 0's when used with a NRZI recording format."

150. As shown above, Tsang anticipates claim 1 from which claims 2 and 9 depend. As to the additional limitation of claim 9, Tsang discloses and claims

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that, after NRZI modulation, (*see* Ex. 1009 at 1:5-41; 2:22-25), where j=2, "invalid patterns (three or more consecutive 1's) do not occur when these code words are concatentated." (*E.g.,* Ex. 1009 at 4:3-13.) Further "the '0's' run length 'k' constraint" = 9, and therefore no more than 9 consecutive zeros are found. (Ex. 1009 at 5:25-39.) (*See* the discussion of claims 1 [D], 1 [E], and 1 [F], supra.)

151. Tsang thus anticipates claim 9.

E. Claim 10 is anticipated by Tsang

152. Claim 10 recites "Apparatus as in claim 2 wherein binary sequences produced by combining codewords have no more than one of j consecutive transitions from 0 to 1 and from 1 to 0 and no more than k+1 consecutive 0's and k+1 consecutive 1's when used in conjunction with a NRZ recording format."

153. As shown above, Tsang anticipates claims 1 and 2 from which claim 10 depends. In particular, Tsang discloses and claims that the binary sequences produced by combining codewords, after NRZI modulation, have no more than 2 consecutive 1's and no more than 9 consecutive 0's, *i.e.*, j = 2 and k = 9. (*See* the discussion of claims 1 [D], 1 [E], and 1 [F], *supra*.)

154. As to the additional limitations of claim 10, Okada discloses no more than one of 2 consecutive transitions from 0 to 1 and from 1 to 0 in NRZ format. In particular, Figure 3 shows the code word assignment and next state table for a 5/6 rate MTR code having j = 2 and k = 9 constraints. (Ex. 1009 at 3:44-46). The

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32 rows of codewords in Figure 3 are shown in NRZI format. (Ex. 1009 at 1:5-26, 4:3-18.) As can be observed, each such codeword has at most two consecutive 1's in a row. A sequence "11" in NRZI results from NRZ strings of "0101" or "1010," *i.e.*, one of 2 consecutive transitions from 0 to 1 and from 1 to 0 in NRZ format, as claimed. Figure 3 shows two columns of codewords for each data word, corresponding to "State 0" and "State 1." Tsang uses a "two-state trellis diagram" which ensures that the MTR $j = 2$ constraint is satisfied across codeword boundaries. (Ex. 1009 at 4:3-18; Ex.) (Figure 8 is similar to Figure 3, but corresponds to a second embodiment having a 6/7 rate MTR code having $j = 2$ and $k = 9$ constraints.) As stated in the '601 Patent, k consecutive 0's in *NRZI* format is equivalent to no more than $k + 1$ consecutive 0's and $k + 1$ consecutive 1's, in *NRZ* format. (Ex. 1001 at 1:15-36.)

155. Tsang thus anticipates claim 10.

F. **Claim 13 is anticipated by Tsang**

1. **Claim 13[A]: "A method for encoding m-bit binary datawords into n-bit binary codewords in a recorded waveform, where m and n are preselected positive integers such that n is greater than m, comprising the steps of:"**

156. Claim 13 is highly similar to claim 1, but claim 13 recites a "method" while claim 1 recites an "apparatus."

157. As informed by counsel, the preamble of the claim may not be limiting. Alternatively, if the preamble is found to be limiting, as shown above,

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Tsang discloses and claims apparatuses and methods for encoding m-bit binary datawords into n-bit binary codewords, in a recorded waveform, wherein m is greater than n. (*See* the discussion of claim 1 [A], *supra*.)

158. Tsang thus discloses and claim element 13 [A].

2. Claim 13[B]: "receiving binary datawords; and"

159. As explained above with respect to claim element 1 [B], Tsang discloses a first embodiment, depicted in Figure 4A, wherein datawords (11) are received by a "data word receiver" consisting of a 5-bit register (10), and a second embodiment, depicted in Figure 9A, wherein datawords (61) are received by a 6-bit register (60). Tsang thus discloses and claims claim 13 [B].

3. Claim 13[C]: "producing sequences of n-bit codewords;"

160. As explained above with respect to claim element 1 [C], Tsang discloses a first embodiment wherein an encoder (15) is coupled to a receiver means (10) for producing sequences of 6-bit codewords. (Ex. 1009, Figure 4A; 6:5-28.) In a second embodiment, Tsang discloses an encoder (65) coupled to a receiver means (60) for producing sequences of 7-bit codewords. (*Id.*, Figure 9A; 11:43-56.) Thus, Tsang discloses claim element 13 [C].

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4. **Claim 13[D]: "imposing a pair of constraints (j;k) on the encoded waveform;"**

161. As explained above with respect to claim elements 1 [D], [E], and [F], Tsang discloses and claims MTR constraints $j = 2$ and $k = 9$. Thus, Tsang discloses claim element 13 [D].

5. **Claim 13[E]: "generating no more than j consecutive transitions of said sequence in the recorded waveform such that $j \geq 2$; and"**

162. As explained above with respect to claim elements 1 [E], Tsang discloses and claims MTR constraints $j = 2$, resulting in generation of not more than 2 consecutive transitions. Thus, Tsang discloses claim element 13 [E].

6. **Claim 13[F]: "generating no more than k consecutive sample periods of said sequences without a transition in the recorded waveform."**

163. As discussed above with respect to claim element 1 [F], Tsang discloses and claims MTR constraint $k = 9$, ensuring no more than 9 consecutive sample periods without a transition in the recorded waveform. Thus, Tsang discloses and claims claim 13 [F].

G. Claim 14 is anticipated by Tsang

164. Claim 14 recites "The method as in claim 13 wherein the consecutive transition limit is defined by the relationship $2 \leq j < 10$."

165. As explained previously, Tsang anticipates claim 13 from which claim 14 depends. As to the additional limitations of claim 14, as explained above with

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respect to claim 2, Tsang discloses and claims apparatuses and methods wherein j = 2. Tsang thus anticipates claim 14.

H.   Claim 15 is anticipated by Tsang

166.   Claim 15 recites "The method as in claim 14 wherein the consecutive transition limit is j=2."

167.   As discussed previously, Tsang anticipates claims 13 and 14 from which claim 15 depends. As to the additional limitation of claim 15, as shown above with respect to apparatus claim 2, Tsang discloses and claims apparatuses and methods wherein j = 2. Tsang thus anticipates claim 15.

I.   Claim 16 is anticipated by Tsang

168.   Claim 16 recites the "method as in claim 14 wherein the binary sequences produced by combining codewords have no more than j consecutive 1's and no more than k consecutive 0's when used with the NRZI recording format."

169.   As explained previously, Tsang anticipates claim 14 from which claim 16 depends. As to the additional limitations of claim 16, Tsang discloses and claims that the binary sequences produced by combining the disclosed 6- and 7-bit codewords, after NRZI modulation, have no more than 2 consecutive 1's and no more than 9 consecutive 0's, *i.e.*, j = 2, k = 9 . (*See* the discussion of claims 1 [D], 1 [E], and 1 [F], *supra*.) Tsang thus anticipates claim 16.

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J.   Claim 17 is anticipated by Tsang

170.   Claim 17 recites "The method as in claim 14 wherein the binary sequences produced by combining codewords have no more than one of j consecutive transitions from 0 to 1 and from 1 to 0 and no more than one of k+1 consecutive 0's and k+1 consecutive 1's when used in conjunction with the NRZ recording format."

171.   As discussed previously, Tsang anticipates claims 14 from which claim 17 depends. In addition, for the reasons discussed previously with respect to claim 10, Tsang discloses that the binary sequences produced by combining codewords have no more than one of j consecutive transitions from 0 to 1 and from 1 to 0 and no more than one of k+1 consecutive 0's and k+1 consecutive 1's when used in conjunction with the NRZ recording format.

172.   Tsang thus anticipates claim 17.

**IX.   CLAIMS 12 AND 21 ARE OBVIOUS OVER OKADA IN VIEW OF SHIMODA**

A.   Claim 12 is obvious over Okada in view of Shimoda

173.   Claim 12 recites "Apparatus as in claim 2 wherein the receiver means incorporates means for removing certain code-violating patterns from the detection process wherein the detection process comprises *at least one of* the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis ..." [Emphasis added.]

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174. As shown above, Okada teaches all of the limitations recited in claims 1 and 2, from which claim 12 depends. (*See* the discussion of Okada with respect to anticipation of claims 1 and 2, *supra*.) Okada teaches a 8-to-13 block encoder, but does not disclose "means for removing certain code-violating patterns from the detection process" wherein the detection process comprises "removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis."

175. Shimoda discloses an apparatus and method for encoding binary data into codewords using an RLL code (as opposed to MTR code). The apparatus and method comprises an encoder (101), a recording/reproducing system (102), a Viterbi equalizer (103), and a decoder (104), as depicted in Figures 7 and 8:

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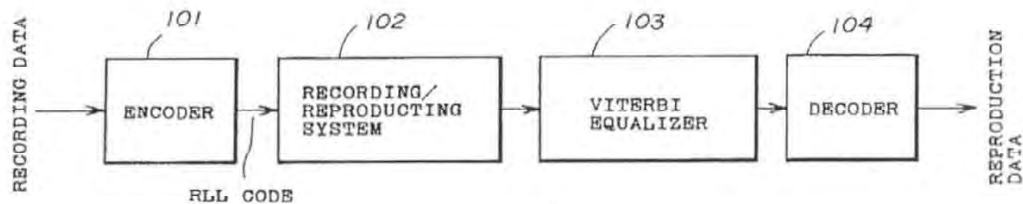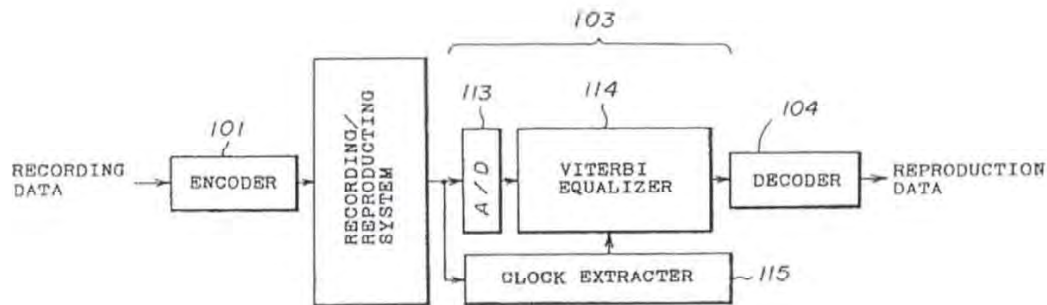
(Ex. 1008, Figs. 7 and 8, respectively.)

176.   The encoder (101) encodes recording data into run length limited ("RLL") code data. (Ex. 1008, 4:13-27.) The recording/reproducing system (102) records the RLL code data on a recording medium, such as a magnetic disk, and reproduces the RLL code data from the recording medium. The Viterbi equalizer (103) equalizes the RLL code data read out from the recording medium. The decoder (104) decodes equalized RLL code data output by the Viterbi equalizer 103, and generates reproduction data. (*See id.*)

177.   The Viterbi equalizer eliminates the intersymbol interference which takes place in the recording/reproducing system (102). (Ex. 1008, 4:28-40). "A viterbi decoding algorithm designed for use with an RLL code does not particular have state transitions inherent in the RLL code." (*Id.*) " In other words, there are state transitions which do not take place due to the rule of the RLL code." Thus, "a maximum likelihood path determination circuit provided in the viterbi equalizer ...

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does not have any structural elements related to the state transitions which do not

take place due to the rule of the RLL code." (*Id.*)

178. In one embodiment, Shimoda discloses an RLL (1,7) code generated

in accordance with the following rules:

BASIC TRANSFORM	
DATA	CODE WORD
00	101
01	100
10	001
11	010

EXCEPTION		
DATA	CODE WORD BASED ON BASIC TRANSFORM	CORRECTED CODE WORD
0000	101101	101000
0001	101100	100000
1000	001101	001000
1001	001100	010000

(Ex. 1008, 4:65-5:31). Shimoda discloses "the trellis state transition diagram of

the Viterbi equalizer (114)" in Figure 9, (*id.*), which is reproduced below:

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RLL (1, 7), 3 TAPS
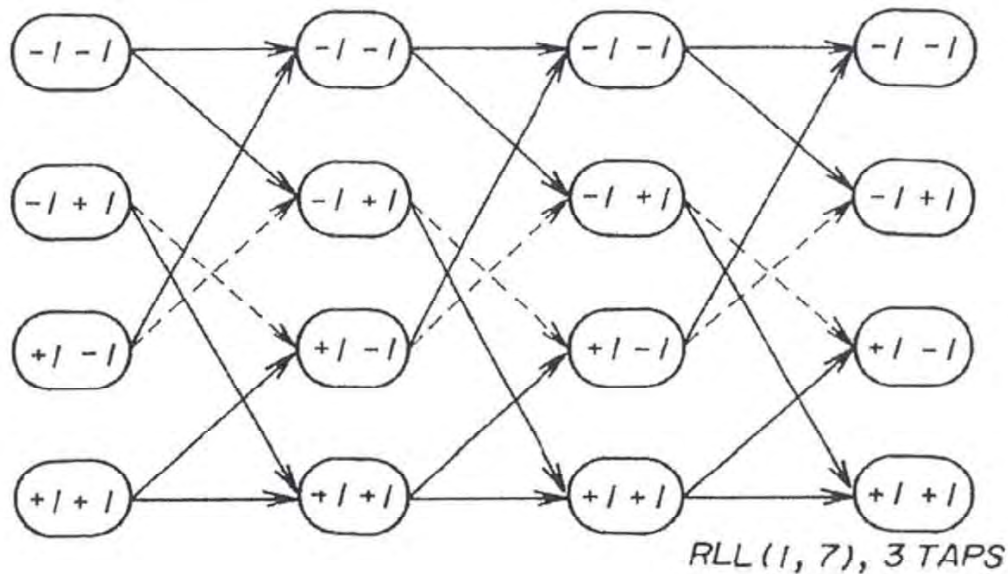
(Ex. 1008, Fig. 9.) "In FIG. 9, it is assumed that the directions of the write current (recording data) are defined as +1 and -1. In this case, a time series of the write current encoded into the (1,7) code does not have two transitions (+1, -1, +1) and (-1, +1, -1)." (*Id.*, 5:23-30). "Thus, *state transitions indicated by broken lines shown in FIG. 9 do not take place in the viterbi equalizer 114* which uses the RLL (1,7) code." (*Id.*) (emphasis added). As discussed above in Section III(E), the term "means for removing certain code-violating patterns" reads on a Viterbi trellis corresponding to a detection system, or its equivalents. Shimoda, in Figure 9, discloses this structure.

179. In another embodiment, Shimoda discloses an RLL (2,7) code generated in accordance with the following rules:

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DATA	CODE WORD
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

(Ex. 1008 at 6:52-7:8.) In this embodiment, a time series of the write data "does

not have state transitions of (+1, -1, +1), (-1, +1, -1), (+1, -1, -1, +1) and (-1, +1,

+1, -1)." (*Id.*, 7:1-8). "Thus, *there are not state transitions indicated by broken*

lines shown in FIG. 12, and it is not necessary for the viterbi equalizer 114 to

have circuits related to such state transitions which do not take place at all." (*Id.*)

(emphasis added). Figure 12 is reproduced below:

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RLL(2,7), 4 TAPS
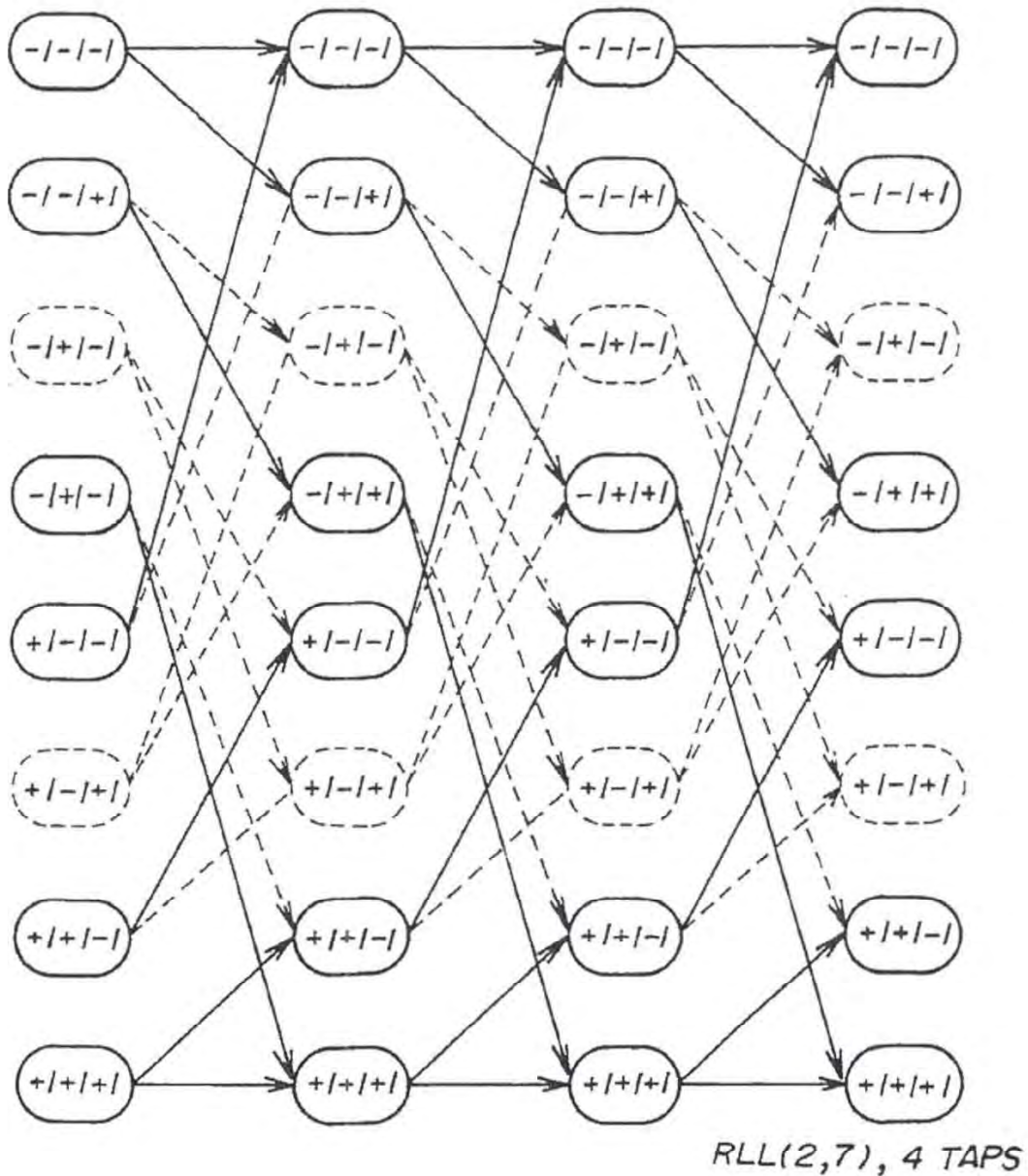
(Ex. 1008, Fig. 12.) Shimoda, in Figure 12, therefore discloses an additional

Viterbi trellis corresponding to a detection system, which corresponds to the claim

term "means for removing certain code-violating patterns."

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180.   Shimoda therefore discloses apparatuses and methods "wherein the receiver means incorporates means for removing certain code-violating patterns from the detection process wherein the detection process comprises" a step of "removing states and state transitions corresponding to" transitions that violate RLL (d,k) codes "from a Viterbi trellis."

181.   It would have been obvious for a person having ordinary skill in the art at the time of the alleged invention to combine the teachings of Okada and Shimoda to arrive at the alleged invention recited in claim 12. Both references address issues with data storage and associated apparatus and methods to reduce errors. (Ex. 1007 at abstract; Ex. 1008 at abstract.) A person of ordinary skill naturally would have been motivated to include with the 8-to-13 bit block encoder of Okada a Viterbi trellis corresponding to a "maximum likelihood path" detection system, as taught by Shimoda, because Okada is sub-optimal and it was well-known that the purpose of "maximum likelihood path detection" systems is to lower the bit error rate in an optimal manner. A maximum likelihood path detection system computes the most probable input resulting in an observed output. One of ordinary skill would have thus been motivated to further minimize the bit error rate by optimizing the apparatus described in Okada using the Viterbi trellis of Shimoda. Further, adapting the recording apparatus of Okada in this way in view of Shimoda was well within the ability of one of ordinary skill in the art at the

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time. Indeed, removing states and state transitions corresponding to code violating patterns from a Viterbi trellis is a routine function, well-known and easily employed by graduate students in the field. Moreover, doing so would have produced the predictable (and desirable) result of a lower bit error rate.

182. Further, a person of ordinary skill would have been motivated to include in the detection process a step of removing states and state transitions corresponding to more than j consecutive transitions from the Viterbi trellis, as taught by Shimoda, because then the device does not need to "have any structural elements related to the state transitions which do not take place due to the rule" of the MTR code, (Ex. 1008 at 4:28-40), making the device more "compact" and "less expensive." (*Id.* at 2:64-65.)

183. Claim 12 is therefore obvious over Okada in view of Shimoda.

B. Claim 21 is obvious over Okada in view of Shimoda.

184. Claim 21 recites "The method as in claim 13 wherein the method of receiving data incorporates the removal of certain code-violating patterns from the detection process wherein the detection process comprises *at least one* of the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis …" [Emphasis added.]

185. As shown above in the Section discussing Okada's anticipation of certain claims, Okada teaches all of the limitations recited in claim 13 from which

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claim 21 depends. Further, "method" claim 21 is similar to "apparatus" claim 12.

As shown above, claim 12 is obvious over Okada in view of Shimoda. Claim 21 is

obvious for the same reasons.

186. Again, Okada teaches a 8-to-13 block encoder, but does not disclose

"the removal of certain code-violating patterns from the detection process"

wherein the detection process comprises "removing states and state transitions

corresponding to more than j consecutive transitions from a Viterbi trellis." As

shown above with respect to claim 12, Shimoda teaches a Viterbi trellis

corresponding to a maximum likelihood path detection system, wherein RLL code

violating states and states transitions are removed from the detection process. For

the same reasons discussed with respect to claim 12, it would have been obvious

for a person having ordinary skill in the art at the time of the alleged invention to

combine the teachings of Okada and Shimoda to arrive at the alleged invention

recited in claim 21.

187. Claim 21 is therefore obvious over Okada in view of Shimoda, for the

same reasons that claim 12 is obvious over Okada in view of Shimoda

X.   CLAIMS 12 AND 21 ARE OBVIOUS OVER TSANG IN VIEW OF SHIMODA

A.   Claim 12 is obvious over Tsang in view of Shimoda

188. Claim 12 recites "Apparatus as in claim 2 wherein the receiver means

incorporates means for removing certain code-violating patterns from the detection

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process wherein the detection process comprises *at least one of* the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis ..." [Emphasis added.]

189.   As shown above, Tsang teaches all of the limitations recited in claims 1 and 2, from which claim 12 depends. (*See* the discussion of Tsang's anticipation of claims 1 and 2, *supra*.) In particular, Tsang discloses and claims rate 5/6 and rate 6/7 encoders, each having MTR constraints of j = 2 and k = 9. Tsang teaches the use of a "trellis diagram in such a manner that invalid patterns (three or more consecutive 1's) do not occur when ... code words are concatenated." (Ex. 1009 at 4:3-19; *see id*. at 10:17-11:57.)

190.   To the extent it is found, however, that Tsang does not disclose "means for removing certain code-violating patterns from the detection process wherein the detection process comprises at least one of the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis," Shimoda supplies such teachings. As discussed previously, Shimoda teaches a Viterbi trellis corresponding to a maximum likelihood path detection system, wherein RLL code violating states and states transitions are removed from the detection process. (*See supra*.).

191.   It would have been obvious for a person having ordinary skill in the art at the time of the alleged invention to combine the teachings of Tsang and

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Shimoda to arrive at the alleged invention recited in claim 12. Tsang expressly discloses the use of a "trellis diagram" to eliminate "invalid patterns." In particular, a person of ordinary skill would have naturally looked to different trellis options in the art, including the Viterbi trellis corresponding to a "maximum likelihood path" detection system taught by Shimoda to accomplish this elimination of "invalid patterns," especially because it was well-known that the purpose of optimal "maximum likelihood path detection" systems such as disclosed in Shimoda is to lower the bit error rate. A maximum likelihood path detection system computes the most probable input resulting in an observed output. One of ordinary skill would have thus been motivated the Viterbi trellis of Shimoda as the "trellis diagram" that eliminates "invalid patterns" in Tsang. Further, using the Viterbi trellis from Shimoda for the "trellis diagram" from Tsang was well within the ability of one of ordinary skill in the art at the time of the invention of the '601 patent. Indeed, removing code violating states and state transitions from a Viterbi trellis was a routine function at that time, well-known and easily employed by even graduate students. Moreover, doing so would have produced the predictable (and desirable) result of a lower bit error rate.

192. Further, a person of ordinary skill would have been motivated to include in the detection process a step of removing states and state transitions corresponding to more than j consecutive transitions from the Viterbi trellis, as

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taught by Shimoda, because then the device does not need to "have any structural elements related to the state transitions which do not take place due to the rule" of the MTR code, (Ex. 1008 at 4:28-40), making the device more "compact" and "less expensive." (*Id.* at 2:64-65.)

193. Claim 12 is therefore obvious over Tsang in view of Shimoda.

B. Claim 21 is obvious over Tsang in view of Shimoda.

194. Claim 21 recites "The method as in claim 13 wherein the method of receiving data incorporates the removal of certain code-violating patterns from the detection process wherein the detection process comprises *at least one* of the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis ..." [Emphasis added.]

195. As shown above, Tsang teaches all of the limitations recited in claim 13 from which claim 21 depends. Further, "method" claim 21 is similar to "apparatus" claim 12. As shown above, apparatus claim 12 is obvious over Tsang in view of Shimoda. Method claim 21 is obvious over Tsang in view of Shimoda, for the same reasons that claim 12 is obvious.

196. Again, if Tsang does not disclose "means for removing certain code-violating patterns from the detection process wherein the detection process comprises at least one of the steps of: removing states and state transitions corresponding to more than j consecutive transitions from a Viterbi trellis,"

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Shimoda supplies such teachings. As discussed previously, Shimoda teaches a Viterbi trellis corresponding to a maximum likelihood path detection system, wherein RLL code violating states and states transitions are removed from the detection process.

197. It would have been obvious for a person having ordinary skill in the art at the time of the alleged invention to combine the teachings of Tsang and Shimoda to arrive at the alleged invention recited in claim 21.

198. Claim 21 is therefore obvious over Tsang in view of Shimoda, for the same reasons that claim 12 is obvious over Tsang in view of Shimoda

XI. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

199. As discussed above, I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the inventors proceeded contrary to the accepted wisdom of the prior art.

200. I have considered these factors in my above obviousness analyses and am not aware of any evidence at this stage indicating that at any of these factors would weigh against a finding of obviousness.

XII. CONCLUSION

201. For the reasons given above, it is my opinion that the Challenged Claims of the '601 patent are not patentable, and should be cancelled.

APPENDIX A

Maximum Transition Run Codes for Data Storage Systems

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Abstract — A new code is presented which improves the minimum distance properties of sequence detectors operating at high linear densities. This code, which is called the maximum transition run code, eliminates data patterns producing three or more consecutive transitions while imposing the usual k-constraint necessary for timing recovery. The code possesses the similar distance-gaining property of the $(1,k)$ code, but can be implemented with considerably higher rates. Bit error rate simulations on fixed delay tree search with decision feedback and high order partial response maximum likelihood detectors confirm large coding gains over the conventional $(0,k)$ code.

I. INTRODUCTION

IN this paper, we present a new code designed to improve the distance properties of sequence detectors operating at relatively high linear densities. The basic idea is to eliminate certain input bit patterns that would cause most errors in sequence detectors. More specifically, the code eliminates input patterns that contain three or more consecutive transitions in the corresponding current waveform, and, as a result, the performance of any near-optimal sequence detector improves substantially at high linear densities [1][2]. This code constraint, designated the maximum transition-run (MTR) constraint, can be realized with simple fixed-length block codes with rates only slightly lower than the conventional $(0,k)$ code. Bit error rate (BER) simulation results with fixed delay tree search with decision feedback (FDTS/DF) detection and high order partial response maximum likelihood (PRML) detection confirm a large coding gain of the MTR codes over the conventional $(0,k)$ code.

II. CODING METHODS

Investigation of high density error patterns in FDTS/DF detection reveals that errors arise mostly due to the detector's inability to distinguish the minimum distance transition patterns, four pairs of which are shown in Fig. 1. These pairs of magnetization waveforms give rise to an NRZ input error pattern of $e_k = \pm\{2 \ -2 \ 2\}$, assuming input data take on +1's and -1's. The proposed approach is to remove data patterns allowing this type of error pattern through coding. The potential improvement in the FDTS detection performance using this approach can be estimated by computing the increase in the minimum distance between two diverging lookahead tree paths after removing the paths that allow the $\pm\{2 \ -2 \ 2\}$ error events [3]. A simple minimum distance analysis for PRML systems reveals that this is also a critical error pattern in high order PRML systems such as

E^2PR4ML. Note that a traditional $(1,k)$ runlength limited (RLL) code eliminates all eight transition patterns shown in Fig. 1 [4][5], but the rate penalty is typically too large to see any coding gain unless the linear density is very high. The idea of MTR coding is to eliminate three or more consecutive transitions, but allow the dibit pattern in the written magnetization waveform. Thus, with MTR coding, the error events of the form $\pm\{2 \ -2 \ 2\}$ will still be prevented as with $(1,k)$ coding, but the rate penalty is significantly smaller than that of the typical $(1,k)$ RLL code. Notice that with the MTR constraint, the write precompensation efforts can be directed mainly on dibit transitions, unlike in conventional $(0,k)$ coded systems. An independent study also suggests that removing long runs of consecutive transitions improves the offtrack performance in some PRML systems [6]. There exist other types of code constraints that can offer similar distance-enhancing properties for high order PRML systems [7].
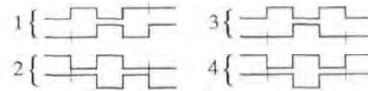

Fig. 1: Pairs of write patterns causing most errors in sequence detection at high linear densities.

Fig. 2 shows the state diagram of the MTR code based on the NRZI convention, where 1 and 0 represent the presence and absence, respectively, of a magnetic transition. Also included is the usual k-constraint for timing recovery. The capacity of the code can be obtained by finding the largest eigenvalue of the adjacency matrix for the given state diagram [8]. The capacities for different k values are given in Table 1
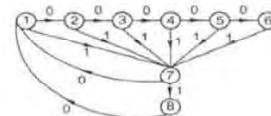

Fig. 2: State transition diagram for the MTR code with $k=6$.

k	capacity	k	capacity
4	.8376	8	.8760
5	.8579	9	.8774
6	.8680	10	.8782
7	.8732	∞	.8791

Table 1: Capacities for MTR codes.

While state-dependent encoders and sliding-block decoders can be designed for the MTR constraint (which can be easily generalized to limit any runs of consecutive transitions), we observe that simple fixed-length block codes can be realized with

good rates and reasonable k values. A computer search is utilized to first find all n-bit codewords that are free of an NRZI 111 string or $k+1$ consecutive NRZI 0's. Then, in order to meet the MTR constraint at the codeword boundaries, words that start or end with an NRZI 11 string are removed. Also, the k constraint is satisfied at the boundary by removing the words with k_1+1 leading 0's or k_2+1 trailing 0's, where $k_1+k_2=k$. Finally, if the number of the remaining codewords is greater than or equal to 2^m, then those codewords can be used to implement a rate m/n block code. Table 2 shows important code parameters for representative block codes obtained through computer search. The efficiency was found by dividing the code rate m/n by the capacity computed for the given value of k and the MTR constraint. As an example of an MTR block code, 16 codewords required to implement the rate 4/5 code with $k=8$ are given in Table 3.

m	n	k	eff.	No. avail. codewords	No. needed codewords
4	5	8	.91	16	16
8	10	6	.92	282	256
9	11	6	.94	514	512
10	12	8	.95	1,066	1,024
14	17	6	.95	18,996	16,384
16	19	7	.96	69,534	65,536
24	28	8	.98	17,650,478	16,777,216

Table 2: Parameters for MTR block codes.

00001	00110	01100	10010
00010	01000	01101	10100
00100	01001	10000	10101
00101	01010	10001	10110

Table 3: A rate 4/5 MTR block code with $k=8$.

III. MODIFIED DETECTION AND DISTANCE INCREASE

To realize the coding gain at the detector output, the detector has to be modified. In the case of PRML systems, this amounts to removing those states and state transitions that correspond to the illegal data patterns from the trellis diagram. For the FDTS/DF detector, the code-violating lookahead paths must be prevented from being chosen as the most-likely path, a technique similar to the one used in the (1,7) coded FDTS/DF channel [9]. To illustrate the idea, consider Fig. 3 that shows a $\tau=2$ lookahead tree utilized in FDTS/DF detection. By utilizing the past decision, an illegal path, which contains three consecutive transitions, can be identified as indicated by either the solid (when the past decision is -1) path or the shaded (when the past decision is 1) path. The complexity of the FDTS/DF detector can also be reduced considerably with the MTR code, as elaborated in a companion paper [10].
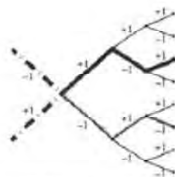

Fig. 3: Modified FDTS detection with MTR coding

With this modification in FDTS/DF detection, the squared minimum Euclidean distance between any two diverging paths, denoted by β_{min}^2, is given by $4\cdot(1+f_1^2+f_2^2+\cdots+f_\tau^2)$ for τ greater than or equal to 2, where f_k represents the equalized dibit response (at the output of the forward equalizer). For example, the effective SNR gain of the $\tau=2$ FDTS/DF over the decision feedback equalization (DFE) channel, assuming the same MTR code, is given by $10\cdot\log_{10}(1+f_1^2+f_2^2)$ dB.

The distance gain with MTR coding is also significant for high order PRML systems such as E^2PR4. When the critical NRZ error pattern is $\pm\{2\ -2\ 2\}$, the minimum distance for the E^2PR4 response $\{1\ 2\ 0\ -2\ -1\}$ is $6\sqrt{2}$. With MTR coding, the worst case error pattern becomes a single bit error pattern of $\pm\{2\}$, and the corresponding channel output distance is simply the square root of the energy in the equalized dibit response, or $10\sqrt{2}$. This increase in the minimum distance is equivalent to an SNR gain of 2.218 dB. When the code rate penalty is small, the overall coding gain is significant.

IV. BER SIMULATION RESULTS

To verify the coding gain, FDTS/DF detection was simulated with the rate 4/5 and rate 16/19 MTR codes as well as with a rate 8/9 $(0,k)$ code. The BERs were first obtained as a function of readback SNR for different tree depths. The BER of the PR4ML detector was also simulated for comparison. The Lorentzian transition response was assumed, and the user density, defined as PW50 over the user bit interval, is fixed at 2.5 for all codes. The SNR value required to achieve an error rate of 10^{-5} was then recorded for each depth/code combination.

The results are summarized in Fig. 4, where the effective SNR improvement of each system over PR4ML is shown. The performance advantage of MTR codes is clear. With the rate 16/19 MTR code, for example, the depth 1 FDTS/DF performs as well as the depth 5 FDTS/DF used with the conventional $(0,k)$ code, yielding a 2.5 dB gain over the PR4ML. When the 4/5 MTR code is used, FDTS/DF with a tree depth of 2 outperforms the depth 5 FDTS/DF with the 8/9 $(0,k)$ code. For a given tree depth, the rate 16/19 MTR code yields a 1.5 - 2 dB coding gain over the conventional 8/9 $(0,k)$ code.

Also shown are the SNR performances of PRML systems with and without MTR coding. The coding gain is obvious with E^2PRML and E^3PRML, in which the minimum distance is improved with the MTR code. However, with EPR4ML the performance advantage of the MTR code is small since the MTR code does not improve the minimum distance in the EPR4 system. This is because the minimum distance error pattern in an EPR4 system is of the form $\pm\{2\}$, which is not affected by the MTR constraint. The MTR code does, however, eliminate non-minimum distance error patterns of the form $\pm\{\ldots2\ -2\ 2\ldots\}$, resulting in a small performance improvement over the $(0,k)$ coded EPR4 system when the code rate is sufficiently high as with the 16/19 code.

Comparisons also can be made between the PRML systems and FDTS/DF systems. For example, the depth 2 FDTS/DF with the rate 4/5 MTR code improves more than 1 dB over EPR4ML with the rate 8/9 $(0,k)$ code. At this density and with a Lorentzian transition response, EPR4ML has a 1.5 dB advantage over PR4ML. Of the PR targets, the EPR4 appears to provide a best fit

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to the natural channel as indicated by the superior performance of EPR4ML over even higher order PRML systems. Large enough FIR filters are used for equalization for both PRML and FDTS/DF systems so that the performances are not degraded by imperfect equalization.

In Fig. 5, similar plots are presented for a modeled MR head response. The trends are similar to the Lorentzian case, except that within the PRML family the performance improves as the order of the PR polynomial increases. Also, the MTR coding gain is larger than in the case of the Lorentzian response for all detectors. The depth 2 FDTS/DF channel with the rate 4/5 MTR code provides a 2.5 dB SNR gain over the EPR4ML channel with the rate 8/9 $(0,k)$ code. With the particular MR head response used here, EPR4ML already has a 4 dB advantage over PR4ML at this linear density.

Since the MTR code eliminates data patterns with crowded transitions, the overall transition noise, as measured per unit length of track, is expected to be reduced. Fig. 6 shows the simulation results similar to those presented in Fig. 5, except random transition position jitter and transition width variations are included in the read waveform construction process [11]. The rms values of both transition noise parameters are set at 4.4 % of the user bit interval. The SNR reflects only the additive noise component. As is evident from the figure, the coding gain of the MTR code over the $(0,k)$ code is much larger in the presence of transition noise. For example, with $\tau=2$ FDTS/DF detection, the SNR difference is 6 dB between the rate 4/5 MTR code and the rate 8/9 $(0,k)$ code which allows long runs of consecutive transitions.

Although the results are not shown here, we have also observed that the MTR code tends to reduce the relative frequencies of long error events in DFE and FDTS/DF systems.
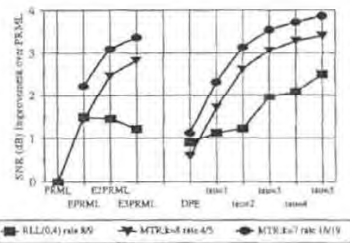

Fig. 4: Summary of PRML and FDTS/DF performances with and without MTR codes (Lorentzian response and additive noise).
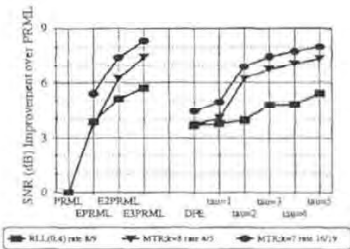

Fig. 5: Summary of PRML and FDTS/DF performances with and without MTR codes (MR head response and additive noise).
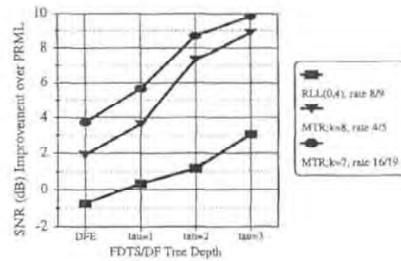

Fig. 6: Summary of FDTS/DF performances with and without MTR codes (MR head response and mixed noise).

V. CONCLUSION

A simple coding scheme is presented which improves the performance of FDTS/DF and high order PRML systems operating at relatively high linear densities. The code eliminates three or more consecutive transitions while allowing the k-constraint for timing purposes. The code can be implemented as simple block codes with reasonable rates such as 4/5, 8/10 and 16/19. BER simulations on FDTS/DF and PRML systems confirm large coding gains over the conventional $(0,k)$ code.

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APPENDIX B

On–track and off–track distance properties
of Class 4 partial response channels

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ABSTRACT

We consider Class 4 partial response (PR) channels, and examine off-track performance of maximum likeli-
hood sequence estimators for these channels that ignore inter-track interference (ITI). We assume that the pulse
response to the head from an adjacent track is the same Class 4 channel, and only its amplitude varies with the
track-to-head distance, in a way not known to the receiver. For each of these channels, we find analytical expres-
sions for off-track performance, as well as sets of sequences most susceptible to errors in the ITI environment. We
also discuss how the problem of off-track error rate can be alleviated through coding.

Keywords: magnetic recording, class 4, partial response, off–track performance, coding.

1   INTRODUCTION

The transfer function of a digital magnetic recording channel for a given linear density can be closely approx-
imated by a partial response (PR) polynomial of the form $(1 - D)(1 + D)^N$, for some integer $N \geq 1$. In general,
higher linear densities require higher order polynomials. Equalization of a recording channel to the PR channel
with the transfer function that best approximates the channel transfer function at a given density will incur the
least equalization loss.

A significant noise source in magnetic recording channels is inter-track interference (ITI). When the read head
is not centered over the data track, it is partially positioned over an adjacent track and picks up the magnetization
from it. When tracks become narrow, the side *fringing* causes the head to pick up signals from an adjacent track,
even if it is not physically over that track. An important issue that should affect the choice of N is, therefore,
the performance of the corresponding channel in the presence of ITI, often referred to as off-track performance.

Magnetic recording channels at current linear densities resemble channels with transfer functions of the above form for $N = 1, 2, 3$, referred to as *Class 4* partial response. These channels are also known as $1 - D^2$ or PR4, $(1 - D)(1 + D)^2$ or EPR4, and $(1 - D)(1 + D)^3$ or EEPR4. Most of the commercially available detectors employ PR equalization to the PR4 channel. Using the same detection system at higher linear densities would result in a performance loss. Thus the system should be either augmented by a coding scheme, which would recover the loss through the coding gain, or replaced by a detection system employing PR equalization to the EPR4 or EEPR4 channel. In any case the new system should have good off-track properties.

Several studies analyzed off-track performance of Class 4 channels by simulation (see for example Sayiner[9] and references therein). We find analytical expressions for off-track performance of these channels, as well as sets of sequences most susceptible to errors in the ITI environment. We discuss how the problem of off-track error rate can be alleviated through coding.

In Section II we derive a bound on the error-probability performance for a general discrete-time recording channel with additive white Gaussian noise and a general model of ITI. In Section III we consider Class 4 channels under the assumption that the pulse response to the head from an adjacent track is the same Class 4 channel and only its amplitude varies with the track to head distance. In Section IV we discuss possibilities of coding for these systems. In Section V we provide an extensive summary of the obtained results, for the benefit of a reader not very interested in mathematical details.

2 DISCRETE TIME MAGNETIC RECORDING CHANNEL

2.1 Channel model

We consider a discrete-time model for the magnetic recording channel with input $a = \{a_n\} \in \mathcal{C} \subseteq \{-1, 1\}^\infty$, impulse response $\{h_n\}$, and output $y = \{y_n\}$ given by

$$y_n = \sqrt{E} \sum_m a_m h_{n-m} + \eta_n. \tag{1}$$

where h_n are integer, η_n are independent Gaussian random variables with zero mean and variance σ^2, and E is a constant related to the output voltage amplitude. We refer to E/σ^2 as the signal-to-noise ratio (SNR) per track. In the case of ITI, when the read head picks up magnetization from an adjacent track, the channel model becomes

$$y_n = \sqrt{E} \sum_m a_m h_{n-m} + \sqrt{E} \sum_m x_m g_{n-m} + \eta_n, \tag{2}$$

where $\{g_n\}$ is the discrete-time impulse response of the head to the adjacent track and $x = \{x_n\} \in \mathcal{C}$ is the sequence recorded on that track.

We analyze the performance of the receiver that ignores the ITI assuming the received signal to be as given by (1). It performs maximum likelihood sequence estimation (MLSE) for that model, *i.e.*, it determines an $\widehat{a}$ satisfying

$$\min_{a \in \mathcal{C}} \Omega(a) = \Omega(\widehat{a}),$$

where $\Omega(a)$ is the well known log-likelihood function for channels with inter-symbol interference,[4]

$$\Omega(a) = \sum_n \left(y_n - \sqrt{E} \sum_m a_m h_{n-m} \right)^2. \tag{3}$$

2.2 Error–probability performance

Let $a = \{a_n\}$ and $b = \{b_n\}$ be two allowable recorded sequences which differ in a finite number of places, and $\epsilon = \{\epsilon_n = (a_n - b_n)/2\}$ be the normalized error sequence corresponding to a and b. In the case of no ITI, probability of detecting b given that a was recorded equals to $Q(d(\epsilon)\sqrt{\mathrm{SNR}})$, where $d(\epsilon)$ is the distance between a and b given by

$$d^2(\epsilon) = \sum_n \left(\sum_m \epsilon_m h_{n-m} \right)^2. \tag{4}$$

Thus a lower bound to the minimum probability of an error event in the system is proportional to $Q(d_{\min}\sqrt{\mathrm{SNR}})$, where $d_{\min} = \min_{\epsilon \neq 0} d(\epsilon)$.

In the case of ITI we examine the probability of detecting sequence b given that sequence a was recorded on the track being read and sequence x was recorded on an adjacent track. This probability is given by

$$P[\Omega(b) < \Omega(a)|a, x] = P[\Omega(b) - \Omega(a) < 0|a, x].$$

Expressing $\Omega(a)$ and $\Omega(b)$ as in (3), we obtain

$$P[\Omega(b) - \Omega(a) < 0|a, x] =$$
$$P\left[\sum_n \left(y_n - \sqrt{E} \sum_m a_m h_{n-m} \right)^2 - \sum_n \left(y_n - \sqrt{E} \sum_m b_m h_{n-m} \right)^2 < 0|a, x \right]$$

Substituting (2) for y_n in the above equation gives

$$P[\Omega(b) - \Omega(a) < 0|a, x] = P\left[\sum_n \eta_n \sum_m \epsilon_m h_{n-m} + \sqrt{E} \sum_n \left(\sum_m \epsilon_m h_{n-m} \right)^2 + \right.$$
$$\left. \sqrt{E} \sum_n \left(\sum_m x_m g_{n-m} \right) \left(\sum_m \epsilon_m h_{n-m} \right) < 0 \right],$$

where and $\epsilon_n = (a_n - b_n)/2$. Since

$$\frac{1}{\sigma \left[\sum_n \left(\sum_m \epsilon_m h_{n-m} \right)^2 \right]^{1/2}} \sum_n \eta_n \sum_m \epsilon_m h_{n-m}$$

is a zero-mean, unit-variance Gaussian random variable, we have

$$P[\Omega(b) - \Omega(a) < 0|a, x] = Q(\delta(\epsilon, x)\sqrt{\mathrm{SNR}}),$$

where $\delta(\epsilon, x)$ is the distance between a and b in the *presence* of x given by

$$\delta(\epsilon, x) = \frac{\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2 + \sum_n \left(\sum_m x_m g_{n-m}\right)\left(\sum_m \epsilon_m h_{n-m}\right)}{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^{1/2}}.$$

Thus a lower bound to the minimum probability of an error event in the system is proportional to $Q\left(\delta_{\min}\sqrt{\text{SNR}}\right)$, where $\delta_{\min} = \min_{\epsilon \neq 0, x \in C} \delta(\epsilon, x)$.

We derive a simple lower bound on $\delta(\epsilon, x)$ as follows:

$$\delta(\epsilon, x) \geq \frac{\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2 - \left|\sum_n \left(\sum_m x_m g_{n-m}\right)\left(\sum_m \epsilon_m h_{n-m}\right)\right|}{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^{1/2}}$$

$$\geq \frac{\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2 - \sum_n M \left|\sum_m \epsilon_m h_{n-m}\right|}{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^{1/2}},$$

where $M = \max_{n, x \in C} \sum_m x_m g_{n-m}$, *i.e.*, M is the maximum absolute value of the interference. Note that $M = \sum_n |g_n|$. We'll assume that $M < 1$. Since the h_n are integers and $\epsilon_n \in \{-1, 0, 1\}$, we can further bound $\delta(\epsilon, x)$ as follows:

$$\delta(\epsilon, x) \geq \frac{\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2 - M \sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2}{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^{1/2}}$$

$$= (1 - M)\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^{1/2},$$

and thus

$$\delta_{\min} = \min_{\epsilon, x} \delta(\epsilon, x) \geq (1 - M)d_{\min}.$$

The bound is achieved if and only if there exists an $\epsilon \in \arg\min_{\epsilon \neq 0} d(\epsilon)$ for which $\sum_m \epsilon_m h_{n-m} \in \{-1, 0, 1\}$ for all n, and there exists an $x \in C$ such that $\sum_m x_m g_{n-m} = \mp M$ whenever $\sum_m \epsilon_m h_{n-m} = \pm 1$. We show below that this bound can be achieved for the PR4 and the EPR4 channels but not for the EEPR4 channel.

3 DISTANCE PROPERTIES OF BINARY CLASS 4 CHANNELS

We now consider Class 4 channels, *i.e.*, channels with transfer functions given by $H(D) = \sum_n h_n D^n = (1 - D)(1 + D)^N$ for $N = 1, 2, 3$. We assume that the pulse response to the head from an adjacent track is the same Class 4 channel, and only its amplitude varies with the track to head distance with a parameter α, *i.e.* $g_n = \alpha h_n$. This assumption is only approximate since the transition response from a track to a head gets wider as the distance between them increases, as discussed by Vea and Moura[2] and Lindholm.[3] With $g_n = \alpha h_n$, the above lower bound becomes

$$\delta_{\min} = \min_{\epsilon, x} \delta(\epsilon, x) \geq (1 - \alpha A)d_{\min}, \tag{5}$$

where A is the maximum value of the noiseless Class 4 channel output; $A = 2, 4, 6$ and $d_{\min}^2 = 2, 4, 6$ for $N = 1, 2, 3$, respectively.

For the three Class 4 channels, we examine if the bound can be achieved by working in the transform domain where each sequence $\{s_n\}$ has a corresponding function $S(D) = \sum_n s_n D^n$. For that purpose, we note that the minimum distance of the uncoded channel with transfer function $H(D)$ with no ITI, defined by (4), can be expressed as

$$d_{min}^2 = \min_{\epsilon(D) \neq 0} \|H(D)\epsilon(D)\|^2,$$

where $\epsilon(D) = \sum_{i=0}^{l-1} \epsilon_i D^i$, $\epsilon_i \in \{-1, 0, 1\}$, $\epsilon_0 \neq 0$, $\epsilon_{l-1} \neq 0$, is the polynomial corresponding to a normalized error sequence $\epsilon = \{\epsilon_i\}_{i=1}^{l-1}$ of length l, and the squared norm of a polynomial refers to the sum of its squared coefficients. The bound (5) is achieved if and only if there exists an $e(D)$ for which $\|H(D)\epsilon(D)\|^2 = d_{min}^2$ and all coefficients y_n of $y(D) = H(D)\epsilon(D)$ are in the set $\{-1, 0, 1\}$, and there exists an $x \in C$ such that in $H(D) \cdot \sum_n x_n D^n = \sum_n z_n D^n$, $z_n = \mp A$ whenever $y_n = \pm 1$.

3.1 The PR4 channel

For $N = 1$ the channel transfer function is equal to $1 - D^2$. This channel is usually treated as two interleaved $1 - D$ channels. For the $1 - D$ channel $d_{min}^2 = 2$ is attained for $\epsilon(D) = \sum_{k=0}^{l-1} D^k$. In this case $\delta(\epsilon, x)$ achieves lower bound (5) for $x = \{\cdots, x_{-2}, 1, -1, x_1, \cdots, x_{l-2}, -1, 1, x_{l+1}, \cdots\}$, since the only non-zero coefficients of $y(D) = 1 - D^l$ are $y_0 = 1$, $y_l = -1$, and in $(1 - D) \cdot \sum_n x_n D^n = \sum_k z_k D^k$, we have $z_0 = -2$ and $z_l = 2$. Therefore, for the PR4 channel, $\delta_{min} = \sqrt{2}(1 - 2\alpha)$.

EXAMPLE 1. Consider a noiseless $1 - D$ channel. Let sequences a, b, $\epsilon = (a - b)/2$, and x be as follows:

$$
\begin{aligned}
a &= \cdots, a_{-1}, -1, +1, +1, +1, a_4, \cdots \\
b &= \cdots, a_{-1}, -1, -1, -1, +1, a_4, \cdots \\
\epsilon &= \cdots, \quad 0, \quad 0, +1, +1, \quad 0, \quad 0, \cdots \\
x &= \cdots, x_{-1}, +1, -1, -1, +1, x_4, \cdots
\end{aligned}
$$

Let a be recorded on the track being read and x recorded on an adjacent track. Then $\delta(\epsilon, x) = \sqrt{2}$ for $\alpha = 0$, $\delta(\epsilon, x) = 1/\sqrt{2}$ for $\alpha = 0.25$, and $\delta(\epsilon, x) = 0$ for $\alpha = 0.5$.

3.2 The EPR4 channel

For $N = 2$ the channel transfer function is equal to $(1 - D)(1 + D)^2$. It is well known that $d_{min}^2 = 4$ is attained for $\epsilon(D) = 1$, which gives $y(D) = 1 + D - D^2 - D^3$. However, for the corresponding error sequence, $\delta(\epsilon, x)$ cannot achieve lower bound (5) because that would require a sequence x for which two successive outputs of the EPR4 channel equal to 4. In order to see if the lower bound can be achieved, we find all error polynomials $\epsilon(D)$ for which $\|(1 - D)(1 + D)^2 \epsilon(D)\|^2 = 4$.

Polynomial $y(D) = (1 - D)(1 + D)^2 \epsilon(D)$ with $\|y(D)\|^2 = 4$ is of the form $1 + c_1 D^{p_1} + c_2 D^{p_2} + c_3 D^{p_3}$ where, for $i \in \{1, 2, 3\}$, $c_i \in \{-1, 1\}$ and p_i are three different positive integers. From the definition of $y(D)$, we know

that $y(1) = 0$, $y(-1) = 0$, $y'\epsilon(1) = 0$ must be satisfied. It can be shown that these conditions require that $y(D)$ be either of the form $\left(1 - D^{2k} + D^{2n+1} - D^{2(k+n)+1}\right)$, $k \geq 1$, $n \geq 0$, or of the form $\left(1 - D^{2k} - D^{2n} + D^{2(k+n)}\right)$, $k, n \geq 1$, $k \neq n$. To further specify $y(D)$ and find the corresponding $\epsilon(D)$, we consider these two cases separately.

1. Polynomial $(1 - D)(1 + D)^2 \epsilon(D) = 1 - D^{2k} + D^{2n+1} - D^{2(k+n)+1}$ factors as

$$(1 - D)(1 + D)^2 \cdot \left(\sum_{j=0}^{k-1} D^{2j}\right)\left(\sum_{i=0}^{2n}(-1)^i D^i\right).$$

Therefore $\epsilon(D) = \left(\sum_{i=0}^{2n}(-1)^i D^i\right)\left(\sum_{j=0}^{k-1} D^{2j}\right)$. Since the coefficient of $\epsilon(D)$ are in $\{-1, 0, 1\}$, we conclude that an arbitrary $k > 1$ requires $n = 0$ and an arbitrary $n > 0$ requires $k = 1$. In the first case $\epsilon(D) = \sum_{j=0}^{k-1} D^{2j}$ and $y(D) = 1 + D - D^{2k} - D^{2k+1}$. In the second case $\epsilon(D) = \sum_{i=0}^{2n}(-1)^i D^i$ and $y(D) = \left(1 - D^2 + D^{2n+1} - D^{2n+3}\right)$.

2. Polynomial $(1 - D)(1 + D)^2 \epsilon(D) = 1 - D^{2n} - D^{2k} - D^{2(k+n)}$ factors as

$$(1 - D)(1 + D)^2 \cdot \left(\sum_{j=0}^{k-1} D^{2j}\right)\left(\sum_{i=0}^{2n-1}(-1)^i D^i\right).$$

Therefore $\epsilon(D) = \left(\sum_{i=0}^{2n-1}(-1)^i D^i\right)\left(\sum_{j=0}^{k-1} D^{2j}\right)$. Since the coefficient of $\epsilon(D)$ are in $\{-1, 0, 1\}$, we conclude that an arbitrary $k > 1$ requires $n = 1$ and an arbitrary $n > 1$ requires $k = 1$. In the first case $\epsilon(D) = \sum_{j=0}^{2k-1}(-1)^j D^j$ and $y(D) = 1 - D^2 - D^{2k} + D^{2k+2}$. In the second case $\epsilon(D) = \sum_{i=0}^{2n-1}(-1)^i D^i$ and $y(D) = 1 - D^2 - D^{2n} + D^{2n+2}$. These two cases are equivalent as was expected from the symmetry of the original $y(D)$ with respect to n and k.

From 1. and 2. we conclude that the error polynomials $\epsilon(D)$ for which $\|(1 - D)(1 + D)^2 \epsilon(D)\|^2 = 4$ are either of the form $\epsilon(D) = \sum_{j=0}^{k-1} D^{2j}$, $k \geq 1$, in which case $y(D) = \left(1 + D - D^{2k} - D^{2k+1}\right)$, or of the form $\epsilon(D) = \sum_{i=0}^{l-1}(-1)^i D^i$, $l \geq 3$, in which case $y(D) = \left(1 - D^2 - (-1)^l D^l + (-1)^l D^{l+2}\right)$. In the former case $\delta(\epsilon, x)$ cannot achieve lower bound (5) because, as above, it would require a sequence x for which two successive outputs of the EPR4 channel equal to 4. It can be shown that in this case $\min_{x \in \mathcal{C}} \delta(\epsilon, x) = \sqrt{4}(1 - 3\alpha)$. In the latter case $\delta(\epsilon, x)$ achieves the lower bound for

$$x = \{\cdots, x_{-4}, -1, -1, 1, 1, -1, -1, x_3, \cdots, x_{l-4}, -1, -1, 1, 1, -1, -1, x_{l+3}, \cdots\}$$

for odd $l \geq 5$, or

$$x = \{\cdots, x_4, -1, -1, 1, 1, -1, -1, x_3, \cdots, x_{l-4}, 1, 1, -1, -1, 1, 1, x_{l+3}, \cdots\}$$

for even $l \geq 6$. It can be shown that $\min_{x \in \mathcal{C}} \delta(\epsilon, x) = \sqrt{4}(1 - 3\alpha)$ for $l = 3, 4$. Therefore, for the EPR4 channel, $\delta_{\min} = \sqrt{4}(1 - 4\alpha)$.

EXAMPLE 2. Consider a noiseless EPR4 channel. Let sequences a, b, $\epsilon = (a - b)/2$, and x be as follows:

$$
\begin{aligned}
a &= \cdots, a_{-3}, a_{-2}, a_{-1}, -1, +1, -1, +1, -1, +1, a_6, a_7, a_8, \cdots \\
b &= \cdots, a_{-3}, a_{-2}, a_{-1}, +1, -1, +1, -1, +1, -1, a_6, a_7, a_8, \cdots \\
\epsilon &= \cdots, \quad 0, \quad 0, \quad 0, -1, +1, -1, +1, -1, +1, \quad 0, \quad 0, \quad 0, \cdots \\
x &= \cdots, -1, -1, +1, +1, -1, -1, +1, +1, -1, -1, +1, +1, \cdots
\end{aligned}
$$

Let a be recorded on the track being read and x recorded on an adjacent track. Then $\delta(\epsilon, x) = \sqrt{4}$ for $\alpha = 0$, and $\delta(\epsilon, x) = 0$ for $\alpha = 0.25$.

3.3 The EEPR4 channel

For $N = 3$ the channel transfer function is equal to $(1-D)(1+D)^3$. Again, it is well known that $d_{\min}^2 = 6$ is attained for $\epsilon(D) = 1 - D + D^2$, which gives $y(D) = 1 + D - D^2 + D^4 - D^5 - D^6$. However, similarly as above, for the corresponding error sequence, $\delta(\epsilon, x)$ cannot achieve lower bound (5) because that would require a sequence x for which a string of three successive outputs of the EEPR4 channel equals to $6, 6, -6$. In order to see if the bound can be achieved, we find all error polynomials $\epsilon(D)$ for which $\|(1-D)(1+D)^3\epsilon(D)\|^2 = 6$. We consider polynomial $y(D) = (1-D)(1+D)^3\epsilon(D) = (1+2D-2D^3-D^4)\cdot(1+e_1 D+e_2 D^2+\cdots+\epsilon_{l-3}D^{l-3}+\epsilon_{l-2}D^{l-2}+\epsilon_{l-1}D^{l-1})$. It is easy to check that for all error sequences of length $l \leq 2$, $\|y(D)\|^2 \geq 10$. For error sequences of length $l \geq 3$, polynomial $y(D)$ is of the form $1+(\epsilon_1+2)D+(\epsilon_2+2\epsilon_1)D^2+D^3 z(D)+(-2\epsilon_{l-2}-\epsilon_{l-3})D^{l+1}+(-2\epsilon_{l-1}-\epsilon_{l-2})D^{l+2}+(-\epsilon_{l-1})D^{l+3}$, where $z(D)$ is a polynomial with degree of at most $l - 3$. Since $\epsilon_{l-1} \neq 0$, we have $\|y(D)\|^2 \geq 3 + \|z(D)\|^2 + 3$, and therefore $\|y(D)\|^2 = 6$ only if $z(D) = 0$. Therefore $y(D) = 1 + D - D^2 + (-2\epsilon_{l-2} - \epsilon_{l-3})D^{l+1} + (-2\epsilon_{l-1} - \epsilon_{l-2})D^{l+2} + (-\epsilon_{l-1})D^{l+3}$. For $y(1) = 0$, we need $y(D) = 1 + D - D^2 + D^{l+1} - D^{l+2} - D^{l+3}$. For $y(-1) = 0$, we need $y(D) = 1 + D - D^2 + D^{2k} - D^{2k+1} - D^{2k+2}$. For $y'(-1) = 0$, we need $y(D) = 1 + D - D^2 + D^4 - D^5 - D^6$. Note that $y(D) = 1 + D - D^2 + D^4 - D^5 - D^6 = (1-D)(1+D)^3 \cdot (1 - D + D^2)$, and therefore $\epsilon(D) = 1 - D + D^2$ is the only error polynomial for which $\|(1-D)(1+D)^3\epsilon(D)\|^2 = 6$. It can be shown that for the corresponding error sequence ϵ, $\min_{x \in C} \delta(\epsilon, x) = \sqrt{6}(1 - 4\alpha)$. Note that this does not determine $\delta_{\min}$ for the EEPR4 channel.

4 CODING FOR IMPROVING OFF–TRACK PERFORMANCE

It was shown above that a lower bound to the minimum probability of an error-event in the system with ITI is proportional to $Q(\delta_{\min}\sqrt{\text{SNR}})$, where

$$\delta_{\min} = \min_{\epsilon, x} \delta(\epsilon, x) \geq (1 - M)d_{\min}.$$

This bound was derived for an arbitrary set of recorded sequences, $C \subseteq \{-1, 1\}^\infty$, and therefore holds in coded as well as uncoded systems. Whether it can be achieved depends on the code. The value of $d_{\min}^2$ is also determined by the code. To improve the error-probability performance of the system, we need codes that increase $d_{\min}^2$ or ensure that the above bound is never achieved or, preferably, perform both tasks.

Codes that increase $d_{\min}^2$ are existing codes designed to improve the on-track performance, $i.e.$, performance of channels with no ITI, as for example matched spectral null codes.[7] In general, these codes may improve the off-track performance as well, since they are likely to reduce the fraction of sequences x for which the bound on $\delta(\epsilon, x)$ can be achieved for a given ϵ. To argue that, we recall that the bound is achieved if and only if there exists an $\epsilon \in \arg\min_{\epsilon \neq 0} d(\epsilon)$ for which $\sum_m \epsilon_m h_{n-m} \in \{-1, 0, 1\}$ for all n and there exists an $x \in C$ such that $\sum_m x_m g_{n-m} = \mp M$ whenever $\sum_m \epsilon_m h_{n-m} = \pm 1$. Codes for improving noise immunity reduce the set of sequences $\epsilon \in \arg\min_{\epsilon \neq 0} d(\epsilon)$ for which $\sum_m \epsilon_m h_{n-m} \in \{-1, 0, 1\}$ for all n. For the sequences that remain, the

number of n such that $\sum_m \epsilon_m h_{n-m} = \pm 1$ is higher, and therefore sequence x has to satisfy more conditions. A good example of this case is a dc-free coded PR4 channel.

Design of high rate codes which improve both on- and off-track error probability performance of Class 4 channels may be a complex problem, and we do not attempt to solve it at this point. Instead, we discuss off-track performance of a dc-free coded PR4 channel and present some coding ideas for the EPR4 and EEPR4 channels which transpired from the above distance properties analysis.

4.1 The PR4 channel

It has been observed in laboratory experiments that a dc-free coded PR4 channel has better off-track performance than its uncoded counterpart.[5] For a dc-free coded $1-D$ channel $d_{\min}^2 = 4$ is obtained for $e(D) = 1 - D^{l-1}$, and the corresponding $y(D)$ is equal to $1 - D - D^{l-1} + D^l$. It is easy to see that in this case $\delta(\epsilon, x)$ achieves lower bound (5) for $x = \{\cdots, x_2, 1, -1, 1, x_2, \cdots, x_{l-3}, -1, 1, -1, x_{l+1}, \cdots\}$ where $l \geq 4$. Therefore, for the dc-free coded PR4 channel, $\delta_{\min} = \sqrt{4(1-2\alpha)}$ degrades with α at the same rate as it does for the uncoded system. However, the sequence x for which the bound is achieved has 6 symbols specified as opposed to at most 4 in the uncoded case. In addition, the bound cannot be achieved for all error sequences for which $\|e(D)H(D)\|^2 = d_{\min}^2$, as in uncoded case, but only for those of length $l \geq 4$.

4.2 The EPR4 channel

Based on the distance properties described above, we know that $\min_{x \in C} \delta(\epsilon, x) = \sqrt{4(1-4\alpha)}$ if and only if $\epsilon(D) = \sum_{i=0}^{l-1} (-1)^i D^i$, $l \geq 5$. It can be shown that for all other error sequences for which $\|H(D)e(D)\|^2 = 4$, we have $\min_{x \in C} \delta(\epsilon, x) = \sqrt{4(1-3\alpha)}$. Therefore, an improvement in the off-track performance of this channel can be accomplished by limiting the length of subsequences of alternating symbols to four. For the NRZI type of recording, this can be achieved by a code that limits the runs of successive ones to three, as the binary complement of the industry standard $8/9\,(0,3)$ block code, introduced for IBM 3480 tape drive. This code has a simple and inexpensive implementation proposed by A. M. Patel.[6] In general, using a code that removes long sequences of alternating symbols at the input of the EPR4 channel is advantageous since these sequences result in long sequences of zeros at the channel output, which is undesirable for timing and gain control.

4.3 The EEPR4 channel

It was shown above that the only error polynomial for which $\|(1-D)(1+D)^3 \epsilon(D)\|^2 = 6$ is $\epsilon(D) = 1 - D + D^2$. This error event can be removed by a code that does not allow successive transitions. For the NRZI type of recording, this can be achieved by a code that does not allow successive ones, as $2/3\,(1,7)$ code. Using this code for high linear density recording systems has already been proposed as a means of reducing the problems associated with closely recorded neighboring transitions. It can be shown that the code also removes all error sequences for

which this polynomial has all its coefficients in the set $\{-1, 0, 1\}$. Therefore $2/3\,(1, 7)$ code gives a performance improvement of for EEPR4 channel with no ITI, and ensures that the lower bound on the performance of the channel with ITI is never achieved. An additional benefit of the code is that it reduces the number of states in the EEPR4 Viterbi detector from 16 to 10 since successive transitions are illegal. The main drawback of the code is its low rate.

5   SUMMARY AND CONCLUSIONS

Magnetic storage detectors employing PR4 equalization exhibit loss in performance at high recording densities and need to be replaced. Two systems are being considered for next generation products: the dc-free coded PR4 channel and the EPR4 channel. Various error probability performance and implementation issues of these two systems should be examined in order to decide which one is a better choice. The analytical results of this paper together with the simulation results obtained by Sayiner[8,9] allow as to compare the systems on the basis of their off-track performance. In addition, the analytical results give an understanding of the systems necessary if coding is to be used for performance improvement.

We analyzed on- and off-track distance properties of PR4, EPR4, and EEPR4 channels, known as Class 4. We also looked at off-track performance of the dc-free coded PR4 channel, and showed some possibilities of improving performance of the EPR4 and EEPR4 channels through coding. Design of high rate codes which improve both on- and off-track error probability performance of Class 4 channels is, however, an interesting open problem. Most of the obtained results are summarized below.

Magnetic recording channels operate at high SNR where the probability of an error event in the system with no ITI is well approximated by $Q(d_{\min}\sqrt{\text{SNR}})$. We found that under the same conditions probability of an error event in the system with ITI is well approximated by $Q(\delta_{\min}\sqrt{\text{SNR}})$, where $\delta_{\min} \geq d_{\min}(1 - M)$ and M is the maximum value that the output of the noiseless channel between the reading head and an adjacent track can take. With the assumption that the pulse response to the reading head from an adjacent track is the same Class 4 channel, and only its amplitude varies with the track to head distance with a parameter α, we have $\delta_{\min} \geq d_{\min}(1 - \alpha A)$ where A is the maximum value the noiseless Class 4 channel output can take ($A = 2, 4$, and 6 for PR4, EPR4, and EPR4 respectively).

We found that the uncoded as well as coded PR4 channel have much better off-track performance than the EPR4 channel, i.e., $\delta_{\min}/d_{\min} = 1 - 2\alpha$ for the PR4 channel and $\delta_{\min}/d_{\min} = 1 - 4\alpha$ for the EPR4 channel, as shown in Fig. 1. The results are in agreement with the ones reported earlier by Sayiner.[8,9] It was found[8] that at a given user density of 2.2, the EPR4 is about 1.2 dB better than the PR4 at 0 % off-track, but only about 0.2 dB at 5 % off-track. In Fig. 1 we see that at 5 % off-track the loss in performance of the PR4 is about 1 dB smaller than the loss of the EPR4.
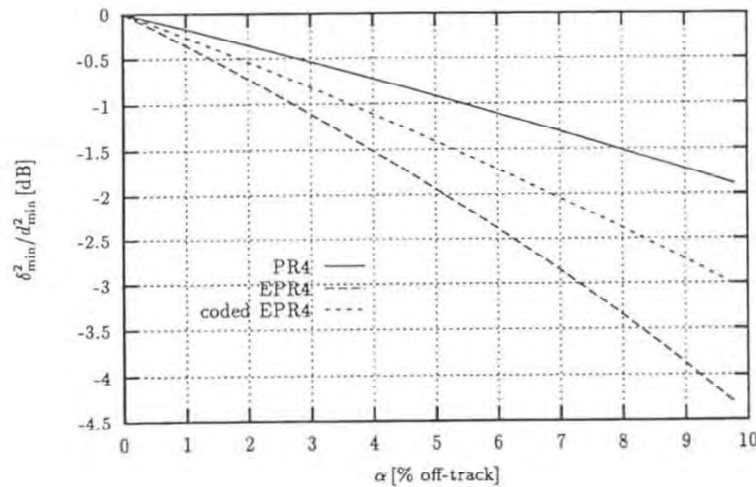
Figure 1: Off-track performance of PR4 and EPR4 channels.

From the EPR4 channel distance properties analysis, we concluded that the channel off-track performance can be improved by a code that limits the runs of successive ones to three. For this purpose we can use the binary complement of the industry standard $8/9\,(0,3)$ block code.

As mentioned above, we also analyzed the distance properties of the EEPR4 channel and showed that its off-track performance for small α is the same as the off-track performance of the EPR4 channel. We also found that the $2/3\,(1,7)$ code gives a performance improvement for the EEPR4 channel with no ITI, and ensures that the lower bound on the performance of the channel with ITI is not achieved.

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[9] N. Sayiner, "The impact of the track density vs. linear density trade-off on the read channel: TCPR4 vs. EPR4," *this conference*.

APPENDIX C

EMINA SOLJANIN

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RESEARCH EXPERTISE AND INTERESTS

Theoretical understanding and practical solutions that enable efficient, reliable, and secure operation of communications networks. Power systems. Quantum computation.

EDUCATION

Ph.D.   Electrical Engineering, Texas A&M University, *1994*.

Dissertation: *Coding for Improving Noise Immunity in Multi-Track, Multi-Head Recording Systems*

Research areas: constrained coding, symbolic dynamics, multi-input, multi-output communications, and data storage.

M.S.   Electrical Engineering, Texas A&M University, *1989*.

Thesis: *New Approach to the Design of Digital Algorithms for Electric Power Measurements*

Research areas: power systems and digital signal processing.

B.S.   European Diploma Degree (M.S. equivalent), Electrical Engineering, University of Sarajevo, Bosnia and Herzegovina (former Yugoslavia), *1986*.

Thesis: *Long-Term Hydro-Plants Scheduling for Electric Power Networks*

Research areas: power systems, stochastic and combinatorial optimization, and graph theory.

EMPLOYMENT HISTORY

Professor, Rutgers University, *Jan. 2016 –*

Member of Technical Staff, Mathematics of Networks and Systems Research Department, Bell Labs, **Postdoctoral** *Sept. 1994 – Dec. 2015 Jan. 1996*, **Regular** *Feb. 1996 – Mar. 2004*, **Distinguished** *Apr. 2004 –*.
Working on a wide range of mathematical problems arising in communications and storage networks; in particular coding, information theoretic, and (more recently) queueing problems concerning efficient, reliable, and secure networking for big data.

Research Engineer, Energoinvest, IRIS Institute, Department for Mathematical Modelling, Sarajevo, Bosnia, *June 1986 – May 1988*.
Developing optimization algorithms and software for power system planning and operation.

TEACHING, MENTORING, AND UNIVERSITY RESEARCH VISITS

Visiting Scientist The Simons Institute for the Theory of Computing, UC Berkeley, *Spring 2015.*

Lecturer for the *2011 Information Theory Summer School.*

Guest Professor at ENSEA/Univ. Cergy-Pontoise/CNRS, ETIS group, France, *Sept. 2010.*

Guest Lecturer at the University College Dublin, Claude Shannon Institute, *Jan. 2009,* teaching an intensive course on *Network Coding.*

Visiting Professor at Ecole Polytechnique Fédérale de Lausanne (EPFL), *Jan.-Dec. 2008*

Adjunct Professor at Columbia University, *Spring 2004–Fall 2005,* teaching *Communication Theory I & II.*

Adjunct Professor at Brooklyn Polytechnic University, *Fall 2004,* teaching *Inform. Theory*

Lecturer at Texas A&M University, *academic year 1993/1994,* teaching *Elec. Circuit Theory.*

Lecturer at University of Sarajevo, Bosnia, *academic years 1986/1987 and 1987/1988,* teaching *Signal Processing I & II.*

Mentor for an NSF postdoctoral researcher at Bell Labs, *July 2010 – July 2012*

Mentor for two Bell Labs postdoctoral researchers, *May 1998 – May 2000* and *Jan. 2000 – Jan. 2001,* organizing and supervising their research projects.

Mentor for summer interns at Bell Labs and DIMACS, organizing and supervising research projects for up to three interns almost every summer since 1997.

Ph.D Thesis Committee Member, students at Rutgers (4), Columbia (1), EPFL (3), Aalborg (1), MIT (2), Toronto (1). – *various degrees of supervision/involvement*

Host Scientist for Bell Labs Global Science Scholars program for final-year high-school (2003–2005). Project design, lecturing, and a week-long supervision for visiting students.

PROFESSIONAL ACTIVITIES AND SERVICE

IEEE Information Theory Society Fellows Committee Member, 2016 – .

IEEE Koji Kobayashi Award Committee Member, 2014 –

IEEE Richard W. Hamming Medal Committee Member, 2013 –2016.

External Advisory Committee and **Industrial Board Member** for the NSF Science & Technology Center for Science of Information (NSF-STC-CSoI), 2013 –.

Best Paper Award Committee Member (3 times) for *IEEE Inform. Theory Society*

Board of Governors Member for the *IEEE Inform. Theory Soc.,* 2009 – 2011 and 2013 –.

DIMACS Council Member, 2003 –.

DIMACS Postdoctoral Committee Member, 2001 – 2011.

Co-Chair for DIMACS Special Focus on Cybersecurity, 2011 – 2015.

Co-Chair for DIMACS Special Focus on Comput. Inform. Th. and Coding, 2000 – 2005.

Guest Editor for the *Elsevier-PhyCom, Special Issue on Network Coding and its Applications to Wireless Communications*, March 2013.

Editorial Board Member *Springer Journal on Applicable Algebra in Engineering, Communication and Computing*, 2008 –.

Associate Editor for Coding Techniques, *IEEE Trans. on Inform. Theory*, 1997 – 2000.

Technical Program Co-Chair for the *2008 IEEE Inform. Theory Workshop* and *2012 International Symposium on Network Coding*

Workshop Co-Organizer
(upcoming, organization and funding granted based on a proposal):
Codes for Data Storage with Queues for Data Access, July, 2017 within the ICERM Women in Data Science and Mathematics Research Collaboration Workshop.

(past selected, organization and funding granted based on a proposal):
Dagstuhl Seminar on *Coding Theory in the Time of Big Data*, Schloss Dagstuhl, Aug. 2016, DIMACS Workshop on *Network Coding: the Next 15 Years*, Dec. 2015, BIRS Workshop on *Mathematical Coding Theory in Multimedia Streaming*, Banff, Oct. 2015. DIMACS Workshop on *Coding Theoretic Methods for Network Security*, April 2015, INFOCOM Workshop on *Communications and Networking Techniques for Contemporary Video*, April 2014, DIMACS Workshop and Working Group on Algorithms for Green Data Strage, Dec. 2013, Dagstuhl Seminar on Coding Theory, Schloss Dagstuhl, Aug. 2013, BIRS Workshop on *Applications of Matroid Theory and Combinatorial Optimization to Information and Coding Theory*, Banff, Aug. 2009, DIMACS Working Group and Workshop on *Coding, Streaming and Compressive Sensing* (March 2009), DIMACS Working Group on *Network Coding* Jan. 2005 and DIMACS Working Group and Workshop on *Theoretical Advances In Information Recording* (March 2004).

Special-Session Organizer *(selected, invited to organize):* Tutorials at *2015 IEEE Internat. Symp. on Inform. Theory (ISIT'15)*, "Information Theory & Coding for Contemporary Video," *2013 IEEE Inform. Theory Workshop (ITW'13)* in Seville, "Network Coding" at *2006 IEEE Comm. Theory Workshop (CTW'06)* in Puerto Rico, "Network Coding" at *2006 IEEE Inform. Theory Workshop (ITW'06)* in Chengdu, "Emerging Applications of Information Theory" at *2004 IEEE Inform. Theory Workshop (ITW'04)* in San Antonio.

Technical Program Committee Member for *(selected) IEEE Internat. Symp. on Inform. Theory (ISIT)*, 2000 – 2002, 2004, and 2008 – , *IEEE Inform. Theory Workshop (ITW)*, 2004 – 2009, *IEEE 2005 Int. Conf. Wireless Networks, Commun., and Mobile Comput.*, *Int. Workshop on Wireless Networks: Communication, Cooperation and Competition*, 2007, *Commun. Theory Symp. at IEEE Global Telecommun. Conf. (GLOBECOM) 2007–2008*, *Internat. Conf. on Comm. (ICC)* 2009.

Technical proof-reader for the *IEEE Transac. Inform. Theory*, 1990 – 1992.

Research Proposal Reviewer for NSF, BSF (United States-Israel Binational Science Foundation), Danish Research Council for Technology and Production Sciences, Research Grants Council of Hong Kong, SFI (Science Foundation of Ireland), UC MICRO Program (University of California Microelectronics Innovation and Computer Research Opportunities).

Affiliations with IEEE Inform. Theory Society, American Mathematical Society (AMS), NSF Center for Discrete Mathematics and Computer Science (DIMACS).

SELECTED BELL LABS SERVICE

Graduate Research Program for Women (GRPW) and **Cooperative Research Fellowship Program (CRFP) for Minorities and Women** committee member, 2002 – 2009.

Global Science Scholars committee member and host to student visitors, 2003–2005.

Afirmative Action Committee Member, 1996 – 1999.

Library Liaison, provided periodic recommendations for book ordering, collected and provided feedback on journal usage, 1996 – .

Seminars Sponsor, recruited and hosted speakers for several internal seminars and reading groups, 1996 – .

Committee Service, served on numerous hiring and various ad-hoc committees, 1995 – .

RECOGNITIONS

- *Distinguished Lecturer* for IEEE Information Theory Society, 2015 – 2016.

- *IEEE Fellow,* for contributions to coding theory and coding schemes for transmission and storage systems, *class of 2014.*

- *IEEE IT Society 2013 Padovani Lecturer,* a person whose research is considered to be of particular interest to students and postdocs is selected to give a special lecture at the yearly North American School of Information Theory. Lecture Ttile: "Secret Lives of Codes: From Theory to Practice and Back"

- *Best Paper Award* for the paper "Trade-off between cost and goodput in wireless: replacing transmitters with coding," (with M. Kim, M. Medard, MIT, J. Barros, Univ. of Porto, and T. Klien, Bell Labs) at *MONAMI'13.*

- *Honorable mention of the paper* "Asymptotic spectra of trapping sets in irregular LDPC code ensembles," (with O. Milenkovic, and P. Whiting, Bell Labs) at the *ICC 2006;* citation: "It provided an important contribution towards the statistical characterization and understanding of trapping sets, which are crucial to the assessment of error-floor effects in LDPC codes."

- *Distinguished Member of Technical Staff,* Bell Labs, March 2004.

- *IEEE Senior Member,* July 2003.

- Recognized as an *exceptional Bell Labs intern mentor* for the Summer 2003.

- IEEE *Referee Recognition* Award, 1998.

- Recognized in the 25th anniversary issue of *EE Times* as one of the 20 young engineers who are likely to make "significant contributions in the new millennium", Oct. 1997.

- Recognized for *teamwork at Bell Labs,* Dec. 1994.

- *Fouraker Fellowship* by EE Department, Texas A&M University, Sep. 1992 – Aug. 1993.

- *Electrical Powe Institute Fellowship* for the masters at EE Department, Texas A&M University, Jun. 1988 – Dec. 1989.

FUNDING

DIMACS Funds – awarded by the NSF and other funding agencies for *DIMACS Special Focus on Cybersecurity*, for workshops, seminar series, visitors, and postdocs from 2011 through 2015. *(Focus Co-Chair)*

NSF NeTS Medium Grant for *Collaborative Research: Secure Networking Using Network Coding* at the level of $882,357 (with Caltech, Purdue, and UT Austin), Sept. 2009 – Aug. 2013. *(Co-PI)*

DARPA IAMANET Contract for *PIANO: Principles for Intrinsically Assurable Network Operation*, with a multidisciplinary team from several universities (Caltech, MIT, Stanford, UMass, UT Austin), led by BAE, 2008. *(personal share $241,000 over 18 months)*

NSF NeTS-NBD Small Grant for *Coding and Transmission Schemes for Content Download* at the level of $569,000 (with UIUC and Rutgers), Sept. 2007 – Aug. 2010. *(Co-PI)*

NSF ITR Medium Grant for *Network Coding From Theory to Practice* at the level of $1.85 million (with Caltech, MIT, and UIUC), Sept. 2003 – Aug. 2008. *(Co-PI)*

DIMACS Funds – $205,000 budget awarded by the NSF and other funding agencies for *DIMACS Special Focus on Computational Information Theory and Coding* for workshops, seminar series, visitors, and postdocs from 2001 through 2004. *(Focus Co-Chair)*

NAE Research Grant – American recipient of the 1999 $10,000 Research Grant by the German-American Networking Program of the *National Academy of Engineering* and its German counterpart. (Elke Offer, TU Munich, was the German recipient.)

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SELECTED INVITED TUTORIAL/EXPOSITORY TALKS

1. "Network coding: a combinatorial framework and an open problem," *BIRS Workshop on Mathematics of Communications: Sequences, Codes and Designs*, Banff, January 2015.

2. "Basics of Network Coding," *BIRS Workshop on Applications of Matroid Theory and Combinatorial Optimization to Information and Coding Theory*, Banff, August 2009.

3. "Network Coding: Theory and Practice," *2007 IEEE Int. Symp. Inform. Theory (ISIT'07)*, Nice, France, June 2007.

4. "Hybrid ARQ: State of the Art," *2007 IEEE Int. Inform. Theory Workshop (ITW'07)*, Bergen, Norway, July 2007.

SELECTED PLENARY AND INVITED RESEARCH TALKS

1. *Queues for Data Access from Coded Distributed Storage*, 18th INFORMS Applied Probability Society Conference, Istanbul, July. 2015.

2. *Cloud Storage Space vs. Download Time for Large Files*, NYIT REU Program, New York, June 2015.

3. *Storage Codes and Data Retrieval*, Workshop on Coding: From Practice to Theory, The Simons Institute for the Theory of Computing, UC Berkeley, Feb. 2015.

4. *Codes for Storage with Queues for Access*, Workshop on Inform. Theory and Applic. (ITA), UCSD, Feb. 2015.

5. *Codes For All Seasons*, plenary talk at 2014 IEEE Workshop on Inform. Theory, Nov. 2014.

6. *Urns & Balls and Communications*, Dept. of Statistics, Univ. of Auckland, Nov. 2014.

7. *How Does Applied Math Become Applicable?* MIT Graduate Women (GW6) student group coffee hour seminar, May 2014.

8. *A coding Tale of a Tail at Scale*, Stanford, Apr. 2014.

9. *How Should We Code in Multicast to Diverse Users and What For?* Stanford, Apr. 2014, and University of Hawaii, Nov. 2014.

10. *Secret Lives of Codes: From Theory to Practice and Back* 2013 Padovani Lecture at the 2013 North American School of Information Theory, Purdue University, June 2013.

11. *Is Coding Beyond the Physical Layer Helpful in Content Centric Networking?*, Workshop on Inform. Theory and Applic. (ITA), UCSD Feb. 2013.

12. *Rateless Codes for Efficient Content Download in Highly Heterogeneous Scenarios*, Aalborg University, Sept. 2012.

13. *Pushing Codes into Clouds*, NSF Workshop on Communication Theory and Signal Processing in the Cloud Era, Berkeley, June 2012.

14. *Urns & Balls and Communications*, MIT Math Seminar, Apr. 2012.

15. *What are Good Coding Schemes for Multicast in Heterogeneous Wireless Networks?* International Zurich Seminar on Communications, March 2012.

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17. *Three Types of Redundancy Against Three Sources of Delay*, UIUC CSL Seminar, Apr. 2011.

18. *Double Dixie Cup Unicast*, UIUC CS Theory Seminar, Apr. 2011, Dagstuhl Seminar on Coding Theory, Nov. 2011.

19. *Content Preparation, Delivery, and Storage for Highly Heterogenous Networks*, EPFL, Oct. 2011, MIT EECS, Sept. 2011.

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21. *On Storing and Retrieving (Coded) Data in Mobile P2P Networks*, Isaac Newton Institute for Mathematical Sciences, special programme on *Stochastic Processes in Communication Sciences*, Cambridge, UK, April 2010.

22. *Coded Streaming in Heterogenous Networks*, BL/HHI Joint Workshop, June 2011, ENST Sept. 2011.

23. *Coding for Delay in Networks*, Texas A&M, Mar. 2011, ETIS/CNRS, Sept. 2011.

24. *Quantum Network Multicast and Coding*, International Seminar on Quantum Networking (Towards Quantum Internet, Madrid, June 2009.

25. *Two (Non)standardized Applications of Fountain Codes*, ETH Zürich, December 2008.

26. *Coding Technologies: Trends, Challenges, Opportunities and Applications*, Alcatel–Lucent Technical Academy, Antwerp, Belgium, July 2008.

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35. *Some Computer Science Problems in Network Coding*, 2004 IEEE Inform. Theory Workshop, San Antonio, Texas, Oct. 2004.

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37. *Frames in Quantum and Classical Information Theory*, EPFL, Lausanne, Switzerland, June 2004, Institute for Quantum Information Seminar, Caltech, Sept. 2003, Quantum Computing Seminar, Texas A&M University, April 2003, and DIMACS Workshop on Source Coding and Harmonic Analysis, May 2002

38. *Network Coding Based on Subtree Decomposition*, EE Seminar, Brooklyn Polytechnic University, Oct. 2003, and Information Science & Technology Seminar, Caltech, Sept. 2003.

39. *Hybrid ARQ in Wireless Networks*, Wireless Communications Lab Seminar, Texas A&M University, April 2003.

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CODING AND SIGNAL PROCESSING FOR MAGNETIC RECORDING SYSTEMS

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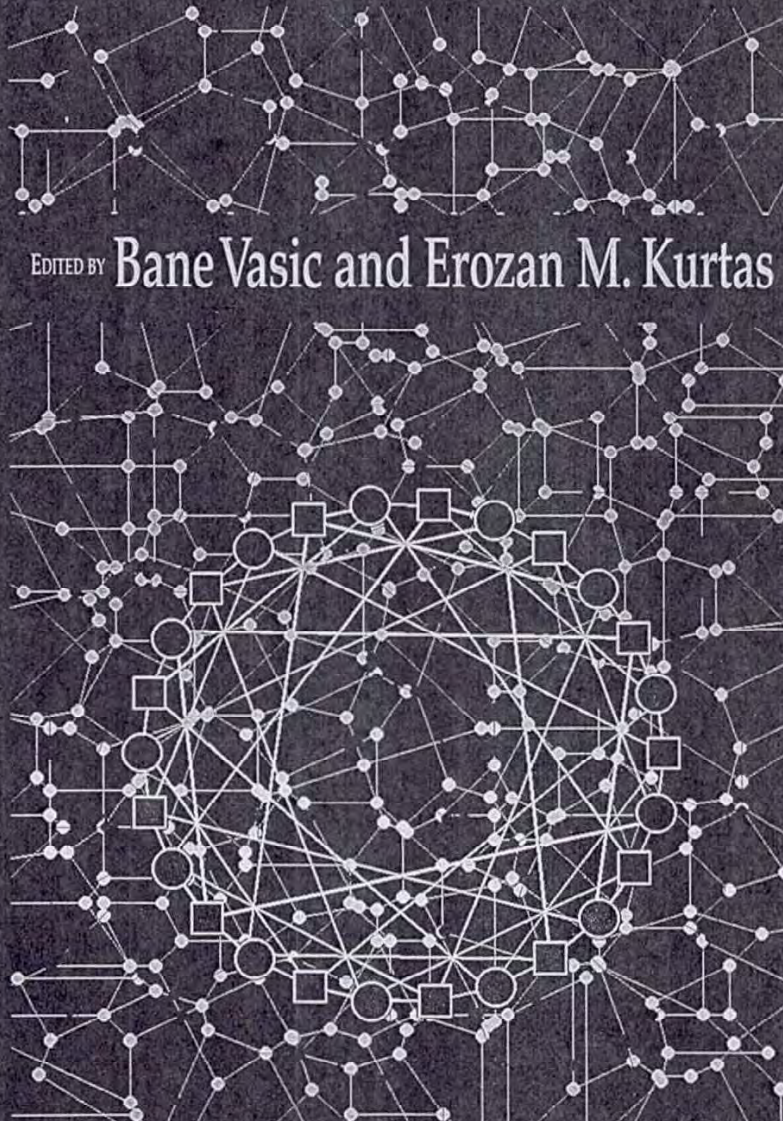
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Preface

A steady increase in recording densities and data rates of magnetic recording systems in the last 15 years is mostly due to advances in recording materials, read/write heads and mechanical designs. The role of signal processing and coding has been to make the best use of the capacity and speed potentials offered by these advances. As the recording technology matures, the hard disk drive "read channel" is becoming more and more advanced, reaching the point where it uses equally or even more complicated signal processing, coding and modulation algorithms than any other telecommunication channel and where, due to the speed, power consumption and cost requirements, the challenges in implementing new architectures and designs have been pushed to today's integrated circuit manufacturing technology limits.

This book reviews advanced coding and signal processing techniques, and architectures for magnetic recording read channels. In the most general terms, the *read channel* controls reading and writing the data to/from recording medium. The operations performed in the data channel include: *timing recovery, equalization, data detection, modulation coding/decoding* and limited *error control*. Besides this so-called *data channel*, a read channel also has a *servo channel* whose role is to sense head position information, and to regulate a proper position of the head above the track. The *error control* functions of a hard drive reside in a *controller*, a separate system responsible for a diverse set of electronic and mechanical functions to provide the user with a data storage system that implements the high-level behavior described by the magnetic hard drive's user interface. A trend in hard drive systems is to merge the functionalities of a read channel and controller into a so-called superchip. This book gives an in-depth treatment of all of these subsystems, with an emphasis on coding and signal processing aspects.

The book has six sections. Each section begins with a review of the underlying principles and theoretical foundations, describes the state-of-the-art systems, and ends with novel and most advanced techniques and methodologies.

The *first* section gives an introduction to recording systems. After a brief history of magnetic storage, we give basic principles of physics of longitudinal and perpendicular magnetic recording, and the physics of optical recording.

A modern hard disk drive comprises a recording medium in the form of a thin film on a surface of a disk, an inductive write head and a giant magneto-resistive read head. We describe and compare two types of recording mechanisms: (i) longitudinal recording in which the media magnetic anisotropy is oriented in the thin film plane, and (ii) perpendicular recording, where the magnetic anisotropy is aligned perpendicular to the film plane. We discuss a pulse response, the media noise powers, and the signal-to-noise ratio calculation for both types of recording. In a recording system, the playback noise originates from the head electronics and the media magnetization random patterns. Generally the medium noise is decomposed into the direct current (DC) remanent and the transition components. However, the transition jitter noise is dominant. In longitudinal recording, due to the random anisotropy dispersion, there always exist some levels of the DC remanent noise. However, in perpendicular recording, the loop full squareness is required to maintain thermal stability. Therefore, the DC remanent noise vanishes.

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The principles of optical recording are becoming increasingly important in hard drives because of a promise of a dramatic increase in the recording density that can be achieved by applying heat assisted magnetic recording (HAMR). In this approach, a laser beam at the spot where data are being recorded heats the magnetic medium. Heating the medium results in a reduction of the coercivity required to write the data to a level accessible by the recording head, while rapid subsequent cooling stabilizes the written data.

We give an introduction and history of magnetic recording heads, their evolution and importance, followed by a description of the write head for both longitudinal and perpendicular recording. We describe how various write head design parameters affect the written and read-back waveforms.

It is well understood that one of the key challenges to increasing areal density in magnetic recording systems is media noise suppression. Reducing the size of magnetic domains written to the medium, which has been the conventional approach to this problem, has a side effect whereby the magnetic domains become thermally unstable. To avoid this, so-called super paramagnetic effects media with increased coercivity are being used. However, the magnetic materials from which the head is made limit the fields that can be applied, and these limits are being approached. When the bit size is reduced, the signal-to-noise ratio is decreased, making the detection problem much more difficult.

The first section should equip the reader with a solid understanding of the physical principles of write and read back processes and constraints in designing a data storage system.

The *second* section gives communication and information theory tools necessary for a design and analysis of coding and signal processing techniques. We begin with modeling the recording channel. Design and analysis of coding and signal processing techniques require a suitable communications channel model for magnetic storage systems. Such a model should correctly reflect the essential physics of the read and write processes of magnetic recording, but must also provide a system level description that allows convenient design, analysis and simulation of the communications and signal processing techniques under study. We introduce common signal and noise models for recording channel models, statistical analysis tools, and partial response (PR) signaling as a method of controlling the intersymbol interference (ISI). We give models for medium noise, nonlinear distortion of magnetic transitions, and jitter. We show the effect of these noises on a number of conventional data detectors.

The first chapter on error control codes introduces finite fields and error correction capabilities of algebraically constructed and decoded codes. We introduce finite fields, define linear codes over finite fields, discuss the relation between minimum distance and error correction capability of a code, introduce cyclic codes and Reed-Solomon (RS) codes and explain in detail their encoding and decoding algorithms. The second chapter gives a theoretical foundation of message-passing algorithms and linear time sub-optimal probabilistic decoding algorithms that achieve near optimum performance. Recently such algorithms have attracted tremendous interest and have been investigated as an alternative decoding scheme for new generation of read channels.

The next chapter reviews sofic systems, the theoretical foundation of constrained (or modulation) codes that are used to translate an arbitrary sequence of user data to a channel sequence with special properties required by the physics of the recording medium. Modulation coding in a read channel serves a variety of important roles. Generally speaking, modulation coding eliminates those sequences from a recorded stream that would degrade the error performance, for example, long runs of consecutive symbols that impact the timing recovery or sequences that result in signals on a small Euclidian distance.

The section ends with a view of recording channels from the information theory standpoint, and a chapter summarizing techniques for bounding the capacity of a PR channel. Such results are very important in that they provide theoretical limits on the performance of practical coding/decoding schemes. Since recording channels can be modeled as ISI channels with binary inputs, we first present the capacity of the general ISI channels with additive white Gaussian noise, which is achieved by correlated Gaussian inputs. When taking the constraint of binary inputs into account, no closed-form solutions exist; however, several upper and lower bounds are derived. Monte-Carlo simulation techniques to estimate the achievable information rates of ISI channels are also described. The simulation-based techniques can be extended

further to compute the achievable information rates of the magnetic recording channels with media noise, present in high density recording systems.

The *third* section begins with a description of physical and logical organization of data in various recording systems and methods of increasing recording density. Then we give a cross section of the state-of-the-art read channels and explain their subsystems. We explain organization of data on the disc tracks, servo sectors and data sectors, seeking and tracking operations, and phase and frequency acquisition. The section on servo information detection explains sensing radial information and read channel subsystem used to perform this operation.

The image of a magnetic storage device presented to a host computer by a standard interface is an abstraction quite different from the reality of the actual mechanisms providing the means for storing data. The device's presentation via the interface is that of a linear and contiguous array of data blocks that are trivially read from and stored in a defect-free space of logical blocks. This image belies the elaborate choreography of signal processing, coding, data structure, control systems, and digital electronics technologies that is exercised with every block of data moved to and from the magnetic media. The function of a hard drive controller is to implement and coordinate the operation of these disparate technologies so as to map the behavior of the physical storage device into the abstract storage model defined by the drive's interface to the host computer. The chapter on hard drive controllers describes some of the architectures implemented by current hard drive controllers to serve this function.

The *fourth* section is concerned with modulation and error control coding for read channels. It starts with an introduction of modulation coding techniques. The first class of constraints discussed is the runlength constraint. It is the most common constraint in hard drives and is imposed to bound the minimal or maximal lengths of consecutive like channel symbols in order to improve timing recovery, reduce intersymbol interference in channels with excess bandwidth and reduce transition noise in nonlinear media. We also discuss other important classes of codes: namely maximum transition run (MTR) coding and spectrum shaping codes.

Maximum transition run constraint, which limits the number of consecutive transitions, improves minimum distance properties of recorded sequences for a variety of channel responses applicable to recording systems. The channel is characterized by types of error events and their occurrence probability, and pairs of coded sequences that produce these errors are determined. This ambiguity is resolved by simply enforcing a constraint in the encoder, which prevents one or both of the coded sequences.

The first type of spectrum shaping codes considered here is codes with higher order spectral zero at zero frequency. Another class of spectrum shaping codes was invented to support the use of frequency multiplexing technique for track following. Both techniques require the existence of spectral nulls at nonzero frequencies. The third class of spectrum shaping codes is those that give rise to spectral lines. Their purpose is to give the reference information to the head positioning servo system.

We continue with modulation codes with error correcting capability and convolutional codes for PR channels designed to increase the minimum Euclidean distance. The section continues with an overview of the research in new classes of modulation codes and detection techniques: capacity approaching codes for partial response channels, coding and detection for multitrack systems and two-dimensional PR equalization and error control.

The *fifth* section gives an in depth treatment of the signal processing techniques for read channels. In PR channels a clock is used to sample the analog waveform to provide discrete samples to symbol-by-symbol and sequence (Viterbi) detectors. Improper synchronization of these discrete samples with respect to those expected by the detectors for a given partial response will degrade the eventual bit error rate (BER) of the system. The goal of adaptive timing recovery is to produce samples for a sequence detector that are at the desired sampling instances for the partial response being used. We review the basics of timing recovery as well as commonly used algorithms for timing recovery in magnetic recording channels, and we introduce a novel technique called interpolated timing recovery. We also introduce adaptive equalization architectures for partial response channels.

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Data in a disk drive is stored in concentric tracks, and when a given track needs to be accessed, the head assembly moves the read/write head to the appropriate radial location. This positioning of the head on top of a given track and maintaining a proper position is achieved by the use of a feedback servo system. The servo system analysis includes a chapter on head position estimation and a chapter on servo signal processing. The first chapter reviews methods to estimate the head position, which is uniquely determined from the radial and angular position of the head with respect to a disk surface.

The second chapter gives an overview of servo channel signal processing using examples of techniques employed in practical servo channels. It reviews how detectors for PR channels can be used to improve the detection of the servo data with time varying Viterbi detector matched to a servo code.

The first article on data detection gives the basic detection principles and techniques. The second one describes signal dependent detectors. It introduces the concepts and tools necessary for performing optimal detection for ISI channels when the noise is not AWGN and signal dependent. We describe the techniques to design both hard and soft decision detectors, in particular the so-called K-step, noise prediction and signal dependent noise prediction detectors.

We end this section with an overview of traditional architectures for signal processing in magnetic read-write channels. Today's dominant architecture, where the majority of signal processing is performed in the digital domain is analyzed in detail. The main challenges and alternatives for implementation of major building blocks are discussed. As the previous chapters had covered the theoretical aspects of operation of these blocks in considerable detail, most of the discussion in this chapter focuses on architectures and techniques that are used in practical read channels. The techniques for implementing iterative decoders as possible future detectors are presented at the end of this chapter.

We conclude this book by the review of new trends in coding, namely iterative decoding, given in the *sixth* section. Iterative coding techniques that improve the reliability of input-constrained ISI channels have recently driven considerable attention in magnetic recording applications.

It has been shown that randomly selected codes of very large block lengths can achieve channel capacity. One way of obtaining a large block length code is concatenating two simple codes so that the encoding and the decoding of the overall code are less complex. Turbo codes represent a way of concatenating two simple codes to obtain codes that achieve the channel capacity. In turbo coding, two systematic recursive constituent convolutional encoders are concatenated in parallel via a long interleaver. For decoding, a practical suboptimal iterative decoding algorithm is employed. The first chapter in this section describes the turbo coding principle in detail.

Drawing inspiration from the success of turbo codes, several authors have considered iterative decoding architectures for coding schemes combining concatenation of outer block, convolutional or turbo encoder with a rate one code representing the channel. Such an architecture is equivalent to a serial concatenation of codes with the inner code being the ISI channel. The decoding of such concatenated codes is facilitated using the concept of codes on graphs.

We continue with an introduction to low-density parity check (LDPC) codes, and describe single-parity check turbo product codes and well-structured LDPC codes. We describe several classes of combinatorially constructed LDPC codes along with their performance PR channels. Due to their mathematical structure, and unlike random codes, these LDPC codes can lend themselves to very low complexity implementations. We describe constructions of regular Gallager LDPC codes based on combinatorial designs, finite geometries and finite lattices.

Two constructions of single-parity check (SPC) codes are considered, one in the form of turbo codes where two SPC branches are concatenated in parallel using a random interleaver, and the other in the form of product codes where multiple SPC codewords are arranged row-wise and column-wise in a two-dimensional array. Despite their small minimum distances, concatenated SPC codes, when combined with a precoded PR channel, possess good distance spectra.

The last chapter introduces turbo coding for multi-track recording channels. It describes a modified *maximum a posteriori* (MAP) detector for the multi-track systems with deterministic or random ITI.

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The turbo equalization and the iterative decoding are performed by exchanging the soft information between the channel MAP detector and the outer soft-input soft-output decoder that corresponds to the outer encoder. The resulting system performance is very close to the information theoretical limits.

We would like to end this preface by acknowledging the excellent work done by the contributors. Also it is a pleasure to acknowledge the financial support from the National Science Foundation (Grant CCR 020859) and the continuous support from the Information Storage Industry Consortium and Seagate Technologies.

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11

Modulation Codes for Storage Systems

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11.1 Introduction

Modulation codes are used to constrain the individual sequences that are recorded in data storage channels, such as magnetic or optical disk or tape drives. The constraints are imposed in order to improve the detection capabilities of the system. Perhaps the most widely known constraints are the runlength limited (RLL(d, k)) constraints, in which 1s are required to be separated by at least d and no more than k 0s. Such constraints are useful in data recording channels that employ peak detection: waveform peaks, corresponding to data ones, are detected independently of one another. The d-constraint helps to increase linear density while mitigating intersymbol interference, and the k-constraint helps to provide feedback for timing and gain control.

Peak detection was widely used until the early 1990s. While it is still used today in some magnetic tape drives and some optical recording devices, most high density magnetic disk drives now use a form of maximum likelihood (Viterbi) sequence detection. The data recording channel is modeled as a linear, discrete-time, communications channel with intersymbol interference (ISI), described by its transfer function and white Gaussian noise. The transfer function is often given by $h(D) = (1 - D)(1 + D)^N$, where N depends on and increases with the linear recording density.

Broadly speaking, two classes of constraints are of interest in today's high density recording channels: (1) constraints for improving timing and gain control and simplifying the design of the Viterbi detector for the channel, and (2) constraints for improving noise immunity. Some constraints serve both purposes.

Constraints in the first class usually take the form of a PRML (G, I) constraint: the maximum run of 0s is G and the maximum run of 0s, within each of the two substrings defined by the even indices and odd indices, is I. The G-constraint plays the same role as the k-constraint in peak detection, while the I-constraint enables the Viterbi detector to work well within practical limits of memory.

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Constraints in the second class eliminate some of the possible recorded sequences in order to increase the minimum distance between those that remain or eliminate the possibility of certain dominant error events. This general goal does not specify how the constraints should be defined, but many such constraints have been constructed [20] and the references therein for a variety of examples. Bounds on the capacities of constraints that avoid a given set of error events have been given in [26].

Until recently, the only known constraints of this type were the matched-spectral-null (MSN) constraints. They describe sequences whose spectral nulls match those of the channel and therefore increase its minimum distance. For example, a set of DC-balanced sequences (i.e., sequences of ± 1 whose accumulated digital sums are bounded) is an MSN constraint for the channel with transfer function $h(D) = 1 - D$, which doubles its minimum distance [18].

During the past few years, significant progress has been made in defining high capacity distance enhancing constraints for high density magnetic recording channels. One of the earliest examples of such a constraint is the maximum transition run (MTR) constraint [28], which constrains the maximum run of 1s. We explain the main idea behind this type of distance-enhancing codes in Section 11.3.

Another approach to eliminating problematic error events is that of parity coding. Here, a few bits of parity are appended to (or inserted in) each block of some large size, typically 100 bits. For some of the most common error events, any single occurrence in each block can be eliminated. In this way, a more limited immunity against noise can be achieved with less coding overhead [5].

Coding for more realistic recording channel models that include colored noise and intertrack interference are discussed in Section 11.4. We point out that different constraints which avoid the same prescribed set of differences may have different performance on more realistic channels. This makes some of them more attractive for implementation.

For a more complete introduction to this subject, we refer the reader to any one of the many expository treatments, such as [16], [17], or [24].

11.2 Constrained Systems and Codes

Modulation codes used in almost all contemporary storage products belong to the class of constrained codes. These codes encode random input sequences to sequences that obey the constraint of a labeled directed graph with a finite number of states and edges. The set of corresponding constrained sequences is obtained by reading the labels of paths through the graph. Sets of such sequences are called constrained systems or constraints. Figure 11.1 and Figure 11.2 depict graph representations of an RLL constraint and a DC-balanced constraint.
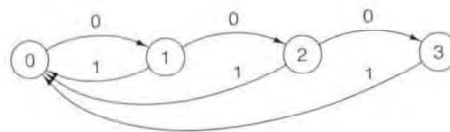

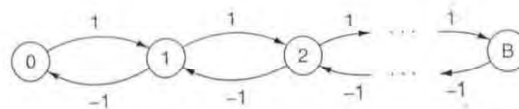FIGURE 11.1   RLL $(1, 3)$ constraint.

FIGURE 11.2   DC-balanced constraint.

Of special interest are those constraints that do not contain (globally or at certain positions) a finite number of finite length strings. These systems are called systems of finite type (FT). An FT system X over alphabet $\mathcal{A}$ can always be characterized by a finite list of forbidden strings $\mathcal{F} = \{w_1, \ldots, w_N\}$ of symbols in $\mathcal{A}$. Defined this way, FT systems will be denoted by $X_{\mathcal{F}}^{\mathcal{A}}$. The RLL constraints form a prominent class of FT constraints, while DC-balanced constraints are typically not FT.

Design of constrained codes begins with identifying constraints, such as those described in Section 11.1, that achieve certain objectives. Once the system of constrained sequences is specified, information bits are translated into sequences that obey the constraints via an *encoder*, which usually has the form of a finite-state machine. The actual set of sequences produced by the encoder is called a constrained code and is often denoted C. A *decoder* recovers user sequences from constrained sequences. While the decoder is also implemented as a finite-state machine, it is usually required to have a stronger property, called sliding-block decodablility, which controls error propagation [24].

The maximum rate of a constrained code is determined by *Shannon capacity*. The Shannon capacity or simply *capacity* of a constrained system, denoted by C, is defined as

$$C = \lim_{n \to \infty} \frac{\log_2 N(n)}{n}$$

where $N(n)$ is the number of sequences of length n. The capacity of a constrained system represented by a graph G can be easily computed from the *adjacency matrix* (or *state transition matrix*) of G (provided that the labeling of G satisfies some mildly innocent properties). The adjacency matrix of G with r states and a_{ij} edges from state i to state j, $1 \le i, j \le r$, is the $r \times r$ matrix $A = A(G) = \{a_{ij}\}_{r \times r}$. The Shannon capacity of the constraint is given by

$$C = \log_2 \lambda(A)$$

where $\lambda(A)$ is the largest real eigenvalue of A.

The *state-splitting algorithm* [1] (see also [24]) gives a general procedure for constructing constrained codes at any rate up to capacity. In this algorithm, one starts with a graph representation of the desired constraint and then transforms it into an encoder via various graph-theoretic operations including splitting and merging of states. Given a desired constraint and a desired rate $p/q \le C$, one or more rounds of state splitting are performed; the determination of which states to split and how to split them is governed by an approximate eigenvector, that is, a vector $\mathbf{x}$ satisfying $A^q \mathbf{x} \ge 2^p \mathbf{x}$.

There are many other very important and interesting approaches to constrained code construction — far too many to mention here. One approach combines state-splitting with look-ahead encoding to obtain a very powerful technique which yields competent codes [14]. Another approach involves variable-length and time-varying variations of these techniques [2, 13]. Many other effective coding constructions are described in the monograph [17].

For high capacity constraints, graph transforming techniques, such as the state-splitting algorithm, may result in encoder/decoder architectures with formidable complexity. Fortunately, a block encoder/decoder architecture with acceptable implementation complexity for many constraints can be designed by well-known enumerative [6], and other combinatorial [32] as well as heuristic techniques [25].

Translation of constrained sequences into the channel sequences depends on the modulation method. Saturation recording of binary information on magnetic medium is accomplished by converting an input stream of data into a spatial stream of bit cells along a track where each cell is fully magnetized in one of two possible directions, denoted by 0 and 1. There are two important modulation methods commonly used on magnetic recording channels: *non-return-to-zero* (NRZ) and *modified non-return-to-zero* (NRZI). In NRZ modulation, the binary digits 0 and 1 in the input data stream correspond to 0 and 1 directions of cell magnetizations, respectively. In NRZI modulation, the binary digit 1 corresponds to a magnetic transition between two bit cells, and the binary digit 0 corresponds to no transition. For example, the channel constraint which forbids transitions in two neighboring bit-cells, can be accomplished by either $\mathcal{F} = \{11\}$ NRZI constraint or $\mathcal{F} = \{101, 010\}$ NRZ constraint. The graph representation of these two constraints is shown in Figure 11.3. The NRZI representation is in this case simpler.
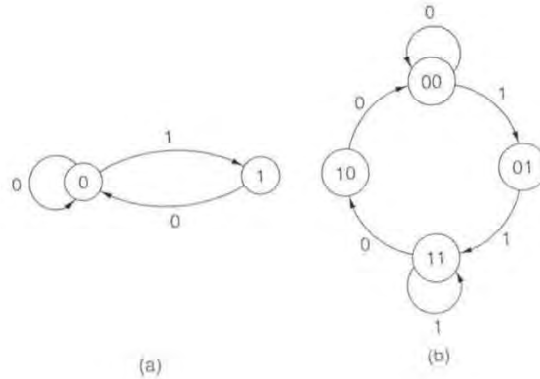
FIGURE 11.3   Two equivalent constraints: (a) $\mathcal{F} = \{11\}$ NRZI, and (b) $\mathcal{F} = \{101, 010\}$ NRZ.

11.3   Constraints for ISI Channels

We discuss a class of codes known as *codes which avoid specified differences*. This is the only class of distance enhancing codes used in commercial magnetic recording systems. There are two main reasons for this: these codes simplify the channel detectors relative to the uncoded channel and even high rate codes in this class can be realized by low complexity encoders and decoders.

11.3.1   Requirements

A number of papers have proposed using constrained codes to provide coding gain on channels with high ISI (see [4, 10, 20, 28]). The main idea of this approach can be described as follows [20]. Consider a discrete-time model for the magnetic recording channel with possibly constrained input $a = \{a_n\} \in \mathcal{C} \subseteq \{-1, 1\}^\infty$, impulse response $\{h_n\}$, and output $y = \{y_n\}$ given by

$$y_n = \sum_m a_m h_{n-m} + \eta_n \qquad (11.1)$$

where $h(D) = \sum_n h_n D^n = (1 - D)(1 + D)^3$ (E^{2}PR4) or $h(D) = \sum_n h_n = (1 - D)(1 + D)^4$ (E^{3}PR4), η_n are independent Gaussian random variables with zero mean and variance σ^2. The quantity $1/\sigma^2$ is referred to as the signal-to-noise ratio (SNR). The minimum distance of the uncoded channel (Equation 11.1) is

$$d_{min}^2 = \min_{\epsilon(D) \neq 0} \|h(D)\epsilon(D)\|^2$$

where $\epsilon(D) = \sum_{i=0}^{l-1} \epsilon_i D^i$, $(\epsilon_i \in \{-1, 0, 1\}, \epsilon_0 = 1, \epsilon_{l-1} \neq 0)$ is the polynomial corresponding to a normalized input error sequence $\epsilon = \{\epsilon_i\}_{i=0}^{l-1}$ of length l, and the squared norm of a polynomial is defined as the sum of its squared coefficients. The minimum distance is bounded from above by $\|h(D)\|^2$, denoted by

$$d_{MFB}^2 = \|h(D)\|^2 \qquad (11.2)$$

This bound is known as the *matched-filter bound* (MFB), and is achieved when the error sequence of length $l = 1$, that is, $\epsilon(D) = 1$, is in the set

$$\arg \min_{\epsilon(D) \neq 0} \|h(D)\epsilon(D)\|^2 \qquad (11.3)$$

For channels that fail to achieve the MFB, that is, for which $d_{min}^2 < \|h(D)\|^2$, any error sequences $\epsilon(D)$ for which

$$d_{min}^2 \leq \|h(D)\epsilon(D)\|^2 < \|h(D)\|^2 \qquad (11.4)$$

are of length $l \geq 2$ and may belong to a constrained system $X_{\mathcal{L}}^{\{-1,0,1\}}$, where $\mathcal{L}$ is an appropriately chosen finite list of forbidden strings.

For code $\mathcal{C}$, we write the set of all admissible nonzero error sequences as

$$\mathcal{E}(\mathcal{C}) = \{\epsilon \in \{-1, 0, 1\}^{\infty}|$$
$$\epsilon \neq 0, \epsilon = (a - b)/2, \ a, b \in \mathcal{C}\}$$

Given the condition $\mathcal{E}(\mathcal{C}) \subseteq X_{\mathcal{L}}^{\{-1,0,1\}}$, we seek to identify the least restrictive finite collection $\mathcal{F}$ of blocks over the alphabet $\{0, 1\}$ so that

$$\mathcal{C} \subseteq X_{\mathcal{F}}^{\{0,1\}} \implies \mathcal{E}(\mathcal{C}) \subseteq X_{\mathcal{L}}^{\{-1,0,1\}} \qquad (11.5)$$

11.3.2 Definitions

A constrained code is defined by specifying $\mathcal{F}$, the list of forbidden strings for code sequences. Prior to that one needs to first characterize error sequences that satisfy Equation 11.4 and then specify $\mathcal{L}$, the list of forbidden strings for error sequences. Error event characterization can be done by using any of the methods described by Karabed et al. [20]. Specification of $\mathcal{L}$ is usually straightforward.

A natural way to construct a collection $\mathcal{F}$ of blocks forbidden in code sequences based on the collection $\mathcal{L}$ of blocks forbidden in error sequences is the following. From the above definition of error sequences $\epsilon = \{\epsilon_i\}$ we see that $\epsilon_i = 1$ requires $a_i = 1$ and $\epsilon_i = -1$ requires $a_i = 0$, that is, $a_i = (1 + \epsilon_i)/2$. For each block $w_{\mathcal{E}} \in \mathcal{L}$, construct a list $\mathcal{F}_{w_{\mathcal{E}}}$ of blocks of the same length l according to the rule:

$$\mathcal{F}_{w_{\mathcal{E}}} = \{w_C \in \{-1, 1\}^l|$$
$$w_C^i = (1 + w_{\mathcal{E}}^i)/2 \text{ for all } i \text{ for which } w_{\mathcal{E}}^i \neq 0\}$$

Then the collection $\mathcal{F}$ obtained as $\mathcal{F} = \cup_{w_{\mathcal{E}} \in \mathcal{L}} \mathcal{F}_{w_{\mathcal{E}}}$ satisfies requirement (Equation 11.5). However, the constrained system $X_{\mathcal{F}}^{\{0,1\}}$ obtained this way may not be the most efficient. (Bounds on the achievable rates of codes which avoid specified differences were found recently in [26].)

We illustrate the above ideas on the example of the E^{2}PR4 channel. Its transfer function is $h(D) = (1 - D)(1 + D)^3$, and its MFB is $\|(1 - D)(1 + D)^3 \cdot 1\|^2 = 10$. The error polynomial $\epsilon(D) = 1 - D + D^2$ is the unique error polynomial for which $\|(1 - D)(1 + D)^3\epsilon(D)\|^2 = 6$, and the error polynomials $\epsilon(D) = 1 - D + D^2 + D^5 - D^6 + D^7$ and $\epsilon(D) = \sum_{i=0}^{l-1}(-1)^i D^i$ for $l \geq 4$ are the only polynomials for which $\|(1 - D)(1 + D)^3\epsilon(D)\|^2 = 8$ (see [20]).

It is easy to show that these error events are not in the constrained error set defined by the list of forbidden error strings $\mathcal{L} = \{+ - + 0\,0, + - + -\}$, where $+$ denotes 1 and $-$ denotes -1. To see that, note that an error sequence that does not contain the string $+ - + 0\,0$ cannot have error polynomials $\epsilon(D) = 1 - D + D^2$ or $\epsilon(D) = 1 - D + D^2 + D^5 - D^6 + D^7$, while an error sequence that does not contain string $+ - + -$ cannot have an error polynomial of the form $\epsilon(D) = \sum_{i=0}^{l-1}(-1)^i D^i$ for $l \geq 4$. Therefore, by the above procedure of defining the list of forbidden code strings, we obtain the $\mathcal{F} = \{+ - +\}$ NRZ constraint. Its capacity is about 0.81, and a rate 4/5 code into the constraint was first given in [19].

In [20], the following approach was used to obtain several higher rate constraints. For each of error strings in $\mathcal{L}$, we write all pairs of channel strings whose difference is the error string. To define $\mathcal{F}$, we look for the longest string(s) appearing in at least one of the strings in each channel pair. For the example above and the $+ - + 0\,0$ error string, a case-by-case analysis of channel pairs is depicted in Figure 11.4. We can distinguish two types (denoted by A and B in the figure) of pairs of code sequences involved in forming an error event. In a pair of type A, at least one of the sequences has a transition run of length 4. In a pair of type B, both sequences have transition runs of length 3, but for one of them the run starts at an even
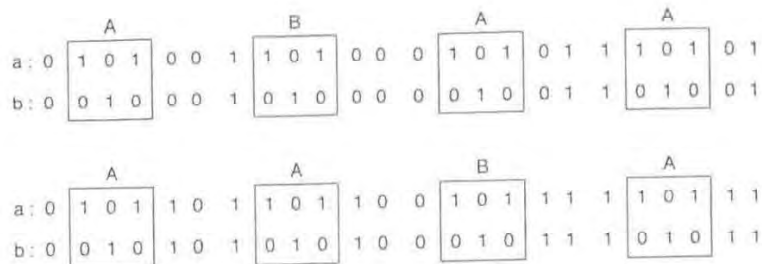
FIGURE 11.4   Possible pairs of sequences for which error event $+ - +00$ may occur.

position and for the other at an odd position. This implies that an NRZI constrained system that limits the run of 1s to 3 when it starts at an odd position, and to 2 when it starts at an even position, eliminates all possibilities shown bold-faced in Figure 11.4. In addition, this constraint eliminates all error sequences containing the string $+-+-$. The capacity of the constraint is about 0.916, and rate 8/9 block codes with this constraint has been implemented in several commercial read channel chips. More about the constraint and the codes can be found in [4, 10, 20, 28].

11.4   Channels with Colored Noise and Intertrack Interference

Magnetic recording systems always operate in the presence of colored noise intertrack interference, and data dependent noise. Codes for these more realistic channel models are studied in [27]. Below, we briefly outline the problem.

Data recording and retrieval process is usually modeled as a linear, continuous-time, communications channel described by its Lorentzian step response and additive white Gaussian noise. The most common discrete-time channel model is given by Equation 11.1. Magnetic recording systems employ channel equalization to the most closely matching transfer function $h(D) = \sum_n h_n D^n$ of the form $h(D) = (1 - D)(1 + D)^N$. This equalization alters the spectral density of the noise, and a better channel model assumes that the η_n in Equation 11.1 are identically distributed, Gaussian random variables with zero mean, variance σ^2, and normalized cross-correlation $E\{\eta_n\eta_k\}/\sigma^2 = \rho_{n-k}$.

In practice, there is always intertrack interference (ITI), that is, the read head picks up magnetization from an adjacent track. Therefore, the channel output is given by

$$y_n = \sum_m a_m h_{n-m} + \sum_m x_m g_{n-m} + \eta_n \tag{11.6}$$

where $\{g_n\}$ is the discrete-time impulse response of the head to the adjacent track, and $x = \{x_n\} \in C$ is the sequence recorded on that track. We assume that the noise is white.

In the ideal case (Equation 11.1), the probability of detecting b given that a was recorded is equal to $Q(d(\epsilon)/\sigma)$, where $d(\epsilon)$ is the distance between a and b given by

$$d^2(\epsilon) = \sum_n \left(\sum_m \epsilon_m h_{n-m} \right)^2 \tag{11.7}$$

Therefore, a lower bound, and a close approximation for small σ, to the minimum probability of an error-event in the system is given by $Q(d_{min,C}/\sigma)$, where

$$d_{min,C} = \min_{\epsilon \in \mathcal{E}_C} d(\epsilon)$$

is the channel minimum distance of code C. We refer to

$$d_{min} = \min_{\epsilon \in \{-1,0,1\}^\infty} d(\epsilon) \tag{11.8}$$

as the minimum distance of the uncoded channel, and to the ratio $d_{min,C}/d_{min}$ as the gain in distance of code C over the uncoded channel.

In the case of colored noise, the probability of detecting b given that a was recorded equals to $Q(\Delta(\epsilon)/\sigma)$, where $\Delta(\epsilon)$ is the distance between a and b given by

$$\Delta^2(\epsilon) = \frac{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]^2}{\sum_n \sum_k \left(\sum_m \epsilon_m h_{n-m}\right) \rho_{n-k} \left(\sum_m \epsilon_m h_{k-m}\right)}$$

Therefore a lower bound to the minimum probability of an error-event in the system is given by $Q\left(\Delta_{min,C}/\sigma\right)$, where

$$\Delta_{min,C} = \min_{\epsilon \in \mathcal{E}_C} \Delta(\epsilon)$$

In the case of ITI (Equation 11.6), we are interested in the probability of detecting sequence b given that sequence a was recorded on the track being read and sequence x was recorded on an adjacent track. This probability is

$$Q(\delta(\epsilon, x)/\sigma),$$

where $\delta(\epsilon, x)$ is the distance between a and b in the *presence* of x given by [30]

$$\delta^2(\epsilon, x) = \frac{1}{\left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2\right]} \left[\sum_n \left(\sum_m \epsilon_m h_{n-m}\right)^2 + \sum_n \left(\sum_m x_m g_{n-m}\right)\left(\sum_m \epsilon_m h_{n-m}\right)\right]^2$$

Therefore a lower bound to the minimum probability of an error-event in the system is proportional to $Q(\delta_{min,C}/\sigma)$, where

$$\delta_{min,C} = \min_{\epsilon \neq 0, x \in C} \delta(\epsilon, x)$$

Distance $\delta_{min,C}$ can be bounded as follows [30]:

$$\delta_{min,C} \geq (1 - M)d_{min,C} \tag{11.9}$$

where $M = \max_{n, x \in C} \sum_m x_m g_{n-m}$, that is, M is the maximum absolute value of the interference. Note that $M = \sum_n |g_n|$. We will assume that $M < 1$. The bound is achieved if and only if there exists an ϵ, $d(\epsilon) = d_{min,C}$, for which $\sum_m \epsilon_m h_{n-m} \in \{-1, 0, 1\}$ for all n, and there exists an $x \in C$ such that $\sum_m x_m g_{n-m} = \mp M$ whenever $\sum_m \epsilon_m h_{n-m} = \pm 1$.

11.5 An Example

There are codes that provide gain in minimum distance on channels with ITI and colored noise, but not on the AWGN channel with the same transfer function. This is best illustrated using the example of the partial response channel with the transfer function $h(D) = (1 - D)(1 + D)^2$ known as EPR4. It is well known that for the EPR4 channel $d_{min}^2 = 4$. Moreover, as discussed in Section 11.3, the following result holds:

Proposition 11.1 Error events $\epsilon(D)$ such that

$$d^2(\epsilon) = d_{min}^2 = 4$$

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take one of the following two forms:

$$\epsilon(D) = \sum_{j=0}^{k-1} D^{2j}, \quad k \geq 1$$

or

$$\epsilon(D) = \sum_{i=0}^{l-1} (-1)^i D^i, \quad l \geq 3$$

Therefore, an improvement of error-probability performance can be accomplished by codes which eliminate the error sequences ϵ containing the strings $-1 + 1 - 1$ and $+1 - 1 + 1$. Such codes were extensively studied in [20].

In the case of ITI Equation 11.6, we assume that the impulse response to the reading head from an adjacent track is described by $g(D) = \alpha H(D)$, where the parameter α depends on the track to head distance. Under this assumption, the bound (Equation 11.9) gives $\delta_{min}^2 \geq d_{min}^2 (1 - 4\alpha)^2$. The following result was shown in [30]:

Proposition 11.2   Error events $\epsilon(D)$ such that

$$\min_{x \in C} \delta^2(\epsilon, x) = \delta_{min}^2 = d_{min}^2 (1 - 4\alpha)^2 = 4(1 - 4\alpha)^2$$

take the following form:

$$\epsilon(D) = \sum_{i=0}^{l-1} (-1)^i D^i, \quad l \geq 5$$

For all other error sequences for which $d^2(\epsilon) = 4$, we have $\min_{x \in C} \delta^2(\epsilon, x) = 4(1 - 3\alpha)^2$.

Therefore, an improvement in error-probability performance of this channel can be accomplished by limiting the length of strings of alternating symbols in code sequences to four. For the NRZI type of recording, this can be achieved by a code that limits the runs of successive ones to three. Note that the set of minimum distance error events is smaller than in the case with no ITI. Thus performance improvement can be accomplished by higher rate codes which would not provide any gain on the ideal channel.

Channel equalization to the EPR4 target introduces cross-correlation among noise samples for a range of current linear recording densities (see [27] and references therein). The following result was obtained in [27]:

Proposition 11.3   Error events $\epsilon(D)$ such that

$$\Delta^2(\epsilon) = \Delta_{min}^2$$

take the following form:

$$\epsilon(D) = \sum_{i=0}^{l-1} (-1)^i D^i, \quad l \geq 3, \quad l \text{ odd}$$

Again, the set of minimum distance error events is smaller than in the ideal case (white noise), and performance improvement can be provided by codes which would not give any gain on the ideal channel. For example, since all minimum distance error events have odd parity, a single parity check code can be used.

11.6   Future Directions

11.6.1   Soft-Output Decoding of Modulation Codes

Detection and decoding in magnetic recording systems is organized as a concatenation of a channel detector, an inner decoder, and an outer decoder, and as such should benefit from techniques known as erasure and list decoding. To declare erasures or generate lists, the inner decoder (or channel detector) needs to assess symbol/sequence reliabilities. Although the information required for this is the same one necessary for producing a single estimate, some additional complexity is usually required. So far, the predicted gains for erasure and list decoding of magnetic recording channels with additive white Gaussian noise were not sufficient to justify the increasing complexity of the channel detector and inner and outer decoder. However, this is not the case for systems employing new magneto-resistive reading heads, for which an important noise source, thermal asperities, is to be handled by passing erasure flags from the inner to the outer decoder.

In recent years, one more reason for developing simple soft-output channel detectors has surfaced. The success of turbo-like coding schemes on memoryless channels has sparked the interest in using them as modulation codes for ISI channels. Several recent results show that the improvements in performance turbo codes offer when applied to magnetic recording channels at moderate linear densities are even more dramatic than in the memoryless case [12, 29]. The decoders for turbo and low density parity check codes (LDPC) either require or perform much better with soft input information which has to be supplied by the channel detector as its soft output. The decoders provide soft outputs which can then be utilized by the outer Reed-Solomon (RS) decoder [22]. A general soft-output sequence detection was introduced in [11], and it is possible to get information on symbol reliabilities by extending those techniques [21, 31].

11.6.2   Reversed Concatenation

Typically, the modulation encoder is the inner encoder, that is, it is placed downstream of an error-correction encoder (ECC) such as an RS encoder; this configuration is known as standard concatenation (Figure 11.5). This is natural since otherwise the ECC encoder might well destroy the modulation properties before passing across the channel. However, this scheme has the disadvantage that the modulation decoder, which must come before the ECC decoder, may propagate channel errors before they can be corrected. This is particularly problematic for modulation encoders of very high rate, based on very long block size. For this reason, a good deal of attention has recently focused on a reversed concatenation scheme, where the encoders are concatenated in the reversed order (Figure 11.6). Special arrangements must be made
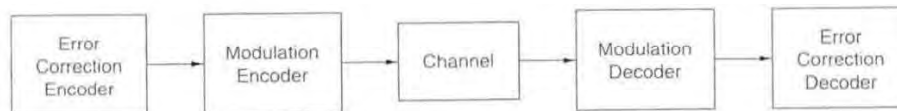

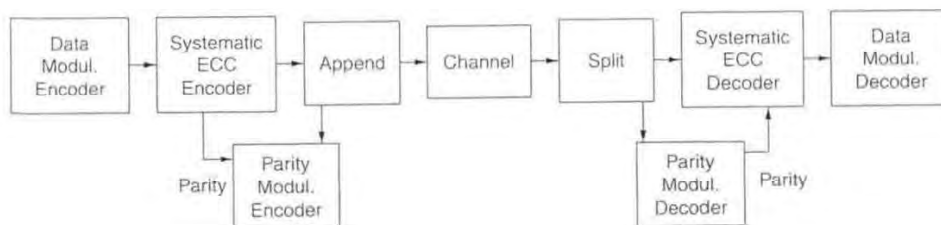FIGURE 11.5   Standard concatenation.

FIGURE 11.6   Reversed concatenation.

to ensure that the output of the ECC encoder satisfies the modulation constraints. Typically, this is done by insisting that this encoder be systematic and then reencoding the parity information using a second modulation encoder (the "parity modulation encoder"), whose corresponding decoder is designed to limit error propagation; the encoded parity is then appended to the modulation-encoded data stream (typically a few merging bits may need to be inserted in between the two streams in order to ensure that the entire stream satisfies the constraint). In this scheme, after passing through the channel the modulation-encoded data stream is split from the modulation-encoded parity stream, and the latter is then decoded via the parity modulation decoder before being passed on to the ECC decoder. In this way, many channel errors can be corrected before the data modulation decoder, thereby mitigating the problem of error propagation. Moreover, if the data modulation encoder has high rate, then the overall scheme will also have high rate because the parity stream is relatively small.

Reversed concatenation was introduced in [3] and later in [23]. Recent interest in the subject has been spurred on by the introduction of a lossless compression scheme, which improves the efficiency of reversed concatenation [15], and an analysis demonstrating the benefits in terms of reduced levels of interleaving [8]; see also [9]. Research on fitting soft decision detection into reversed concatenation can be found in [7, 33].

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UNITED STAT&u DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08//30.716	10/15/96	MOON	J	1008.10-US-0

E1M1/0916

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EXAMINER
KUST, J

ART UNIT	· PAPER NUMBER
2104	

DATE MAILED: 09/16/97

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

EXHIBIT
6

PTO-90C (Rev. 2/90)
*U.S. GPO: 1997-472-10000000

1- File Copy

UMN_0000738

Page 315 of 358

UMN EXHIBIT 2008
LSI Corp. et al. v. Regents of Univ. of Minn.
IPR2017-01068

	Application No. 08/730,716	Applicant(s) Moon et al
Office Action Summary		
	Examiner Jason L. Kost	Group Art Unit 2104

☐ Responsive to communication(s) filed on _____ .

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire ____3____ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-21* is/are pending in the application.

    Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-5, 10, 13-17, and 20* , is/are rejected.

☒ Claim(s) *6-9, 11, 12, 18, 19, and 21* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

    ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

        ☐ received.

        ☐ received in Application No. (Series Code/Serial Number) _____ .

        ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    *Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

UMN_0000739

Page 316 of 358   UMN EXHIBIT 2008
LSI Corp. et al. v. Regents of Univ. of Minn.
IPR2017-01068

DETAILED ACTION

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-5, 10, 13-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iketani et al (U.S. Pat. No. 4,760,378). These claims, as written, read on the well known method of channel encoding wherein m-bit datawords are encoded into n-bit codewords, with n>m, such that there is a minimum physical distance between level transitions in the encoded data to facilitate subsequent detection, and a maximum physical distance between level transitions to facilitate synchronization (i.e., d and k constraints). Iketani discloses such a method. In particular, refer to either Figure 19 or 23 of Iketani, which show encoders including receiver means for receiving datawords, and encoder means for producing DC-free sequences of fixed length codewords for generating no more than 1 consecutive transition in the recorded waveform and no more than k consecutive sample periods without a transition in the encoded waveform. Note that the claim language "generating no more than j consecutive transitions in the recorded waveform such that j is an integer equal to or greater than 2" includes the case in which d is 1 or greater in a NRZI

format, since then there would never be two consecutive level transitions in the encoded

waveform on two consecutive clock pulses.

3.   Claims 6-9, 11, 12, 18, 19, and 21 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

4.   The following is a statement of reasons for the indication of allowable subject matter: The

further limitations of claims 6-9, 11, 12, 18, 19, and 21 essentially require that two or more

consecutive level transitions on two or more consecutive clock pulses in the encoded waveform

be avoided, a condition that is not found in prior art m/n channel encoders.

5.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. Busby (U.S. Pat. No. 4,775,985), van Gestel (U.S. Pat. No. 4,779,072), Benjauthrit

(U.S. Pat. No. 5,341,134), Siegel et al (U.S. Pat. No. 5,450,443), and Soljanin (U.S. Pat. No.

5,608,397) disclose various methods for channel encoding.

6.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Jason Kost, whose telephone number is (703) 308-0308. The examiner can

Serial Number: 08/730,716   Page 4

Art Unit:

normally be reached from 7:00 to 4:30 Monday through Thursday, and from 7:00 to 3:30 on
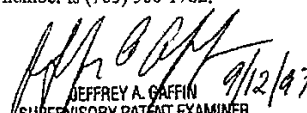
every other Friday.

    If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for this Group is (703)

305-3431.

    Communications via Internet e-mail regarding this application, other than those under 35

U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be

addressed to [jeffrey.gaffin@uspto.gov].

    All Internet e-mail communications will be made of record in
the application file. PTO employees do not engage in Internet
communications where there exists a possibility that sensitive
information could be identified or exchanged unless the record
includes a properly signed express waiver of the confidentiality
requirements of 35 U.S.C. 122. This is more clearly set forth in
the Interim Internet Usage Policy published in the Official
Gazette of the Patent and Trademark on February 25, 1997 at 1195
OG 89.

    Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Group receptionist whose telephone number is (703) 308-1782.

JLK
September 11, 1997

JEFFREY A. GAFFIN 9/12/97
SUPERVISORY PATENT EXAMINER
GROUP 2100

Notice of References Cited		Application No. 08/730,716	Applicant(s) Moon et al			
		Examiner Jason L. Kost	Group Art Unit 2104		Page 1 of 1	

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,608,397	3/4/97	Soljanin	341	58
B	5,450,443	9/12/95	Siegel et al	375	286
C	5,341,134	8/23/94	Benjauhrit	341	58
D	4,779,072	10/18/88	Van Gestel	341	59
E	4,775,985	10/4/88	Busby	375	25
F	4,760,378	6/26/88	Iketani et al	340	347DD
G					
H					
I					
J					
K					
L					
M					

FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

NON-PATENT DOCUMENTS

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V		
W		
X		

UMN_0000743

· NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) __10/15/96__, are
A.____ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
B. __X__ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.
___ Not black solid lines. Fig(s)_____
___ Color drawings are not acceptable until petition is granted.
Fig(s)_____
2. PHOTOGRAPHS. 37 CFR 1.84(b)
___ Photographs are not acceptable until petition is granted.
Fig(s)_____
___ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s)_____
___ Poor quality (half-tone). Fig(s)_____
3. GRAPHIC FORMS 37 CFR 1.84 (d)
___ Chemical or mathematical formula not labeled as separate figure.
Fig(s)_____
___ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis.
Fig(s)_____
___ Individuals waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s)_____
4. TYPE OF PAPER 37 CFR 1.84(e)
___ Paper not flexible, strong, white, smooth, nonshiny, and durable.
Sheet(s)_____
___ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds copy machine marks not accepted. Fig(s)_____
___ Mylar, velum paper is not acceptable (too thin). Fig(s)_____
5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)
21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)
21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)
21.0 cm. by 29.7 cm. (DIN size A4)
___ All drawing sheets not the same size. Sheet(s)_____
___ Drawing sheet not an acceptable size. Sheet(s)_____
6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size

21.6 cm. X 35.6 cm. (8 1/2 X 14 inches)	21.6 cm X 33.1 cm (8 1/2 X 13 inches)	21.6 cm. X 27.9 cm (8 1/2 X 11 inches)	21.0 cm. X 29.7 cm. (DIN Size A4)
T 5.1 cm. (2")	2.5 cm. (1")	2.5 cm. (1")	2.5cm.
L .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	2.5 cm.
R .64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.5 cm
B .54 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.0 cm.

Margins do not conform to chart above.
Sheet(s)_____
___ Top (T) ___ Left (L) ___ Right (R) ___ Bottom (B)

7. VIEWS. 37 CFR 1.84(h)
REMINDER: Specification may require revision to correspond to drawing changes.
___ All views not grouped together. Fig(s)_____
___ Views connected by projection lines or lead lines
Fig(s)_____
Partial views. 37 CFR 1.84(h) 2

___ View and enlarged view not labled separately or properly.
Fig(s)_____
___ Sectional views. 37 CFR 1.84 (h) 3
___ Hatching not indicated for sectional portions of an object.
Fig(s)_____
___ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s)_____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)_____
9. SCALE. 37 CFR 1.84(k)
___ Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction.
Fig(s)_____
___ Indication such as "actual size" or scale 1/2" not permitted.
Fig(s)_____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings).
Fig(s)_____
11. SHADING. 37 CFR 1.84(m)
___ Solid black shading areas not permitted.
Fig(s)_____
___ Shade lines, pale, rough and blurred. Fig(s)_____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
___ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(l) Fig(s)_____
___ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(l) Fig(s)_____
___ English alphabet not used. 37 CFR 1.84(p)(2)
Fig(s)_____
_X_ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3)
Fig(s) 5, 10, 11.
13. LEAD LINES. 37 CFR 1.84(q)
___ Lead lines cross each other. Fig(s)_____
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14 NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
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15. NUMBER OF VIEWS. 37 CFR 1.84(u)
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___ View numbers not preceded by the abbreviation Fig.
Fig(s)_____
16. CORRECTIONS. 37 CFR 1.84(w)
___ Corrections not made from prior PTO-948.
Fig(s)_____
17. DESIGN DRAWING. 37 CFR 1.152
___ Surface shading shown not appropriate Fig(s)_____
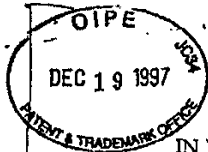___ Solid black shading not used for color contrast.
Fig(s)_____

COMMENTS:

ATTACHMENT TO PAPER NO. __5__   REVIEWER __A. Doan__   DATE __2/28/97__
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Moon et al.   Attorney Docket No.: 1008.10-US-02

Application No.: 08/730,716   Examiner: J. Kost

Filed: October 15, 1996   Group Art Unit: 2104

For: METHOD AND APPARATUS FOR IMPLEMENTING
MAXIMUM TRANSITION RUN CODES

_ _

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action of September 16, 1997, amendment to

the above-identified patent application is requested.

In the Claims

Please amend the claims as follows:

1. (Once amended) Apparatus for encoding m-bit binary datawords into n-bit binary

codewords, in a recorded waveform, where m and n are preselected positive

integers such that n is greater than m , comprising:

receiver means for receiving the dataword;

encoder means coupled to the receiver means, for producing

sequences of fixed length codewords;

UMN_0000745

means for imposing a pair of constraints (j:k) on the encoded waveform wherein the j constraint is defined as the maximum number of consecutive transitions allowed on consecutive clock periods in the encoded waveform to facilitate the reduction of a probability of a detection error in said receiver means:

said sequences generating no more than j consecutive transitions in the recorded waveform such that j is an integer equal to or greater than 2; and

said sequences generating no more than k consecutive sample periods without a transition in the recorded waveform.

13. (Once amended) A method for encoding m-bit binary datawords into n-bit binary codewords in a recorded waveform, where m and n are preselected positive integers such that n is greater than m, comprising the steps of:

receiving binary datawords; and

producing sequences of n-bit codewords;

imposing a pair of constraints (j:k) on the encoded waveform:

generating no more than j consecutive transitions of said sequence in the recorded waveform such that $j \geq 2$; and

generating no more than k consecutive sample periods of said sequences without a transition in the recorded waveform.

2

Remarks

The Examiner rejected claims 1-5, 10, 13-17 and 20 under 35 U.S.C. § 102(b) as being anticipated by Iketani et al. (U.S. Patent No. 4,760,378). Claims 6-9, 11, 12, 18, 19 and 21 were objected to as being dependent upon a rejected claim. The applicants respectfully traverse this rejection for the following reasons.

Claims 1 and 13 are amended herein to better define the invention. No new matter has been introduced as a result of this amendment. The applicants respectfully request that the arguments and discussions posed hereinbelow be reviewed in light of the proposed amendment.

Generally, Iketani et al. teaches a method and apparatus for constructing/converting a run length limited code in which the minimum number of continuous bits of the same binary value is constrained to d and the maximum number thereof is constrained to k. Specifically, Iketani et al. discloses a method and apparatus for converting a run length limited (RLL) code for converting m-bit data words to n-bit code words while constraining the minimum number of continuous bits having the same binary value to d and the maximum number of continuous bits having the same binary value to k in a bit sequence generated by concatenation of the code words. Accordingly, Iketani et al. discloses a method and apparatus in which a minimum number of continuous bits with the same binary value is constrained to d and the maximum number of continuous bits having the same value is constrained to k.

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Further, the primary element of innovation in Iketani et al. is provision of a systematic code conversion which can readily generate a substantially optimum RLL code for a given d and k. Each of 2 (d,k) code words each consisting of n bits is divided into three blocks. Usable code words are selected in accordance with a value uniquely determined for the given d and k, and a uniquely determined concatenation rule for the selected code words is introduced so that a d, k-constrained RLL code having a higher performance can be readily generated.

Thus, Iketani et al. discloses a method and apparatus for encoding an m-bit data word into an n-bit (d, k) RLL codeword.

It should be noted that the definition implemented by Iketani et al. for run length limited (RLL) codes is not consistent to those defined here. The definition used here is the same as that employed by P. H Siegel, "Recoding codes for digital magnetic storage," *IEEE Transactions on Magnetics*, pp. 1344-1349, Sept. 1985 and by Iketani's reference T. Horiguchi et al., "An optimization of modulation codes in digital recording," *IEEE Transactions on Magnetics*, pp. 740-742, Nov. 1976. To quote from the latter,

> RLL codes are such that any two consecutive ones in coded binary sequences are separated by at least d zeros but no more than k zeros . . .. The resulting coded binary sequence is then converted into a waveform using NRZI rules, i.e., a transition for one and no transition for zero.

In contrast, the abstract for Iketani et al. states

> A systematic method and apparatus for constructing a run length limited code in which the minimum number of continuous bits of the same binary value is constrained to d and the maximum number thereof is constrained to k.

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T. Horiguchi et al. describe a rate 2/3 code with d=1 and k=7. This is referenced by Iketani et al., in Embodiment 4, which presents a code with d=2 and k=7 and state "The RLL code of the present embodiment has the same d, Tw, and Tmin as those of the convention 2/3 conversion code and a k which is smaller by one." Thus RLL constraints d, k described by the references and defined herein are equivalent to the constraints by Iketani et al. of d+1 and k+1.

As a result, d=1 described by Iketani et al. is equivalent to a standard d=0 code, which neither requires a non-transition between consecutive transitions nor limits the maximum number of consecutive transitions. The case where d is 1 or greater in NRZI format corresponds to cases in Iketani et al. where d is 2 or greater. In the sequel the definition from T. Horiguchi et al. and the applicant's specifications is used rather than that from Iketani et al. It is well known to those skilled in the art that this method of encoding and the codes associated therewith require a minimum of d clock periods without a transition in the transmitted/recorded signal following the transition. A maximum of k consecutive clock periods without a transition are allowed between two transitions. Accordingly, Iketani et al.'s disclosure relates to a particular/special case in which d= 1. For all cases where d > 0, see for example Iketani et al.'s disclosure for a case where d≥2 (i.e., Per Iketani et al.'s definition), two consecutive transitions cannot occur in two consecutive clock periods. Therefore, the constraint d>0 produces an encoder output in which transitions are separated by a minimum number of clock

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periods and are separated by a minimum physical distance in cases where the encoder output is recorded in a storage medium such as a magnetic disk or tape.

In sharp contrast to Iketani et al., the present invention provides an apparatus for encoding m-bit binary datawords into n-bit binary codewords, in a recorded waveform, where m and n are preselected positive integers such that n is greater than m, including a receiver means for receiving the dataword; encoder means coupled to the receiver means, for producing sequences of fixed length codewords; means for imposing a pair of constraints (j;k) on the waveform wherein the j constraint is defined as the maximum number of consecutive transitions allowed on consecutive clock periods in the encoded waveform; said sequences generating no more than j consecutive transitions in the recorded waveform such that j is an integer equal to or greater than 2; and said sequences generating no more than k consecutive sample periods without a transition in the recorded waveform. The k constraint in the present invention is defined in a manner similar to standard RLL codes. It is included with the j constraint to facilitate synchronization in the receiver.

One of the distinguishing aspects of the present invention includes that j be equal to or greater than two. The most restrictive condition is when j=2. In this case, at most, two consecutive transitions on two consecutive clock periods are allowed. Because the constraint prevents only transition runs with more than j consecutive transitions in consecutive clock periods, patterns with j or fewer consecutive transitions can be permitted. For example, if j=3, the encoder can to

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produce sequences with isolated transitions, two consecutive transitions on two consecutive clock periods, and three consecutive clock periods. All sequences containing j+1 or more consecutive transition on consecutive clock periods are prohibited because they violate the restrictive conditions.

The difference between Iketani et al. and the present invention is clearly shown by comparing the MTR constraint against all RLL codes for which d>0, which therefore includes Iketani's d>1 code. It is well known by those skilled in the art, that any code for which d>0 has the property that a transition cannot occur in the clock period immediately following the clock period in which the transition occurred. The minimum number of clock periods that must pass before the next transition is given by d. In sharp contrast, the MTR code of the present invention with j≥2 does not impose this constraint. Specifically, applicants' invention solves a different problem than the Iketani et al. reference in that the claims recite a method in which codewords that result in two consecutive transitions, in two consecutive clock periods, are possible. This is prohibited by a d>0 code. Accordingly, a subset of the codewords permitted in MTR coding violates all RLL d>0 codes, including those disclosed by the reference. The present invention therefore utilizes a new principle of operation and is novel and distinguished from the reference. Specifically, the distinguishing features are recited in the claims signifying the MTR constraints implemented relative to the RLL code.

It is recognized by those skilled in the art that the sequences eliminated with an MTR code can also be eliminated with an RLL code with d>0, because such a

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code corresponds to the constraint j=1. However, because the MTR constraint allows a set of codewords not valid with RLL d>0 coding, the code rate m/n which is the ratio of the data word bit length to the codeword bit length, can be made larger. This is noteworthy because it allows the MTR code to convey more information per code bit than the corresponding RLL code.

The code rate advantage of MTR (j; k) coding can be quantified by calculating the capacity, or theoretical upper bound for m/n for a particular set of constraints and comparing it against an appropriate RLL (d,k) code. In the range of j values recited in claims 1 and 2 of the present invention, the case for which j=2 is the most restrictive and yields the lowest capacity. Among RLL codes for which d>0, d=1 is the least restrictive and yields the highest capacity.

In the interest of clarifying the distinction between the reference and the present invention, Appendix A is provided herewith for illustrative purposes only. Those skilled in the art would appreciate the fact that discussions/explanations relating to transition run codes are better explained with the help of drawings. Thus, Appendix A illustrates some of the pertinent and distinguishing features of the present invention in light of the Iketani et al., reference. Illustrative example 1 is similar to Iketani et al.'s d=2. Specifically, however, consistent with accepted code definition, illustrative examples 1 and 2 show finite state transition diagrams for an RLL (1, k) code and MTR (2, k) code, respectively. The transition labels are written in NRZI convention where a "1" corresponds to a transition and a "0" to the absence of transition. Any data pattern

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permitted by the code constraints can be obtained by moving from state to state and reading off the transition labels.

A review of the illustrative examples indicates that the MTR code has a larger capacity because the added state increases the number of transitions out of state 0 and into state 1, while all other states are unchanged. This implies that for a fixed number of bits, more sequences could be formed. To quantify the difference, an adjacency matrix A with rows and columns indexed from zero is formed where the element in row i and column j corresponds to the number of transitions from state i to state j in the finite state transition diagram. Using a technique from the field of information theory, the capacity is calculated by taking the base-2 logarithm of the largest real eigenvalue from the matrix A. Consider the RLL (1,7) code which is common in magnetic recording applications. The capacity for the constraints is 0.6792 and the rate 2/3 code commonly used achieve 98.1% of this upper bound. On the other hand, the MTR code with j=2 and k=7 yields a capacity of 0.8732, allowing rates of m/n such as 6/7. In this illustrative example, the MTR code has a capacity which is 28.6% greater than the RLL d=1 code. This means that if an RLL codeword of length n can convey four bits of data, an MTR codeword of the same length corresponds to a little more than five bits of data.

The relationship between various code constraints may be better illustrated with examples of the relevant sequences. Illustrative example 3 shows eight representative binary sequences and indicates which, if any, code constraints they violate. Sequence I and II simply show that a sequence with more than k NRZI

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zeros violates the k constraint used by both the RLL and MTR codes. Sequence III is a single transition that is allowed in all cases. Sequence IV, however, violates the RLL d=1 because it does not contain the requisite minimum of one non-transition between adjacent transitions. It is also allowed by all the MTR j constraints considered. Sequence VI, which has three consecutive transition in three consecutive clock periods violates both the RLL d=1 and MTR j=2 constraints, but is valid for MTR j≥3. Sequence VII shows j consecutive transitions for the case where j>3, and sequence VIII is the same sequence with one additional transition. In all cases, the conclusions are the same if the polarity of the underlying waveform is inverted.

As is understood by those skilled in the art, there is a difference between MTR coding and RLL coding with d=0, which is the same as Iketani et al.'s d=1. If d=0, then multiple consecutive clock periods are allowed. However, the d=0 constraint, unlike the MTR j constraint, does not specify an upper limit to the number of consecutive transitions. This is a significant difference between the two coding systems because, as recited in the claims of the present invention, constraining the maximum number of consecutive transitions in consecutive clock periods to j is the mechanism by which the code structure enables the probability of a detection error in the receiver to be reduced.

Accordingly, the present invention is not anticipated by Iketani et al. Further, the applicants' invention solves a different problem than the reference and such different problem is recited in the claims. Furthermore, the present invention
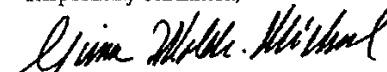
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is not rendered obvious by the Iketani et al. reference because there is no suggestion or implication of the inventive elements of the present invention by the reference.

The references made of record but not relied upon have been noted. These references are believed to neither teach nor suggest the applicants' invention, either alone or in combination with the other prior art of record.

In conclusion, in light of the amendment of claims 1 and 13 and the comments and arguments advanced hereinabove, all pending claims 1-21 are now in condition for allowance. Notice to that effect is respectfully requested.

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,

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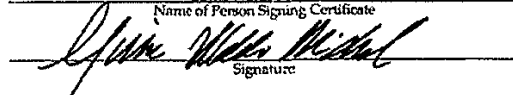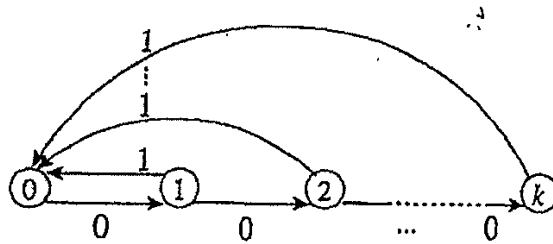
Illustrative Example 1. Finite state transition diagram with NRZI labels for an RLL (d=1, k) (Iketani, d=2) code.
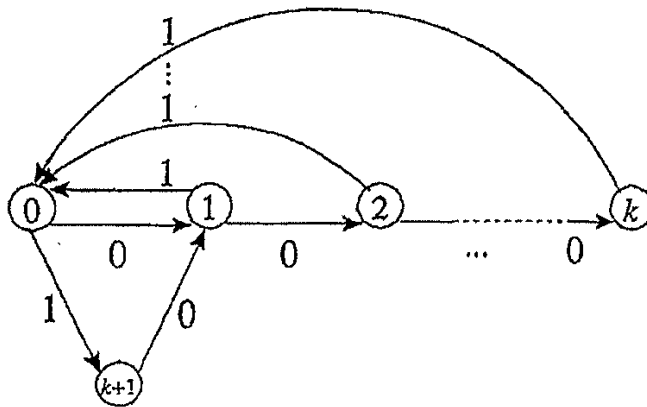
Illustrative Example 2. Finite state transition diagram with NRZI labels for and MTR (j=2; k) code.

Binary Sequences   Violates Code Constraint

	k	$d=1$	$j=2$	$j=3$	$j>3$
I	N	N	N	N	N
II	Y	N	N	N	N
III	N	N	N	N	N
IV	N	Y	N	N	N
V	N	N	N	N	N
VI	N	Y	Y	N	N
VII	N	Y	Y	Y	N
VIII	N	Y	Y	Y	Y

Illustrative Example 3. Representative binary sequences eliminated by the relevant code constraints. The NRZI code bits are indicated above the appropriate waveform.

Manchester Receiver

The Manchester Receiver example shows how to use the HDL Verifier™ to design,
test, and verify a VHDL Manchester Receiver model with clock recovery capabilities.

Background on Manchester Encoding

Transmission of digital data frequently requires some form of modulation to overcome limits in a physical signal channel. One
technique used for modulating digital data is Manchester Encoding. This technique has the following useful characteristics:

- The transmit clock signal can be easily extracted from the received data.
- The encoded signal never produces frequency components near DC, regardless of the data, which is useful for transmission
  over channels that require AC coupling.
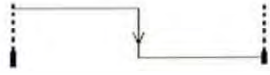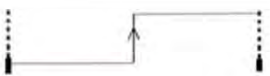- The encoding circuit is very simple and stateless.

On the negative side, Manchester coding requires substantial bandwidth (above the Shannon limit), which tends to limit its
usefulness in wireless applications. However, for connected applications such as short haul Optical fiber and Ethernet, it is
frequently a good solution.

The following sections discuss:

- The Encoding
- The Receiver
- Decoding with Inphase and Quadrature Convolution

The Encoding

Manchester Encoding involves a transmitter that encodes clock and data signals in a synchronous bit stream, such that each bit
represents a signal transition. The following table shows how each bit setting is defined for an encoding:

Bit Setting	Transition	Encoded Waveform
1	1 to 0	
0	0 to 1	

Transitions in the Manchester Encoding occur at the center and beginning of each bit. The transition at the center is defined by the
bit value, while the transition at the beginning is dependent on the value of the previous bit. Consider the following diagram:
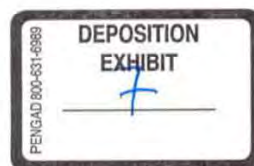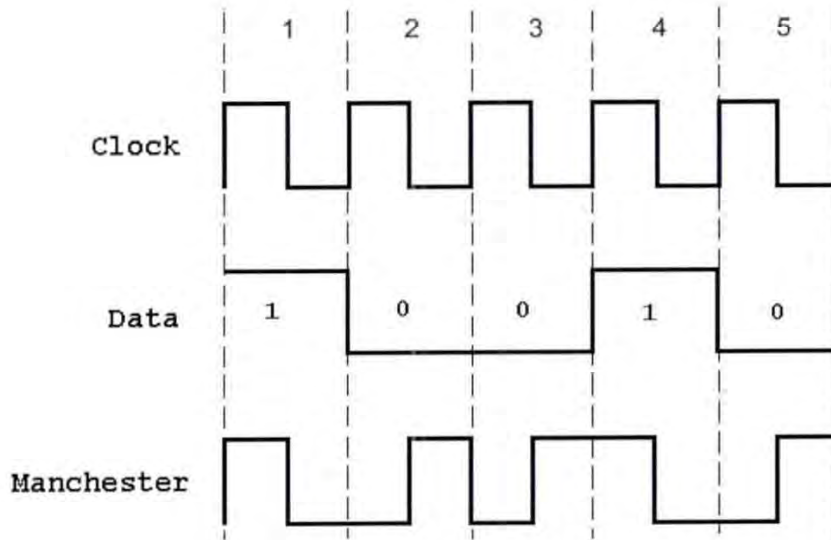
As the preceding Manchester encoded signals shows:

- The value of 1 for the first bit forces a high-to-low transition at the center of that bit.
- The value of 0 for the second bit forces a low-to-high transition at the center of that bit and, because the first bit transitioned from high-to-low, no transition occurs at the start of that bit.
- The value of 0 for the third bit forces a low-to-high transition at the center of that bit and because the second bit transitioned from low-to-high, a high-to-low transition occurs at the start of that bit.
- The value of 1 for the fourth bit forces a high-to-low transition at the center of that bit and, because the third bit transitioned from low-to-high, no transition occurs at the start of that bit.
- The value of 0 for the fifth bit forces a low-to-high transition at the center of that bit and, because the fourth bit transitioned from high-to-low, no transition occurs at the start of that bit.

The Receiver

A device that receives the encoded bit stream is responsible for decoding the bit stream by separating the clock and data information. In most cases, the receiver must retrieve the original data stream by using only the encoded signal. This simplifies the communications channel, but means the receiver must overcome the following:

- Differences between the clock used to encode the signal and the clock in the receiver (see the figure below).
- The two clocks can be close in frequency, but small frequency errors occur.
- The phase between the clocks will be arbitrary.
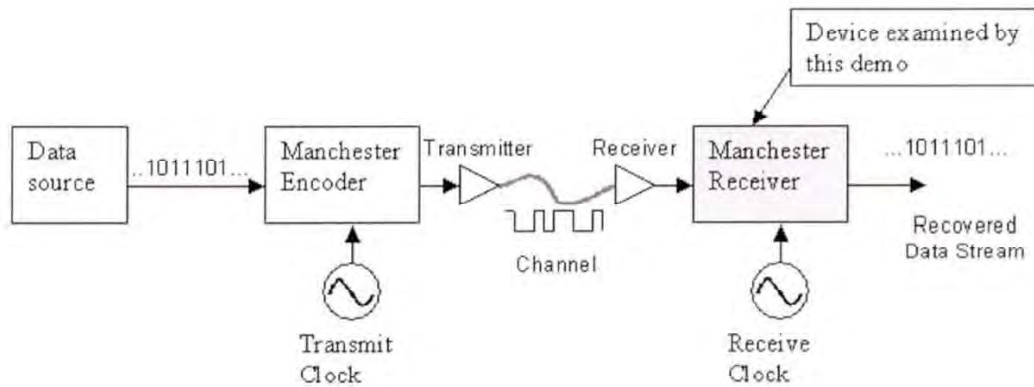
The Manchester Receiver example validates the computations performed by a Manchester Receiver device that is modeled in VHDL and simulated in ModelSim®. Numerous approaches are available for implementing a Manchester receiver. This example uses a Delay Lock Loop (DLL) that requires the receiver to use a clock that is very close in frequency to the transmit clock. This results in a simple clock recovery circuit that has a limited frequency lock range.

The receiver over-samples the received data stream at 16 times the data rate. Thus, the receive clock must have a nominal period of 1/16th the data period. To compensate for minor differences between the transmitting and receiving clocks or drifts in the channel delay, the receiver adjusts its data period by up to one clock cycle (+/-) per data period. Thus, the receiver can use 15, 16 or 17 clock cycles to recover the data encoded from the incoming sampled signal. For example, if the receiver clock is slightly faster then the transmitter clock (frequency error), the receive cycle occasionally needs to add an extra clock cycle to compensate.

Large sudden phase errors, such as those that occur at startup time, require multiple data periods to acquire a good lock on the signal. By limiting the maximum phase correction to 1/16th of the total data period, the receiver can be slow to correct large phase errors.

Decoding with Inphase and Quadrature Convolution

Decoding a received Manchester signal can occur in several ways, but the approach taken in this example is to consider Manchester Encoding as a digital phase modulation with two symbols; +180 and -180 degrees. By convolving the incoming signal with a reference inphase (I) and quadrature (Q) waveform at the modulation frequency, it is possible to extract the data and retrieve information about any phase errors in the received waveform. After one data cycle, the receiver computes two values (referred to as Isum and Qsum in the VHDL code), which are measurements of the I/Q convolution value. The receiver then decodes the values to predict:

- The original transmitted data value for the cycle
- An estimate of the phase error between the incoming signal and the receiver's data period

A critical aspect of this design is the interpretation of the I/Q convolution values. At the end of a data receive cycle, the receiver translates the I/Q values into an estimate of the transmitted data and phase error. One way to present this information is to show these interpretations as plots versus measured I/Q values.

Data is considered invalid if the measured I and Q are completely ambiguous about the encoded data value.

In a similar way, you can generate an I/Q mapping of the phase correction value in plot format. Such a plot gives a visual representation of the decoding block. In practice, the details of this mapping have strong impact on the stability and performance of the Manchester receiver.

In the ideal case where the receiver is perfectly locked to the incoming waveform, the receive cycle is 16 cycles long and the measured I/Q convolution values are fairly easy to interpret. However, data cycles that are 15 or 17 cycles long create some bias in the measurement of the IQ convolution. It is possible to customize the I/Q measurement during these cycles, but that would increase the size and complexity of the receiver. Instead, the data acquisition cycle is extended or shortened with no change in decoding the resulting values. However, this decoder bias can create problems with dithering or reduced noise immunity.

VHDL Implementation of a Manchester Receiver

The focus of this example is a VHDL implementation of a Manchester Receiver. Decoding a Manchester encoded signal presents several challenges, the most prominent of which is clock recovery. The clock is embedded in the received signal and must be extracted to reproduce the original data stream. The figure below shows the example design, which is divided into three main sections of VHDL code:

IQ convolver: Samples the received signal and computes the convolution for the inphase (I) and quadrature (Q) waveforms. For each waveform, the computation is implemented as the sum of XOR operations on the sample and decoded waveform received from the state counter.

Decoder: Models a combinatorial circuit that interprets the results of the I/Q convolver.

State counter: Generates the I/Q waveforms that are convolved with received signals, taking into account phase errors (lags and leads), as necessary. The phase of the I/Q generator is adjusted to match the incoming Manchester encoded waveform. To accomplish the necessary adjustment, at the beginning of a new cycle, the state counter checks an adjustment value, adj, and then changes the period of the next I/Q cycle. This adjustment value is limited to adding or removing a single clock period from the 16 periods that are nominally used for an I/Q waveform.
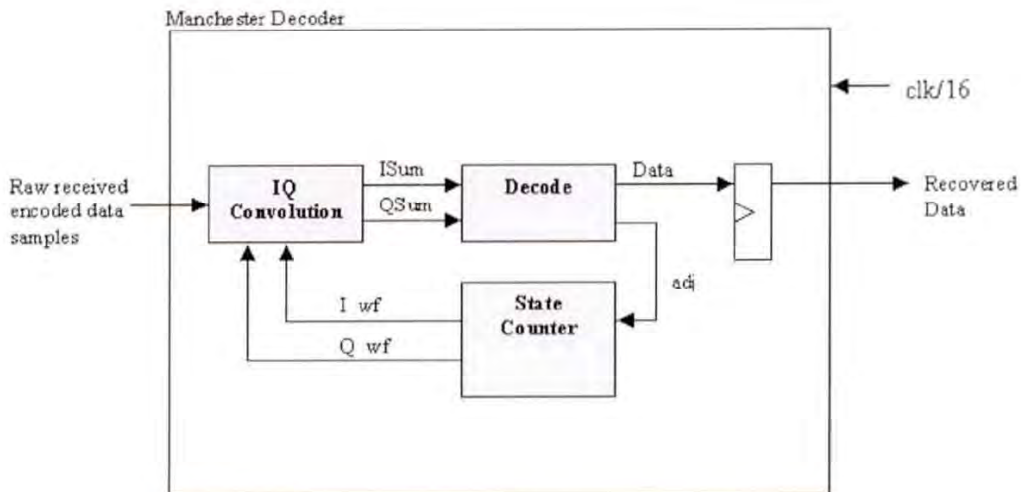
The following timing diagram shows an inphase waveform, quadrature waveform, and the convolved results with no phase error, data lags, and data leads.
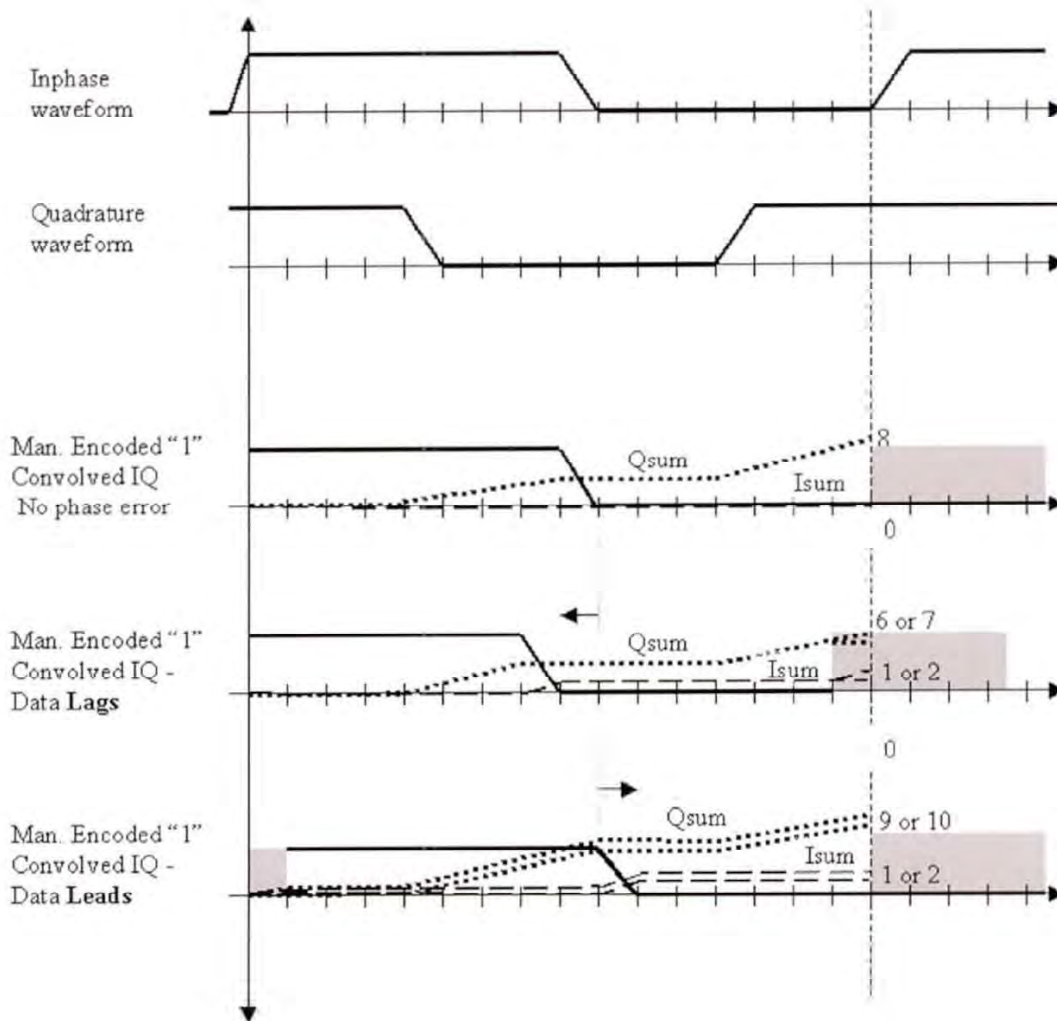
MATLAB® Models of VHDL Components

The example includes three MATLAB® functions that test the VHDL model. A MATLAB function maps to each of the three VHDL components:

I/Q convolver: Verifies that the VHDL I/Q convolver code computes expected output for a randomly generated stream of samples. The MATLAB function verifies this by computing the convolution for the inphase and quadrature waveforms (I_wf and Q_wf). The computation is implemented as an XOR and accumulation of the binary signals.

Decoder: Displays a plot of the I/Q mapping generated by the decoder for visual verification.

State counter: Generates the inphase and quadrature waveforms. During test benching, this MATLAB function has complete control of signals applied during the simulation, including clock generation, resets, and so on.

Running the Example

Starting the MATLAB Server

The example starts the MATLAB server, hdldaemon, such that it uses TCP socket communication with a socket port number identified as available by the operating system.

```
hdldaemon('socket',0)        % Activate MATLAB server to accept foreign VHDL calls
```

```
HDLDaemon socket server is running on port 4040 with 0 connections
```
The example then calls hdldaemon with the 'status' option to get the assigned port number and store it in portnum for future reference.

```
dstat = hdldaemon('status');
portnum = dstat.ipc_id;
```

```
HDLDaemon socket server is running on port 4040 with 0 connections
```
Both the server and client parts of an application link must use the same port number. Thus, at some point, the example program needs to forward the portnum over to ModelSim.

Testing the Decoder

The first component of the Manchester Receiver model to be tested is the decoder. The script creates 2 plots of the transfer function of this entity. This test is simply a visualization of the decoder behavior. The example script:

1. Sets a testisdone flag to 0 and displays informational messages.

```
global testisdone;
testisdone = 0;
```

2. Sets the project directory to a directory that has write access and is suitable for holding a ModelSim project.

```
projectdir = pwd;
```

3. Changes the format of the project directory and decoder VHDL file specifications to the UNIX® format, which ModelSim and Tcl use, by replacing backslashes (\) with forward slashes (/).

```
unixprojectdir = ['"' strrep(projectdir,'\','/')  '"'];
unixsrcfile = ['"' ...
    strrep(fullfile(matlabroot,'toolbox','edalink','extensions','modelsim',...
    'modelsimdemos','vhdl','manchester','decoder.vhd'),'\','/') ...
    '"'];
```

4. Defines a sequence of Tcl commands to be executed in the context of ModelSim.

```
tclcmd = { ['cd ' unixprojectdir ],...
            'vlib work',...
           ['vcom -performdefaultbinding ' unixsrcfile],...
            'vsimmatlab work.decoder',...
           ['matlabtb decoder -mfunc manchester_decoder -socket ',num2str(portnum)],...
            'run 3000',...
            'quit -f'};
```

The previous list defines each command:

- Changes to the writable project directory.
- Adjusts the placement of the ModelSim window so it does not obscure the MATLAB window.
- Creates the project library work if it does not already exist.
- Compiles the VHDL file. The example script specifies the 'performdefaultbinding' option to enable default bindings in the event that they have been disabled in the modelsim.ini file.
- Loads an instance of the VHDL entity decoder for MATLAB test benching with the vsimmatlab command. This command is an HDL Verifier extension to the ModelSim command set.
- Initiates a MATLAB test benching session for the loaded instance of entity decoder with the matlabtb command. This command is an extension to the ModelSim command set. The command in the example specifies the entity instance, the MATLAB function that is to test the entity (manchester_decoder.m), and TCP socket communication with socket port portnum. For a link to be established between ModelSim and MATLAB, the value of portnum must match the socket port that was specified when the MATLAB server (hdldaemon) was started.

- Runs the ModelSim simulation for 3000 iterations of the current resolution limit. By default, the simulation runs for 3000 nanoseconds. Quits ModelSim without asking for confirmation.

5. Starts ModelSim for use with the HDL Verifier with a call to vsim.

```
vsim('startupfile','decoder.do','tclstart',tclcmd);
```

This command starts ModelSim with a Tcl command script that executes some general-purpose startup commands and then the user-defined commands specified with the 'tclstart' property. The 'startfile' property causes vsim to write the entire startup Tcl command script to decoder.do for future reference or use.

6. Displays informational messages and waits for (manchester_decoder.m) to run to completion.

```
disp('Waiting for testing of ''decoder.vhd'' to complete');
disp('(flag from manchester_decoder.m indicates completion)');
while testisdone == 0,
    pause(0.501);
end
disp('MATLAB test of decoder.vhd is complete!');
disp('Check the generated plot for results.');
```

```
Waiting for testing of 'decoder.vhd' to complete
(flag from manchester_decoder.m indicates completion)
done
MATLAB test of decoder.vhd is complete!
Check the generated plot for results.
```
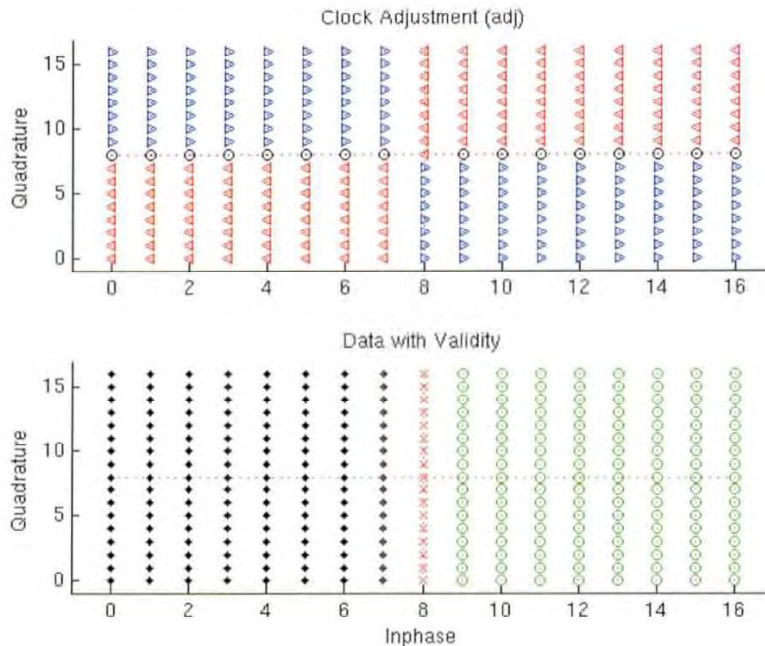

Testing the I/Q Convolver

Similarly for the I/Q convolver. The example script:

1. Sets a testisdone flag to 0 and displays informational messages.

```
testisdone = 0;
```

2. Sets the project directory to a directory that has write access and is suitable for holding a ModelSim project.

```
projectdir = pwd;
```

3. Changes the format of the project directory and decoder VHDL file specifications to the UNIX format, which ModelSim and Tcl use, by replacing backslashes (\) with forward slashes (/).

```
unixprojectdir = ['"' strrep(projectdir,'\','/')  '"'];
unixsrcfile = ['"' ...
    strrep(fullfile(matlabroot,'toolbox','edalink','extensions','modelsim',...
    'modelsimdemos','vhdl','manchester','iqconv.vhd'),'\','/') ...
    '"'];
```

4. Defines a sequence of Tcl commands to be executed in the context of ModelSim.

```
tclcmd = { ['cd ' unixprojectdir ],...
            'vlib work',...
          ['vcom -performdefaultbinding ' unixsrcfile],...
            'vsimmatlab work.iqconv',...
            'force /iqconv/clk 1 0, 0 5 ns -repeat 10 ns ',...
            'force /iqconv/enable 1',...
            'force /iqconv/reset 1',...
            'run 100',...
          ['matlabtb iqconv -rising /iqconv/clk -mfunc manchester_iqconv -socket ',num2str(portnum)],...
            'run 1000',...
            'quit -f'};
```

The following list defines each command:

* Changes to the writable project directory.
* Adjusts the placement of the ModelSim window so it does not obscure the MATLAB window.
* Creates the project library work if it does not already exist.
* Compiles the VHDL file. The example script specifies the -performdefaultbinding option to enable default bindings in the event that they have been disabled in the modelsim.ini file.
* Loads an instance of the VHDL entity iqconv for MATLAB test benching with the vsimmatlab command. This command is an HDL Verifier extension to the ModelSim command set.
* Applies the ModelSim force command to drive the entity's clk, enable, and reset signals, which get passed on to the test bench as oport data. The first force command specifies that clk is to be set to 1 at time equals 0, to 0 after 5 nanoseconds, and repeat the high-to-low cycle every 10 nanoseconds. The second and third force commands set the enable and reset signals to 1.
* Runs the ModelSim simulation for 100 iterations of the current limit. By default, the simulation runs for 100 nanoseconds. This accounts for the startup phase.
* Initiates a MATLAB test benching session for the loaded instance of entity iqconv with the matlabtb command. This command is an extension to the ModelSim command set. The command in the example specifies the entity instance iqconv, the event that triggers an invocation of the MATLAB function, the MATLAB function that is to test the entity (manchester_iqconv.m), and TCP socket communication with socket port portnum. The -rising option specifies that the MATLAB function be called when clk experiences a rising edge. For a link to be established between ModelSim and MATLAB, the value specified with -socket must match the socket port that was specified when the MATLAB server (hdldaemon) was started.
* Runs the ModelSim simulation for 1000 iterations of the current resolution limit. By default, the simulation runs for 1000 nanoseconds.
* Quits ModelSim without asking for confirmation.

5. Starts ModelSim for use with the HDL Verifier with a call to vsim.

```
vsim('startupfile','iqconv.do','tclstart',tclcmd);
```

This command starts ModelSim with a Tcl command script that executes some general-purpose startup commands and then the user-defined commands specified with the 'tclstart' property. The 'startfile' property causes vsim to write the entire startup Tcl command script to iqconv.do for future reference or use.

6. Displays informational messages and waits for (manchester_iqconv.m) to run to completion.

```
disp('Waiting for testing of ''iqconv.vhd'' to complete');
disp('(flag from manchester_iqconv.m indicates completion)');
while testisdone == 0,
    pause(0.501);
end
disp('Test of iqconv.vhd complete (If it failed, there would be an error message printed above)!');
```

```
Waiting for testing of 'iqconv.vhd' to complete
(flag from manchester_iqconv.m indicates completion)
Test of iqconv.vhd complete (If it failed, there would be an error message printed above)!
```

Testing the State Counter

Now we test the State Counter (statecnt.vhd). The script will create checks isum and qsum outputs for a randomly generated stream of data samples and sets the testisdone flag to 0 and displays informational messages.

```
testisdone = 0;
projectdir = pwd;
unixprojectdir = ['"' strrep(projectdir,'\','/')  '"'];
unixsrcfile = ['"' ...
    strrep(fullfile(matlabroot,'toolbox','edalink','extensions','modelsim','modelsimdemos',...
    'vhdl','manchester','statecnt.vhd'),'\','/') ...
    '"'];

tclcmd = { ['cd ' unixprojectdir ],...
            'vlib work',...
           ['vcom -performdefaultbinding ' unixsrcfile],...
            'vsimmatlab -t 1ns work.statecnt ',...
            'force /statecnt/clk 1 0, 0 5 ns -repeat 10 ns ',...
           ['matlabtb statecnt -mfunc manchester_statecnt -socket ',num2str(portnum)],...
            'run 30000',...
            'quit -f'};
```

The following list defines each TCL command in the tclcmd:

- Changes to the writable project directory.

- Adjusts the placement of the ModelSim window so it does not obscure the MATLAB window.

- Creates the project library work if it does not already exist.

- Compiles the VHDL file. The example script specifies the -performdefaultbinding option to enable default bindings in the event that they have been disabled in the modelsim.ini file. Loads an instance of the VHDL entity statecnt for MATLAB test benching with the vsimmatlab command. This command is an HDL Verifier extension to the ModelSim command set. The -t option specifies a ModelSim simulator time resolution of 1 nanosecond (the default). Applies the ModelSim force command to drive the entity's clk signal, which gets passed on to the test bench as oport data. The force command specifies that clk is to be set to 1 at time equals 0, to 0 after 5 nanoseconds, and repeat the high-to-low cycle every 10 nanoseconds.

- Initiates a MATLAB test benching session for the loaded instance of entity statecnt with the matlabtb command. This command is an extension to the ModelSim command set. The command in the example specifies the entity instance statecnt, the MATLAB function that is to test the entity (manchester_statecnt.m), and TCP socket communication with socket port portnum. For a link to be established between ModelSim and MATLAB, the value specified with -socket must match the socket port that was specified when the MATLAB server (hdldaemon) was started.

- Runs the ModelSim simulation for 30000 iterations of the current resolution limit. By default, the simulation runs for 30000 nanoseconds.

- Quits ModelSim without asking for confirmation.

```
vsim('startupfile','statecnt.do','tclstart',tclcmd);

disp('Waiting for testing of ''statecnt.vhd'' to complete');
disp('(flag from manchester_statecnt.m indicates completion)');
while testisdone == 0,
    pause(0.501);
```

```
end
disp('MATLAB test of statecnt.vhd is complete!');
disp('Check the generated plot for results.');
```

```
Waiting for testing of 'statecnt.vhd' to complete
(flag from manchester_statecnt.m indicates completion)
MATLAB test of statecnt.vhd is complete!
Check the generated plot for results.
```
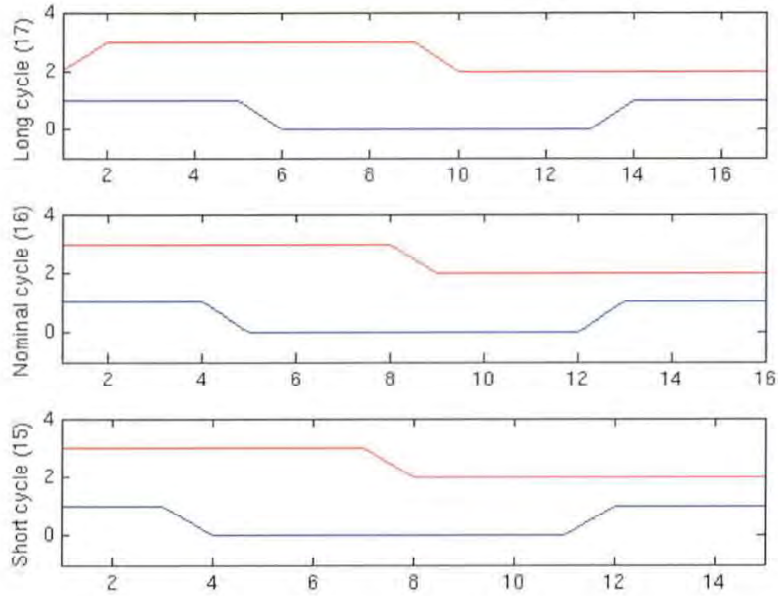

Kill hdldaemon

```
hdldaemon('KILL');
```

```
HDLDaemon server was shutdown
```
Test of statecnt.vhd complete (Examine plot produced). This concludes the manchester tutorial example.

United States Patent [19]

Soljanin

[11] Patent Number: 5,608,397

[45] Date of Patent: Mar. 4, 1997

[54] **METHOD AND APPARATUS FOR GENERATING DC-FREE SEQUENCES**

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[21] Appl. No.: **515,445**

[22] Filed: **Aug. 15, 1995**

[51] Int. Cl.^{6} **H03M 7/00**

[52] U.S. Cl. **341/58**; 341/50; 341/95; 360/40

[58] Field of Search 341/58, 50, 95, 341/106; 360/39, 40

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Attorney, Agent, or Firm—Katharyn E. Olson

[57] **ABSTRACT**

A method and apparatus generates a channel codeword based on codewords with arbitrary block digital sums. Respective portions of the channel codeword are generated based on respective sets of input symbols, and the channel codeword is generated from the portions in accordance with another set of input symbols. The potions are advantageously codewords, comprising symbols, generated by selecting, for each set of input symbols, a codeword from a codebook and by adapting, as for example by ordering or by inverting symbols in, the codewords to form the channel codeword.

50 Claims, 5 Drawing Sheets

FIG. 1

INFORMATION → | LEMPEL-ZIV COMPRESSOR | → | REED-SOLOMON CODER | → | MODULATION CODER |

110   120   130

| MODULATION CODER | ↓

NOISE → | CHANNEL/ MEDIUM |

140

| CHANNEL/ MEDIUM | ↓

RECEIVED INFORMATION ← | LEMPEL-ZIV DECOMPRESSOR | ← | REED-SOLOMON DECODER | ← | MODULATION DECODER | ← | EQUALIZER |

180   170   160   150

FIG. 2

$q \bullet m + p$
INPUT SYMBOLS

130

$\{m_1, m_2, ... m_q\}$ → | CODEBOOK OF 2^m CODEWORDS OF BDS = x | → $\{n_1, n_2, ... n_q\}$ → | INVERTER | → BDS = 0 OUTPUT CODEWORD

p   210   220

| CONTROL CODEBOOK | → CONTROL CODEWORD →

230

FIG. 3

FIG. 4

FIG. 5

FIG. 6

FIG. 7

FIG. 8

FIG. 9

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METHOD AND APPARATUS FOR GENERATING DC-FREE SEQUENCES

TECHNICAL FIELD

The invention relates to a field of coding for digital systems.

BACKGROUND OF THE INVENTION

Information (e.g., signals representing voice, data, video, text, or encoded versions thereof) must typically be processed before the information can be transmitted over a communications channel or recorded on a medium. First, the information, if not already in digital form, is digitized, as for example by an analog-to-digital converter whereby the information is represented as symbols comprising elements from a set of binary digits or bits, {0,1}. Next, the digitized information may be optionally be compressed to represent the information in a reduced number of symbols. Any reduction in the number of symbols representing the information may be partially offset if the compressed information is processed using error correcting codes. Error correcting codes introduce additional symbols to a signal (e.g. to a digital representing compressed information) to form an encoded signal. In particular, an error correcting code operates on groups of symbols, called information words, in the signal. Each information word is used to generate, according to a prescribed error correcting coding 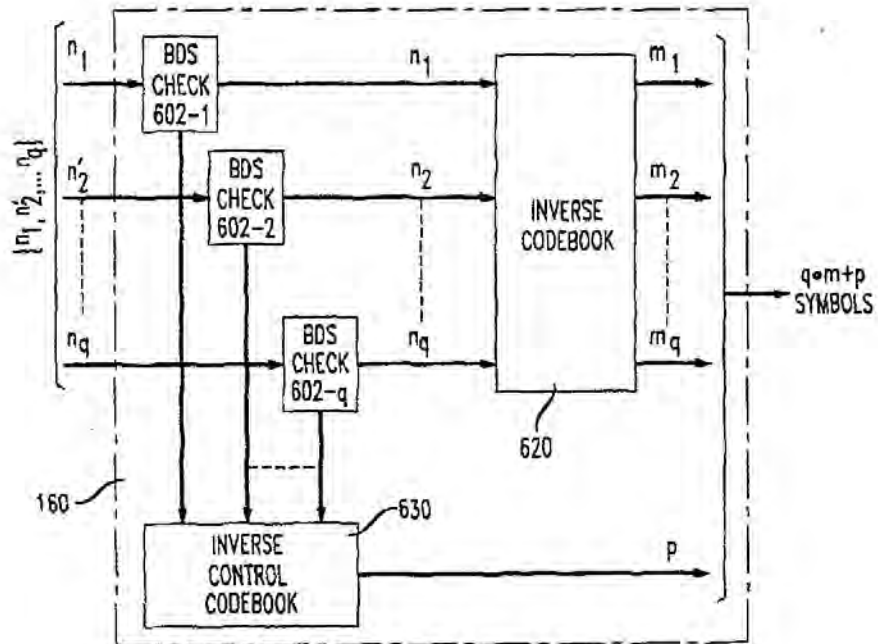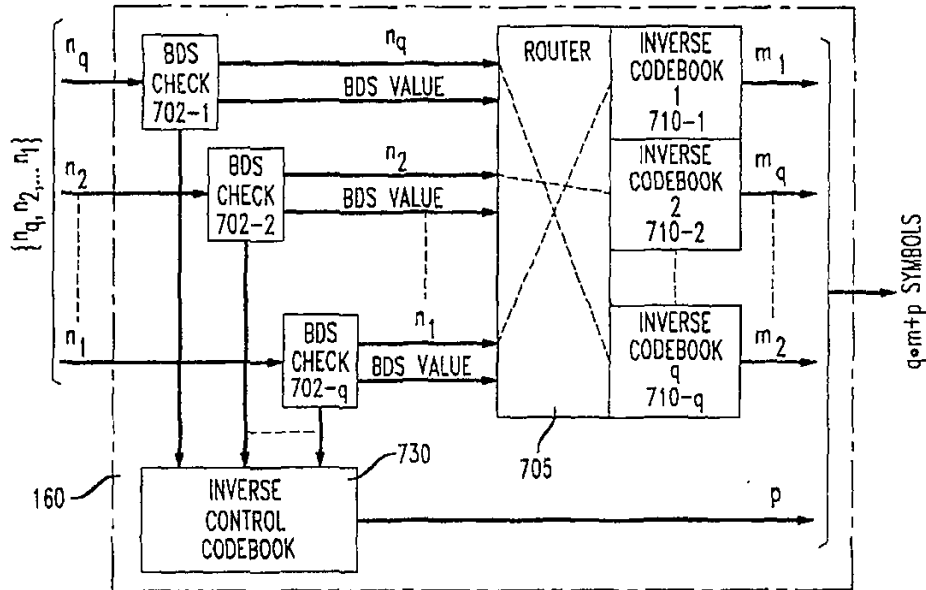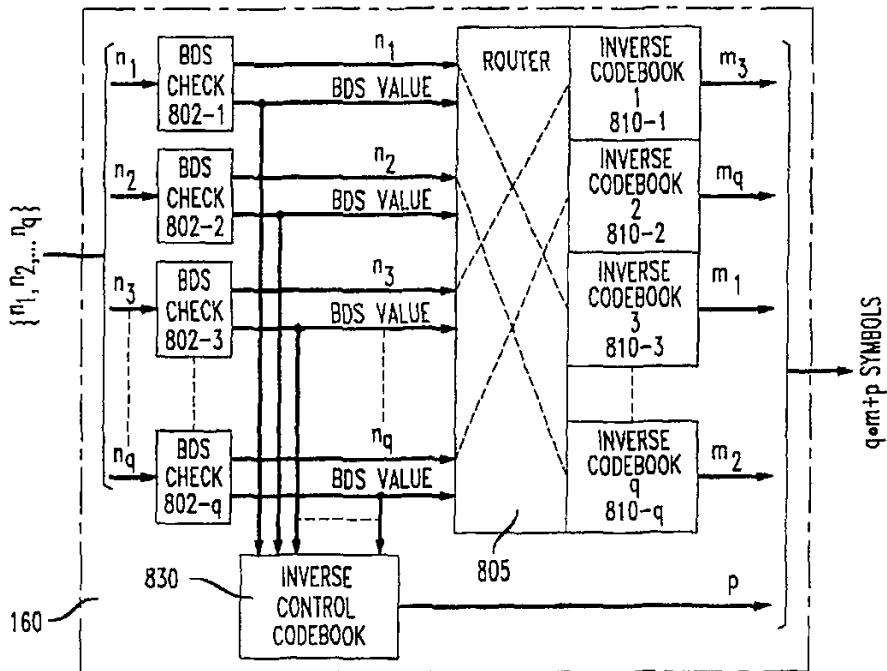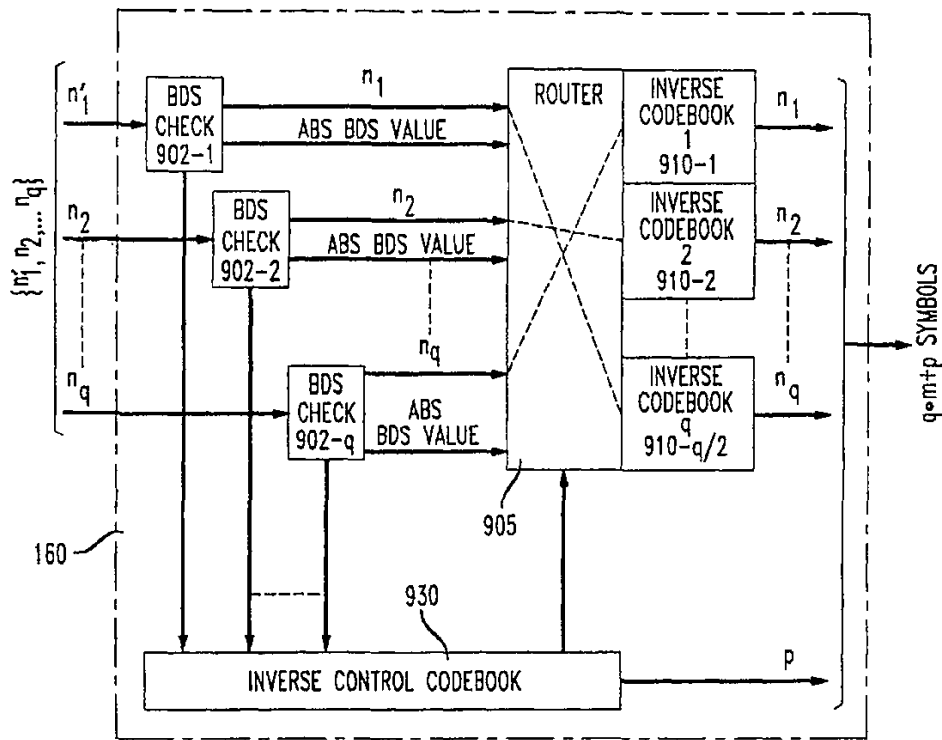rule, a codeword comprising a larger group of symbols. See e.g., Shu Lin and Daniel J. Costello, Jr., *Error Control Coding,* Prentice Hall, Englewood Cliffs, N.J., 1983. The encoded signal, comprising the codewords, may then be either transmitted over the communications channel or recorded on a medium. In either case, the encoded signal will be corrupted by noise introduced in the transmission or recording process, such as by atmospheric noise (caused by lightening) on radio channels. The additional symbols introduced by the error correcting codes improve the ability of a system receiving the corrupted encoded signal to recover the compressed information.

Importantly, an additional or further kind of coding, termed modulation coding, is often used to process information (such as the encoded signal generated using the error correcting codes) before transmission over a channel or recording on a medium. In particular, modulation coding advantageously transforms a group of input symbols (such as a group of symbols which comprises a codeword generated by an error correcting code) and generates a channel or modulation codeword which channel codeword comprises a larger number of symbols than the number of symbols in the group of input symbols. As with error correcting codes, modulation coding can improve a system's immunity to noise. Perhaps more importantly, modulation codes can advantageously be used to regulate time parameters (e.g. for controlling oscillator or counting circuits) and to regulate gain parameters (e.g. for amplifier circuits) in recording and communications systems as explained below.

Modulation coding may be implemented, for example, by establishing, for each possible combination of input symbols in a group, a one-to-one mapping between the group and a corresponding channel codeword. In short, each combination of input symbols uniquely specifies a channel codeword and vice versa. Such a mapping may be established by taking a group of input symbols and using it as an address of a memory device (such as a read only memory or a random access memory) where the contents of the address

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are the symbols comprising the channel codeword. The memory device is referred to as a codebook. The particular group of input symbols may be obtained or decoded from the channel codeword by using, for example, an inverse codebook where a channel codeword is an address of a location in a memory device where the contents of the address are the group of symbols corresponding to the channel codeword.

Consider a system which records information on a magnetic medium and in which a channel codeword comprising a sequence of seven binary digits "1010001" is to be represented on the magnetic medium. The binary sequence is advantageously used to modulate or control the flow of an electrical current in one of two opposite directions. The current in turn, produces a magnetic field the direction of which magnetic field is in one of two opposite directions depending on the direction of the current. In particular, transitions from one direction in the current (and consequently in the magnetic field) to the other, correspond to binary "1's" in the sequence. Thus, assuming the electrical current and corresponding magnetic field are established in respective "initial" directions, the first "1" in the sequence of seven binary digits would cause the current and corresponding magnetic field are established to transition or switch to the opposite directions. The current and corresponding magnetic field would remain in the opposite direction during the first "0" in the sequence of seven binary digits. The third binary digit, which is a "1", causes the current and magnetic field to revert or transition back to their initial directions where they remain for the next three digits in the sequence of seven binary digits, i.e., the "0's" cause no change in the direction of magnetization. The seventh digit in the sequence is a "1" which causes the current and corresponding magnetic field to transition to the opposite directions.

To represent the seven digit binary sequence on the magnetic medium, the magnetic medium is divided into portions with each portion corresponding to a particular digit in the binary sequence. Each portion of the magnetic medium is, in turn, exposed to the magnetic field produced according to its corresponding bit in the channel codeword, and is consequently magnetized by the field in one of the two directions. The information recorded on the medium is termed a channel sequence and is defined by the channel codeword. The channel sequence comprises channel symbols, but unlike the symbols in the information and channel codewords described above, the channel symbols in a channel sequence for a magnetic medium are advantageously selected from a set of bipolar symbols, {−1,1}, which set of symbols more closely reflects the physical manifestation of the channel sequence on the medium in which the portions are magnetized with equal (i.e. unit) intensity in one of two (i.e. bi-) opposite (i.e. polar) directions.

The channel codeword which defined the channel sequence is read by detecting a change in a voltage signal caused by: 1) changes in the magnetization of portions of the medium and 2) by noise in the system. The voltage signal is a pulse each time a "1" is detected and just noise each time a "0" is detected. The position of the pulses carries information about timing parameters in the system, and the height of the pulses carries information about gain parameters in the system. Importantly, however, if a long string of "0's" are read, there is no voltage output (other than noise), and hence no timing or gain information, thereby leading to a loss of, or drift in, timing and gain parameters.

Thus, modulation coding schemes which advantageously avoid the recording or transmission of long strings of binary zeros in channel codewords may be used to ensure accurate timing and gain information.

In addition to ensuring accurate timing and gain information, modulation coding may also advantageously be used to generate a signal comprising "dc-free" channel sequences. More particularly, it is often desirable that channel sequences have a spectral null at zero (dc) frequency by which it is meant that the running digital sum (i.e. the arithmetic sum) of all the symbols transmitted in the sequence over a channel or recorded on a medium is bounded. Such sequences are said to be dc-free, and such sequences are desirable because they may provide even further noise immunity. One way to assure a dc-free sequence is to design a system in which the block digital or the arithmetic sum of symbols in a channel sequence transmitted over a channel is zero. However, efficient or high rate modulation codes, i.e., codes that can prevent long strings of zeros from occurring without adding an excessive number of symbols to the information to be recorded, that also define dc-free channel sequences, typically require complex circuitry to implement and often require large power consumption and large area on integrated circuits relative to other elements in the transmission or recording system. Similarly, systems for decoding such high rate modulation codes are also relatively complex. Thus, there is a need for an improved method and apparatus for encoding and decoding information using high rate codes that advantageously are dc-free.

SUMMARY OF THE INVENTION

In accordance with the present invention it is recognized that a channel codeword, comprising a given number of symbols and that advantageously is dc-free, may be generated based on non-dc-free codewords comprising a smaller number of symbols thereby reducing implementation complexity for generating such a channel codeword. Accordingly, a method and apparatus generate a channel codeword by selecting, for each set of input symbols in a plurality of sets of input symbols, a respective codeword, and by generating the channel codeword based on the selected respective codewords and on an additional set of input symbols, the channel codeword advantageously defining a channel sequence with a block digital sum of zero. In one embodiment, the channel codeword comprises two codewords, which two codewords were selected by respective set of input symbols, where the two codewords define respective channels sequences having block digital sums that are inverses of each other and where the ordering of the two codewords in the channel codeword is determined by an additional set of input symbols. In another embodiment, the channel codeword comprises two codewords, which two codewords were selected by respective sets of input symbols, where the two codewords define respective channels sequences having identical block digital sums and where, based on an additional set of input symbols, the symbols in, and thus the block digital sum of, one of the two codewords are inverted.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a system in which in the inventive method may be practiced;

FIG. 2 is a block diagram of a first embodiment of a system for generating dc-free sequences.

FIG. 3 is a block diagram of a second embodiment of a system for generating dc-free sequences.

FIG. 4 is a block diagram of a third embodiment of a system for generating dc-free sequences.

FIG. 5 is a block diagram of a fourth embodiment of a system for generating dc-free sequences.

FIG. 6 is a block diagram of a decoding system advantageously used with the system of FIG. 2.

FIG. 7 is a block diagram of a decoding system advantageously used with the system of FIG. 3.

FIG. 8 is a block diagram of a decoding system advantageously used with the system of FIG. 4.

FIG. 9 is a block diagram of a decoding system advantageously used with the system of FIG. 5.

DETAILED DESCRIPTION

FIG. 1 is a block diagram of a system in which the inventive method may be practiced. In particular, the system of FIG. 1 is useful for recording and reading information via a magnetic medium such as digital audio tape and disk drives.

The information is first advantageously compressed using Lempel-Ziv compressor 110 so as to reduce the amount of information that must be recorded on the medium thereby saving time and money (e.g. by permitting additional information to be recorded on a given amount of recording medium or be requiring less of the medium for holding a given amount of information). Next, the compressed information is advantageously input to encoder 120 which encodes the compressed information using Reed-Solomon codes. The purpose of Reed-Solomon encoding is to introduce extra information into the compressed information to reduce errors introduced in the reading process. Lempel-Ziv and Reed-Solomon encoding are described in greater detail in Timothy C. Bell et al., *Text Compression*, Prentice-Hall, Englewood Cliffs, N.J., 1990 and S. Lin and D. J. Costello, *Error Control Coding*, Prentice-Hall, Englewood Cliffs, N.J., 1983, respectively.

The output of encoder 120 is a series of symbols where each symbol is represented by a set of one or more bits. The symbols are input to modulation coder 130 which generates an N-symbol codeword defining a channel sequence that is transmitted through channel or recorded on medium 140.

The channel sequence is received in equalizer 150 which compensates for distortions (e.g. in frequency and phase) introduced in channel 140. Modulation decoder 160 and Reed-Solomon decoder 170 reverse the encoding processes of modulation encoder 130 and Reed-Solomon encoder 120, respectively. The information is then recovered by decompressing in Lempel-Ziv decompressor 180 the output of Reed-Solomon decoder 170.

Recall that it is often advantageous that a channel sequence have a spectral null at zero (dc) frequency. It has been shown that the power density function of a channel sequence x comprising symbols x_j, (i.e. $x = \ldots x_{-1}, x_0, x_1, \ldots$), vanishes at zero frequency if and only if its running-digital-sum (RDS), defined as

$$RDS_i = \sum_{j=-\infty}^{i} x_j$$

is bounded. It is known how to encode sequences of arbitrary symbols into channel sequences with bounded RDS's by means of dc-free modulation codes which codes may be finite-state codes or block codes. However, such encoding techniques are complex and require extensive circuitry to implement. See, R. Karabed and P. H. Siegel, "Matched spectra-null codes for partial response channels," *IEEE*

Trans. Inf. Theory, Vol. 28, No. 2, pp. 435–439, March 1991; K. J. Knudson, J. K. Wolf and L. B. Milstein, "A concatenated decoding scheme for (1-D) partial response with matched spectral-null coding," *Proc.* 1993 *IEEE Global Telecomm. Conf.* (GLOBECOM '93), Houston, Tex., pp. 1960–1964, November 1993.

Finite state codes are those in which the coded output depends on both the current input and the current state of the coder where the current state is, in turn, a function of prior inputs. Block codes, on the other hand, take blocks of M symbols, called information words, and map them into blocks of N channel symbols called codewords. Several factors favor the use of block codes. One such factor is limited error propagation since the block codes encode without memory, i.e. the symbols used to encode one block are not used in encoding any other block and thus errors in encoding are typically confined to a particular block. Another factor is ease of implementation. The simplest way to organize a one-to-one mapping of information words to codewords is to form a codebook of 2^M codewords and use an M-symbol input word to specify an N-symbol codeword in the codebook. The ratio M/N defines the rate R of the modulation code. Note that when decoding a received codeword, the M-symbol information word may be recovered, for example, by inverting the mapping or by combinatorial logic circuits in an inverse codebook.

One way to ensure that an arbitrary sequence of codewords has a bounded RDS, each codeword $w = w_1, w_2, \ldots w_N$ is required to have a block digital sum (BDS), defined as

$$BDS = \sum_{j=1}^{N} w_j$$

equal to zero. Codewords defining sequences of bipolar symbols, e.g. codewords with bipolar symbols +1 and −1, with BDS equal to zero are possible only if the codeword length N is even and if half the symbols are −1 and half the symbols are +1. The number of such codewords is then equal to

$$\binom{N}{N/2}.$$

Note, however, that at most 2^M codewords defining sequences with BDS zero can be used to form a codebook for an M/N rate code, where

$$M = \text{floorlog}\binom{N}{N/2},$$

and where the function floor(x) returns the largest integer less than or equal to x.

The above explanation is rendered more clear by use of a specific example. Consider the block length N of a sequence to be 4. There are 16 possible sequences of symbols as shown in Table 1 below, and 6 of these sequences are dc-free as indicated by the asterisks. Note, however, that since the number of codewords in a codebook is advantageously a power of 2, the codebook of length N in this example will be four, and two of the dc-free codewords in Table 1 will not be used thereby lowering the code rate. Table 2 below lists the codebook size and maximum code rate for different values of N where N is a dc-free sequence. Note that in some cases the requirement that

$$M = \text{floorlog}\binom{N}{N/2},$$

causes a substantial number of extra dc-free sequences not to be used. For example, if N=8, then the number of DC free sequences is 70, the code rate is 0.75 with the codebook of size 64, and 6 dc-free sequences are not used. However, if N=10 there are 252 possible dc-free sequences. The codebook is of size 128, and 124 sequences are discarded thereby lowering the code rate to 0.70.

In some applications, e.g. in magnetic recording applications, it is advantageous that modulation codes have rates higher than 3/4 so that a large percentage of the channel sequence represents information and a small portion represents coding. According to Table 2 below, large block length codes and large codebooks are typically required for rates above 3/4. For example, a code of rate 11/14 requires a block length of 14 and a codebook size of 2048 codewords, and a code of rate 13/16 requires a block length of 16 and a codebook of size 8192 codewords. Large codebook size is typically not an advantage when implementing coders since large codebooks require both more time to access codewords stored in the codebooks and more space in an integrated circuit than smaller codebooks. Although some schemes have been proposed to reduce the size of codebooks while maintaining the rate of a given code, these techniques add additional complexity and do not substantially reduce the size of the codebooks.

In accordance with the present invention a coding scheme is proposed which may advantageously reduce the codebook size for a given code rate. The inventive method recognizes that in prior block coding techniques used to generate dc-free modulation codes, each codeword in a codebook was required to define a sequence having a BDS equal to zero to ensure that an arbitrary sequence of codewords had a bounded RDS. In the inventive method, however, information words are applied to modulation coder to select codewords defining sequences with arbitrary or non-restricted BDS. The selected codewords will then be used to generate an output codeword which advantageously defines a dc-free sequence.

FIG. 2 illustrates a first embodiment of the inventive method for generating dc-free sequences. In this embodiment q groups of information words of m symbols and a group of p symbols are input to modulation coder 130. Each group of m input symbols is used to select an n symbol codeword from codebook 210. Codebook 210 advantageously comprises 2^m codewords where the BDS of the symbols in the sequence defined by each codeword is x. Codebook 210 is advantageously implemented in a memory device such as read only memory or random access memory. The codewords selected by the set of input symbols $\{m_1, m_2, \ldots m_q\}$ are $\{n_1, n_2, \ldots n_q\}$ respectively. The group of p input symbols are input to control codebook 230 which contains 2^p codewords defining sequences of bipolar symbols of length q where each sequence has a BDS of zero. The group of p symbols selects a codeword, termed a control codeword, from control codebook 230 which is then input, along with the set of codewords $\{n_1, n_2, \ldots n_q\}$ to inverter 220. Each of the q codewords is associated with one of the q symbols in the control codeword. Inverter 220 inverts the symbols in half of the codewords according to associated symbol in the control word. Thus after inversion, half of the codewords define a sequence with a BDS of x, and half a BDS of −x, and the output codeword (i.e. the group of codewords $\{n_1, n_2, \ldots n_q\}$ as processed by inverter 220) defines a sequence with a BDS of zero.

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To illustrate the above example in a specific context using the inventive method, consider the rate 11/14 code of Table 2 which in prior techniques requires a codebook of size 2048 codewords. In the inventive method as illustrated in FIG. 2, a single codebook (i.e. codebook 210 in FIG, 2) of 7-symbol codewords defining sequences with BDS equal to +1 may be used (e.g. 4 of the symbols in the sequence are +1, and 3 of the symbols are −1). There are

$$\binom{7}{3} = 35$$

such codewords defining sequences with BDS=1, and $32=2^5$ of the codebook are selected for codebook 210. Note that if the sign of each symbol of a codeword in the codebook is inverted, the resulting inverted codeword defines a sequence with a BDS equal to −1. Thus, a rate 11/14 dc-free code can be generated using the method of FIG. 2, as follows. The 11 input symbols are divided into q=2 groups of m=5 symbols and another group of p=1 symbol. The first and second groups of m=5 symbols select respective 7-symbol codewords in codebook 210. The p=1 symbol specifies which of the two selected codewords is to have its symbols inverted in inverter 220 thereby yielding a dc-free output codeword comprising a 7-symbol sequence of BDS=+1 and a 7-symbol sequence of BDS=−1. More formally, the p=1 input symbol can be used to select one of two codewords, either the codeword defining the sequence (−1,1) or the codeword defining the sequence (1,−1), in control codebook 230 as the control word where (−1,1) indicates the symbols of the first 7-symbol codeword are inverted and where (1,−1) indicates the symbols of the second 7-symbol codeword are inverted.

The implementation of FIG. 2 can be used in a variety of contexts. For example, the BDS of sequences defined by codewords in codebook 210 need not be +1. The BDS may be any value as long as 2^m entries are available for codebook 210.

Another embodiment of the present invention is illustrated in FIG. 3 where q groups of m symbols and a group of p symbols are input to modulation coder 130. Each group of m input symbols is used to select a codeword from a respective codebook 310-j, j=1,2, . . . q. Codebook 310-j advantageously comprises 2^m codewords where all codewords in codebook 310-j define sequences with the same BDS, i.e. BDS_j. Further,

$$\sum_{j=1}^{q} BDS_j = 0.$$

The group of p input symbols are input to control codebook 330 which contains 2^p codewords of length q where the control codebook comprises codewords defining sequences with a BDS of zero. The group of p symbols selects a control codeword from control codebook 330 which is input, along with the selected codewords $\{n_1, n_2 \ldots n_q\}$ to orderer 320. Orderer 320 orders or concatenates the codewords according to a rule prescribed by the p symbols, e.g. the output of orderer 320 is $\{n_q, n_2, \ldots n_1\}$. Thus, since one codeword is selected from each codebook and since

$$\sum_{j=1}^{q} BDS_j = 0,$$

the output codeword generated by the system in FIG. 3 defines a sequence with BDS=0.

To illustrate the second embodiment in a specific example, again consider the rate 11/14 code of Table 2. In the second embodiment, two codebooks, 310-1 and 310-2

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are used. Codebook 310-1 contains thirty-two 7-symbol codewords defining sequences with BDS equal to +1. Codebook 310-2 contains thirty-two 7-symbol codewords defining sequences with BDS equal to −1. The rate 11/14 dc-free code can be generated using the method and apparatus of FIG. 3 as follows. The 11 input symbols are divided into two groups of five symbols and another group of one symbol. Each group of five symbols selects a codeword from a respective codebook. The single symbol specifies which of the two selected codewords is to be output first by orderer 320 thereby yielding a dc-free output codeword defining a channel sequence comprising a 7-symbol sequence of BDS= +1 and a 7-symbol sequence of BDS=−1.

The implementation of FIG. 3 can be expanded and is not limited by the examples given above. For example, the BDS of sequences defined by codewords in codebooks 310-j need not be +1 and −1. All that is required is that

$$\sum_{j=1}^{q} BDS_j$$

is zero. Thus, a set of four codebooks defining sequences with $BDS_1=3$, $BDS_2=1$, $BDS_3=-1$ and $BDS_4=-3$ is suitable.

FIG. 4 illustrates a third embodiment of the inventive method for generating dc-free sequences. In this embodiment q groups of m symbols and a group of p symbols are input to modulation coder 130. Each group of m symbols is used to select a codeword from codebook 420-j where the particular codebook selected for a given set of m symbols is determined by the set of p symbols. In particular, the set of p symbols is advantageously used to select a control codeword from control codebook 430 which control codeword is input to codebook selector 405. Codebook selector 405 then routes each set of m symbols to the proper codebook 420-j from which a respective codeword is then selected. As with embodiment of FIG. 3, if the jth codebook comprises codewords defining sequence with BDS_j, and if

$$\sum_{j=1}^{q} BDS_j = 0,$$

then the output codeword generated by modulation coder 130 defines a sequence that is dc-free.

In the context of the rate 11/14 code discussed above, two groups of 5 input symbols and another single input symbol can be input to modulation coder 130. Two codebooks, 410-1 and 410-2 of thirty-two 7-symbol codewords defining sequences with BDS+1 and −1, respectively, are used. The single symbol p is used to decide which group of 5 input symbols uses codebook 410-1 with the other group of 5 input symbols selecting a codeword from codebook 410-2. The resulting output codeword, based on a codeword selected from codebook 410-1 and a codeword from codebook 410-2, will define a channel sequence with a BDS of zero.

Another embodiment of the inventive method is illustrated in FIG. 5 in which q groups of m symbols and a group of p symbols are input to modulation coder 130. The group of p symbols are used both to select the codebooks and to determine which codewords are inverted. Each group of m symbols is used to select a codeword from codebook 520-j where the particular codebook selected for a given set of m symbols is determined by the set of p symbols. In particular, the set of p symbols is advantageously used to select a control codeword from control codebook 530 which control codeword is input to codebook selector 510. Codebook selector 510 then routes each set of m symbols to the proper codebook 520-j from which a respective codeword is then

selected. The routing is based on a control codeword. The control codeword is selected by applying p input symbols to control codebook **530**. The control codewords define sequences with BDS=0. Assuming that each symbol in the sequence is a bipolar symbol (e.g. a +1 or a −1) and that each symbol is associated with a codeword, those codewords associated with a −1 will be inverted and those codewords associated with a +1 will remain unchanged. For example, in FIG. **5**, codeword n_q is input to and inverted in inverter **515** and the output is designated n'_q.

The embodiment of FIG. **5** uses half as many codebooks as the embodiment of FIG. **4** but requires inverter **515**. To illustrate, if codebook **520-1** comprises codewords defining sequences with BDS=3 and codebook **520-2** comprises codewords defining sequences with BDS=1, a dc-free sequence can be generated by selecting a group of 3 codewords from the BDS=1 codebook and second group comprising one codeword from the BDS=3 codebook and inverting symbols in one of the groups. In contrast to a corresponding system using the arrangement of FIG. **4**, the system of FIG. **5** eliminates the need for codebooks comprising codewords defining sequences of BDS=−3 and BDS=−1.

FIG. **6** illustrates a modulation decoder **160** that can be used with the system of FIG. **2**. A read or received channel sequence generates a codeword, herein termed an input codeword, which is broken down into q codewords of length n symbols where each codeword defines a portion of the read or received sequence. Let the prime (') designation indicate a codeword defining a portion sequence with a negative BDS, as achieved for example by inverting a sequence with a positive BDS. Assume for illustrative purposes that the received codeword FIG. **6** is $\{n_1, n'_2, \ldots n_q\}$. The BDS for the jth sequence defined by the jth codeword is determined in BDS check **602-j**. Assuming the BDS of sequences defined by codewords in codebook **210** of FIG. **2** is x, then codewords defining sequences with BDS=−x in FIG. **6** will have their symbols inverted in BDS check **610-j** so that all received codeword will define sequences that have a BDS of x. Each codeword defining the BDS=x sequence will then be input to inverse codebook **620**. Inverse codebook **620** outputs, advantageously based on knowledge of codebook **210** of FIG. **2**, for each codeword, the m input symbol information word corresponding to the codeword. BDS check **602-j** also generates check symbols, depending on whether the BDS of the defined sequences j was +x or −x. The check symbols are input to inverse control codebook **630** to determine, advantageously based on knowledge of control codebook **230**, the set of p input symbols used to generate the control codeword in FIG. **2**.

FIG. **7** illustrates a decoding system advantageously used with the system of FIG. **3**. A read or received channel sequence generates an input codeword, which is broken down into q codewords of length n symbols where each codeword defines a portion of the read or received sequence. The BDS of each sequence defined by the codewords is determined in BDS check **702-j**. The codeword and the BDS value of the corresponding defined sequence are input to router **705**. Depending on the BDS value of a defined sequence, router **705** directs the corresponding codeword to one inverse codebook **710-j**. Inverse codebook **710-j** advantageously operates in a manner similar to inverse codebook **620** of FIG. **6** in that, based on knowledge of codebooks **310-j** used to generate the codewords from the information words, the m symbol input information words can be determined. An additional set of p symbols is decoded by receiving from each BDS check **702-j** a respective check

symbol representing the BDS value of the jth received codeword. These values correspond to symbols in a control codeword and are input to inverse control codebook **730** which, based on knowledge of control codebook **330**, can be used to identify the p symbols used to generate the control word that ordered the codewords during the encoding process.

FIG. **8** illustrates a decoding system advantageously used with the system of FIG. **4**. A read or received channel sequence generates an input codeword, which is broken down into q codewords of length n symbols where each codeword defines a portion of the read or received sequence. The BDS of the sequence defined by each codeword is determined in BDS check **802-j**. The codeword and the BDS value of the corresponding defined sequence are input to router **805** and the codeword is routed to inverse codebook **810-j** based on the BDS value of the corresponding sequence. Marcher **810-j** generates an m symbol information word advantageously based on knowledge of codebook **420-j**. An additional set of p symbols can be determined by receiving from BDS check **802-j** the BDS value defined by the jth received codeword. These values correspond to symbols in a control codeword and are input to inverse control codebook **830** which, based on knowledge of control codebook **430**, can the generate the p symbols.

FIG. **9** illustrates a decoding system advantageously used with the system of FIG. **5**. A read or received channel sequence generates an input codeword, which is broken down into q codewords of length n symbols where each codeword defines a portion of the read or received sequence. The prime designation (') indicates a sequence where the symbol were inverted. The BDS of each codeword is determined in BDS check **902-j**. Codewords defining sequences that were inverted in the encoding process, as evidenced for example by a negative BDS value, are inverted in BDS check **902-j**. The additional p information symbols are determined by receiving from BDS check **902-j** the BDS value of the jth received codeword. These values correspond to symbols in a control codeword and are input to inverse control codebook **930** which, based on knowledge of control codebook **530**, can the generate the p symbols. The codewords and the BDS value are then input into router **905**. Router **905** directs the n symbol codeword to inverse codebook **910-i**. The routing is advantageously based on the BDS value. Inverse codebook **910-i** operates in a fashion similar to the inverse codebooks described above to generate q sets of m information symbols.

This disclosure describes a method and apparatus for modulation encoding. The apparatus and method disclosed herein have been described without reference to specific hardware or software. Instead, the method and apparatus have been described in such a manner that those skilled in the art can readily adapt such hardware and software as may be available or preferable for particular applications. While the above teachings of the present invention have been in terms of modulation coding for a magnetic recording/writing channel, these skilled in the art will recognize the applicability of these teachings to other specific contexts. For example the above teachings are not limited to magnetic recording/writing channels. Likewise, the above teachings are not limited to the particular arrangements shown in the figures above where, for example, the parallel processing of q codewords through q BDS checks could be replaced by serially processing the q codewords through a single BDS check. Further, the above teachings may be extended to include generating output codewords defining sequences having non-zero BDS values which codewords are useful in optical communications.

TABLE 1

1	1	1	1	
1	1	1	−1	
1	1	−1	1	
1	1	−1	−1	*
1	−1	1	1	
1	−1	1	−1	*
1	−1	−1	1	*·
1	−1	−1	−1	
−1	1	1	1	
−1	1	1	−1	*
−1	1	−1	1	*
−1	1	−1	−1	
−1	−1	1	1	*
−1	−1	1	−1	
−1	−1	−1	1	
−1	−1	−1	−1	

TABLE 2

N	R	codebook size
2	1/2 = .5	2
4	2/4 = .5	4
6	4/6 = .667	16
8	6/8 = .75	64
10	7/10 = .70	128
12	9/12 = .75	512
14	11/14 = .786	2048
16	13/16 = .813	8192

I claim:

1. A method comprising the steps of:

selecting, for each set of input symbols in a plurality of sets of input symbols, a respective codeword, and

generating a channel codeword based on the selected respective codewords and on an additional set of input symbols, said channel codeword defining a channel sequence, wherein the block digital sum of the defined channel sequence is zero.

2. The method of claim 1 wherein the step of generating a channel codeword comprises the step of:

ordering said respective codewords based on said additional set of input symbols.

3. The method of claim 2 wherein the step of selecting comprises the steps of, for each set of input symbols:

choosing a codebook from among a plurality of codebooks wherein each codebook in the plurality of codebooks comprises codewords,

choosing said respective codeword from among codewords in the selected codebook based on said each set of input symbols.

4. The method of claim 1 wherein the step of generating a channel codeword comprises the steps of:

inverting codeword symbols in particular respective codewords based on said additional set of input symbols.

5. The method of claim 4 wherein, for each set of input symbols, the selected codewords are selected from among codewords in a single codebook.

6. The method of claim 1 wherein said channel codeword is recorded on a magnetic medium.

7. The method of claim 1 wherein said channel codeword is transmitted over a communications channel.

8. A method comprising the steps of:

for each set of input symbols in a plurality of sets of input symbols, selecting a respective codeword from among codewords in a set of one or more codebooks, wherein each respective codeword defines a respective portion of a channel sequence comprising channel symbols, the

channel symbols in the respective portions having an associated block digital sum, and wherein the sum of the block digital sums of the respective portions is zero, and

generating an channel codeword by concatenating, in an order of concatenation determined by a separate set of input symbols, the respective codewords.

9. The method of claim 8 wherein the step of selecting a respective codeword further comprises the steps of:

selecting, from a first codebook, a first respective codeword for a first set of input symbols, the selecting being based on said first set of input symbols, and

selecting, from a second codebook, a second respective codeword for a second set of input symbols, the selecting being based on said second set of input symbols.

10. The method of claim 9 wherein the channel symbols in the respective portion of a channel sequence defined by said first respective codeword has a block digital sum of x, and wherein the channel symbols in the respective portion of a channel sequence defined by said second respective codeword has a block digital sum of −x.

11. The method of claim 10 wherein said different set of input symbols comprises a single bit having a status and where said order of concatenation is indicated by said status.

12. A method comprising the steps of:

for each set of input symbols in a plurality of sets of input symbols, selecting a respective codeword comprising symbols, and

inverting codeword symbols in particular respective codewords, the particular respective codewords being selected based on a different set of input symbols,

generating a channel codeword based on said codewords, wherein said channel codeword defines a channel sequence comprising channel symbols and wherein the block digital sum of said channel sequence is zero.

13. The method of claim 12 wherein the step of generating comprises the step of:

selecting, based on symbols in said different set of input symbols, a control codeword from a control codebook, the control codeword comprising a number of control symbols equal to the number of respective codewords, each control symbol in the control codebook have a status, and

for each respective codeword, inverting the symbols in the selected codeword according to the status of a respective control symbol in said control codebook.

14. The method of claim 13 wherein said control codeword defines a channel sequence with a block digital sum of zero.

15. A method of generating a channel codeword, said channel codeword defining a channel sequence having a block digital sum of a specified value, said method comprising the steps of:

selecting, for each set of input symbols in a plurality of sets of input symbols, a respective codeword, wherein said respective codeword is associated with a respective channel sequence having an associated block digital sum, and

generating said channel codeword based on said respective codewords and on said respective block digital sums, wherein said channel sequence defined by said channel codeword has a block digital sum equal to said specified value.

16. The method of claim 15 wherein said specified value is zero.

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17. The method of claim 15 wherein the step of selecting comprises the step of:

for each set of input symbols, choosing a codeword from a codebook as said respective codeword.

18. The method of claim 17 wherein the step of choosing comprises the step of:

selecting, according to a first other set of input symbols, a codebook from among a plurality of codebooks, each codebook in said plurality of codebooks comprising codewords, wherein the chosen codeword is selected from among codewords in the chosen codebook.

19. The method of claim 15 or 18 wherein the step of generating comprises:

ordering said respective codewords based on a second other set of input symbols.

20. The method of claim 15 or 18 wherein each respective codeword comprises symbols and wherein the step of generating comprises:

inverting symbols in particular respective codewords based on a second other set of input symbols.

21. The method of claim 19 wherein the step of ordering comprises the steps of:

selecting, based on said second other set of input symbols, a control codeword, said control codeword comprising control symbols, wherein a channel sequence defined by said control codeword has a block digital sum of zero, and

ordering said respective codewords based on the control symbols in said selected control codeword.

22. The method of claim 20 wherein the step of inverting comprises the steps of:

selecting, based on said second other set of input symbols, a control codeword, said control codeword comprising control symbols, wherein a channel sequence defined by said control codeword has a block digital sum of zero, and

inverting symbols in said respective codewords based on said control symbols in said selected control codeword.

23. The method of claim 16 further comprising the step of:

recording said defined channel sequence on a magnetic medium.

24. The method of claim 16 further comprising the step of:

transmitting said defined channel sequence over a communications channel.

25. A method comprising the steps of:

for each portion in a plurality of portions of an input codeword, wherein each portion defines a corresponding portion of a channel sequence comprising channel symbols, wherein each portion of said input codeword comprises symbols, generating a respective set of output symbols, and

generating, based on the block digital sum of the channel symbols in the portion of the channel sequence corresponding to each portion of said input codeword, an additional set of output symbols.

26. The method of claim 25 wherein the step of generating a respective set of output symbols comprises the step of:

selecting for each portion of said input codeword, based on the symbols in said each portion, an entry from among one or more entries in a codebook, the selected entry comprising said respective set of output symbols.

27. The method of claim 26 wherein the step of selecting an entry comprises the step of:

selecting, based on the block digital sum of channel symbols in the channel sequence corresponding to said

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portion, said codebook from among a plurality of codebooks.

28. The method of claim 26 further comprising the step of:

for portions of said channels sequence having a negative block digital sum, inverting symbols in corresponding portions in said input codeword.

29. The method of claim 25 wherein said input codeword is received over a communications channel.

30. The method of claim 25 wherein said input codeword is read from a magnetic recording channel.

31. The method of claim 25 wherein the block digital sum of said portions of said channel sequences corresponding to said portions in said input codeword is zero.

32. The method of claim 25 wherein said input codeword comprises a first portion defining a first portion of said channel sequence wherein the block digital sum of said first portion of said channel sequence is x and wherein said input codeword comprises a second portion defining a second portion of said channel sequence wherein the block digital sum of said second portion of said channel sequence is −x.

33. An apparatus for generating a channel codeword, said channel codeword defining a channel sequence having a block digital sum of a specified value, said apparatus comprising:

means for selecting, for each set of input symbols in a plurality of sets of input symbols, a respective codeword, wherein said respective codeword is associated with a respective channel sequence having an associated block digital sum, and

means for generating said channel codeword based on said respective codewords and on said respective block digital sums, wherein said channel sequence defined by said channel codeword has a block digital sum equal to said specified value.

34. The apparatus of claim 33 wherein said specified value is zero.

35. The apparatus of claim 33 wherein the means for selecting comprises:

means for choosing, for each set of input symbols, a codeword from a codebook as said respective codeword.

36. The apparatus of claim 35 wherein the means for choosing comprises:

means for selecting, according to a first other set of input symbols, a codebook from among a plurality of codebooks, each codebook in said plurality of codebooks comprising codewords, wherein the chosen codeword is selected from among codewords in the chosen codebook.

37. The apparatus of claim 33 or 36 wherein the means for generating comprises:

means for ordering said respective codewords based on a second other set of input symbols.

38. The apparatus of claim 33 or 36 wherein each respective codeword comprises symbols and wherein the means for generating comprises:

means for inverting symbols in particular respective codewords based on a second other set of input symbols.

39. The apparatus of claim 37 wherein the means for ordering comprises:

means for selecting, based on said second other set of input symbols, a control codeword, said control codeword comprising control symbols, wherein a channel sequence defined by said control codeword has a block digital sum of zero, and

means for ordering said respective codewords based on the control symbols in said selected control codeword.

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40. The apparatus of claim **38** wherein the means for inverting comprises:

means for selecting, based on said second other set of input symbols, a control codeword, said control codeword comprising control symbols, wherein a channel sequence defined by said control codeword has a block digital sum of zero, and

means for inverting symbols in said respective codewords based on said control symbols in said selected control codeword.

41. The apparatus of claim **34** further comprising:

means for recording said defined channel sequence on a magnetic medium.

42. The apparatus of claim **34** further comprising:

means for transmitting said defined channel sequence over a communications channel.

43. An apparatus comprising

for each portion in a plurality of portions of an input codeword, wherein each portion defines a corresponding portion of a channel sequence comprising channel symbols, wherein each portion of said input codeword comprises symbols, means for generating a respective set of output symbols, and

means for generating, based on the block digital sum of the channel symbols in the portion of the channel sequence corresponding to each portion of said input codeword, an additional set of output symbols.

44. The apparatus of claim **43** wherein the means for generating a respective set of output symbols comprises:

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means for selecting for each portion of said input codeword, based on the symbols in said each portion, an entry from among one or more entries in a codebook, the selected entry comprising said respective set of output symbols.

45. The apparatus of claim **44** wherein the means for selecting an entry comprises:

means for selecting, based on the block digital sum of channel symbols in the channel sequence corresponding to said portion, said codebook from among a plurality of codebooks.

46. The apparatus of claim **44** further comprising:

for portions of said channels sequence having a negative block digital sum, means for inverting symbols in corresponding portions in said input codeword.

47. The apparatus of claim **43** wherein said input codeword is received over a communications channel.

48. The method of claim **43** wherein said input codeword is read from a magnetic recording channel.

49. The apparatus of claim **43** wherein the block digital sum of said portions of said channel sequences corresponding to said portions in said input codeword is zero.

50. The apparatus of claim **43** wherein said input codeword comprises a first portion defining a first portion of said channel sequence wherein the block digital sum of said first portion of said channel sequence is x and wherein said input codeword comprises a second portion defining a second portion of said channel sequence wherein the block digital sum of said second portion of said channel sequence is −x.

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