Coding for Increased Distance With a d=0 FDTS/DF Detector

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Summary

Examination of the most likely error sequences for FDTS/DF with a d=0 code indicates that ±(...,-2,+2,-2,...) results from confusing the sequences separated by β_{min}. This suggests that the use of a d=0 code that suppresses sequences that could generate these errors would provide an increased signal margin. One of the sequences pairs that generates the minimum distance error must contain three or more consecutive transitions. Thus, the objective of the coding is to prevent tribit or longer transition runs.

A convenient way of viewing the required code constraint is to apply a (d,k) = (0,2) constraint such that the output is assumed to be NRZI data rather than NRZ. A rate 4/5 block code that meets this constraint exists. However, codes with higher rates can be found to meet the (0,2) constraint. Simulations show that significant improvements result from the use of a 16/19 block code. A word of caution: the amount of improvement will depend on the particular pulse response, but these codes will yield an improvement for densities of 2.5 or higher (assuming the ±(-2,+2,-2) sequence has minimum distance).

An example of how a linear boundary may be implemented for a signal space detector (SSD) as previously presented is included for reference. Also, a detector using a signal dependent threshold is shown. This is unlikely to be useful for large tree depths (τ), but may be of interest at a lower complexity.

Description of Codes

Figure 1 shows the state diagram for a (d,k) = (0,2) code with no constraint on the number of consecutive 0's. The capacity of this code is C = 0.8791, which is less than 8/9.

A 4/5 block code exists (shown in Figure 2) with the (0,2) constraint. This has a maximum of 8 consecutive 0's, or a minimum transition spacing of 9T.

To increase the code rate, a block code with rate 16/19 = 0.8421 exists. A state diagram for this code is given in Figure 3. This diagram yields a capacity of 0.8732.

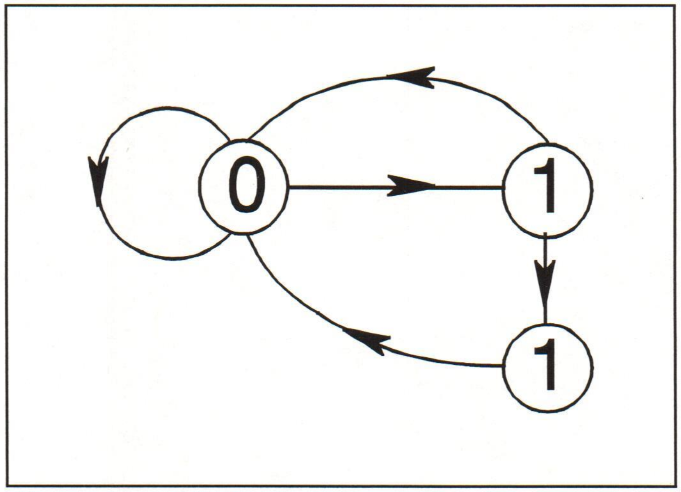

Figure 1. (0,2) Code

Table I. Detector Rate to Obtain 100 Mbit/sec

Code	Rate	Detector Frequency
(0,4/4)	8/9	113 MS/s
(0,2)	12/14	117 MS/s
(0,2)	16/19	119 MS/s
(0,2)	8/10	125 MS/s
(1,7)	2/3	150 MS/s

0000	↔	00001
0001	↔	00010
0010	↔	00100
0011	↔	00101
0100	↔	00110
0101	↔	01000
0110	↔	01001
0111	↔	01010
1000	↔	01100
1001	↔	01101
1010	↔	10000
1011	↔	10001
1100	↔	10010
1101	↔	10100
1110	↔	10101
1111	↔	10110

Figure 2. A Rate 4/5 (0,2) Block Code

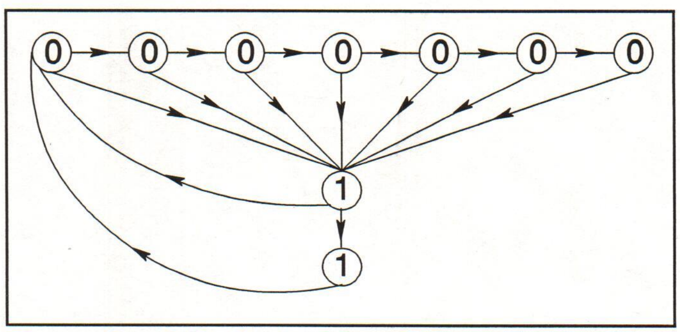

Figure 3. (0,2) Code, Max. 8T spacing for 1's

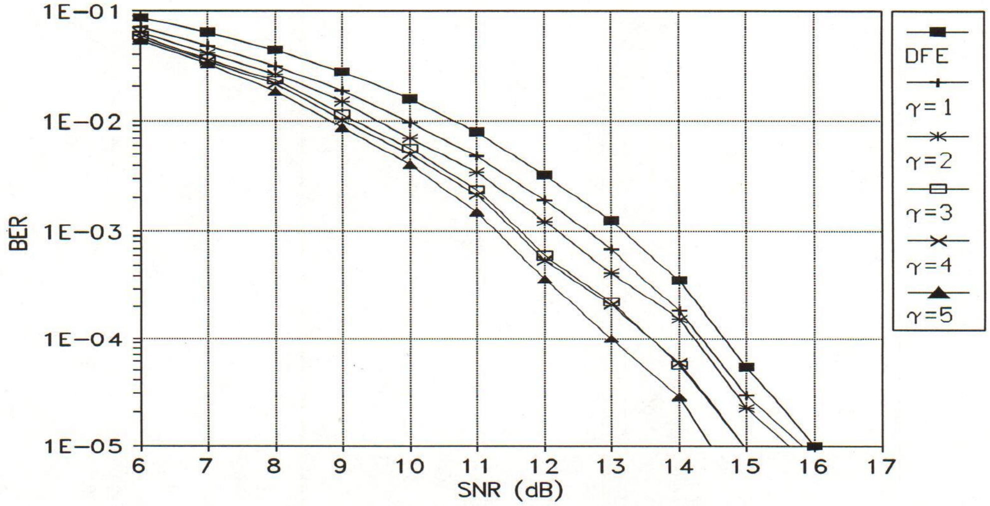

Figure 4. D_u=2.5: (d,k) = (0,4) Rate 8/9 Code

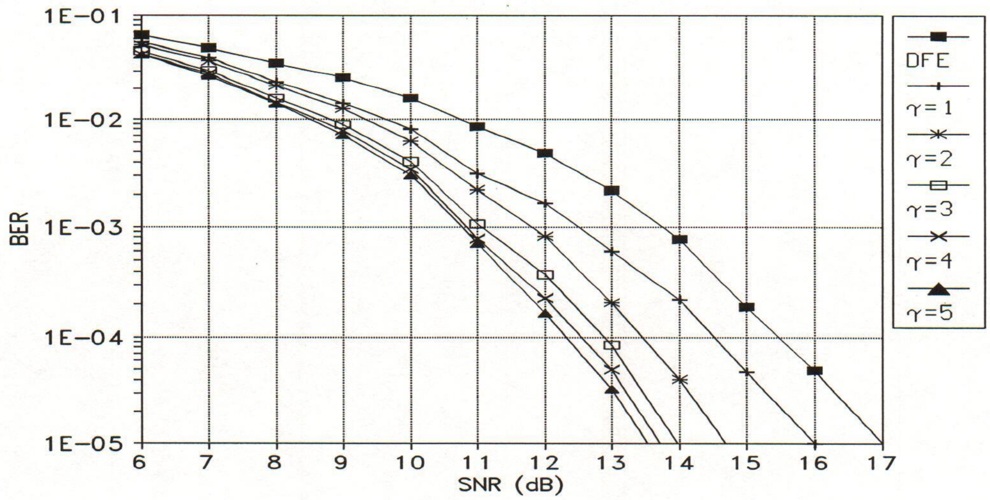

Figure 5. D_u=2.5: (d,k) = (0,8), NRZI (0,2), Rate 4/5 Block Code

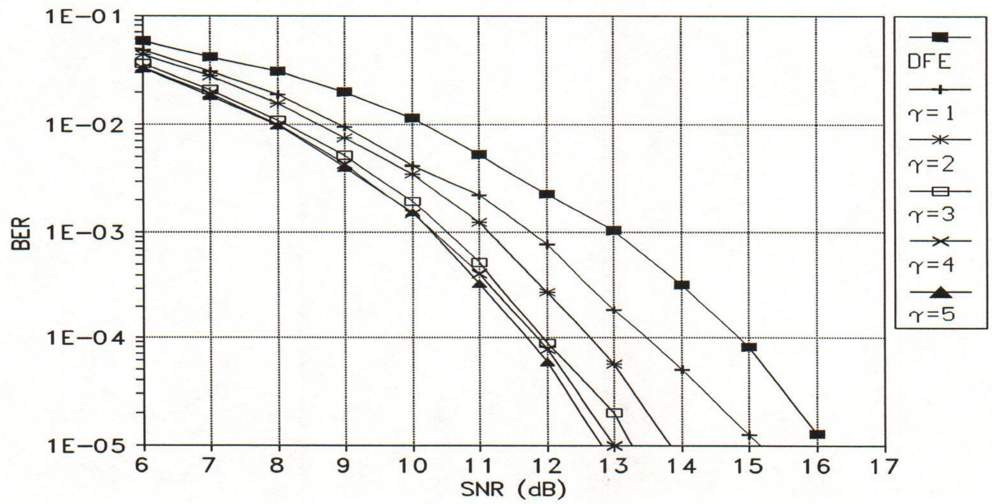

Figure 6. D_u=2.5: (d,k) = (0,7), NRZI (0,2) Rate 16/19 Block Code

SSD Using Piecewise Linear Boundaries

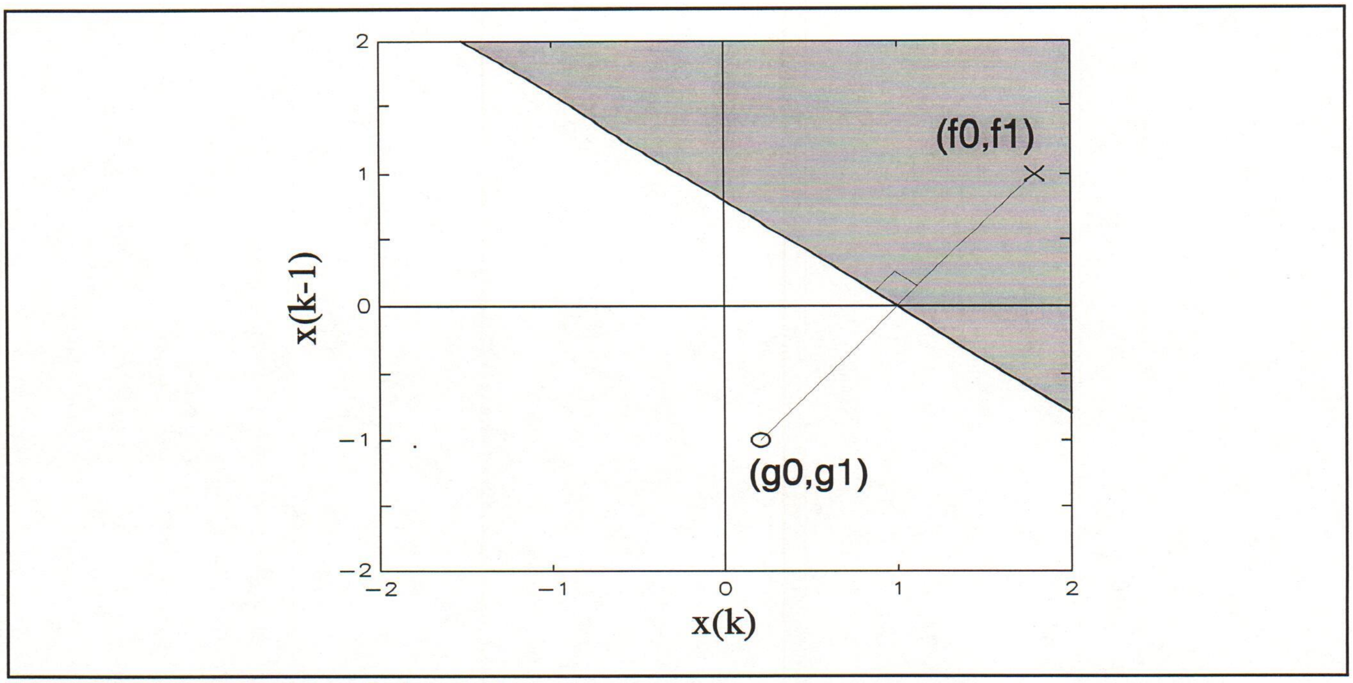

Figure 7. Separating Two Points in Space

$$\sum_{i=0}^{\tau} (f_i - x_i)^2 = \sum_{i=0}^{\tau} (g_i - x_i)^2$$

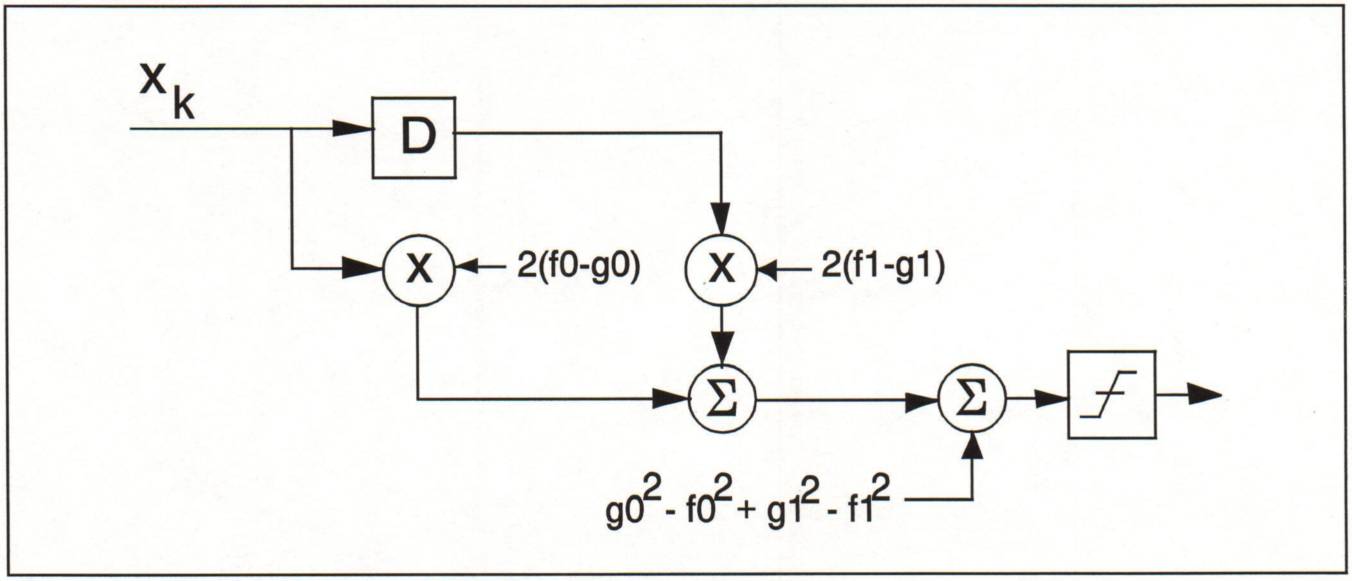

Figure 8. Boundary Using an FIR Filter

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