UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CISCO SYSTEMS, INC.,
Petitioner,

v.

EGENERA, INC.,
Patent Owner.

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Case IPR2017-01340
Patent 6,971,044 B2

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Before MELISSA A. HAAPALA, *Acting Vice Chief Administrative Patent Judge*, KRISTEN L. DROESCH and CHARLES J. BOUDREAU, *Administrative Patent Judges*.

HAAPALA, *Acting Vice Chief Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

Cisco Systems, Inc. ("Petitioner") filed a Petition pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–6 of U.S. Patent No. 6,971,044 B2 ("'044 patent"). Paper 1 ("Pet."). Egenera, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Applying the standard set forth in 35 U.S.C. § 314(a), we granted Petitioner's request and instituted an *inter partes* review of all challenged claims. Paper 7 ("Dec.").

During the trial, Patent Owner timely filed a Response (Paper 18, "PO Resp."), to which Petitioner timely filed a Reply (Paper 25, "Reply"). An oral hearing was held on July 25, 2018, and a copy of the transcript was entered into the record. Paper 32 ("Tr.").

Additionally, Patent Owner filed a Motion to Exclude Evidence (Paper 29, "Mot. To Exclude"), to which Petitioner filed an Opposition (Paper 31,"Mot. Opp.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of the claims on which we instituted trial. Based on the record before us, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6 of the '044 patent are unpatentable.

I. BACKGROUND

A. *The '044 Patent (Ex. 1001)*

The '044 patent describes processing systems having virtualized communication networks and storage for quick deployment and reconfiguration. Ex. 1001, 1:17–19. The platform provides a large pool of processors from which a subset may be selected and configured through software commands to form a virtualized network of computers that may be

deployed to serve a given set of applications or customer. *Id.* at 2:59–64.

The virtualization may include virtualization of local area networks (LANs)

or the virtualization of I/O storage. *Id.* at 2:67–3:2.

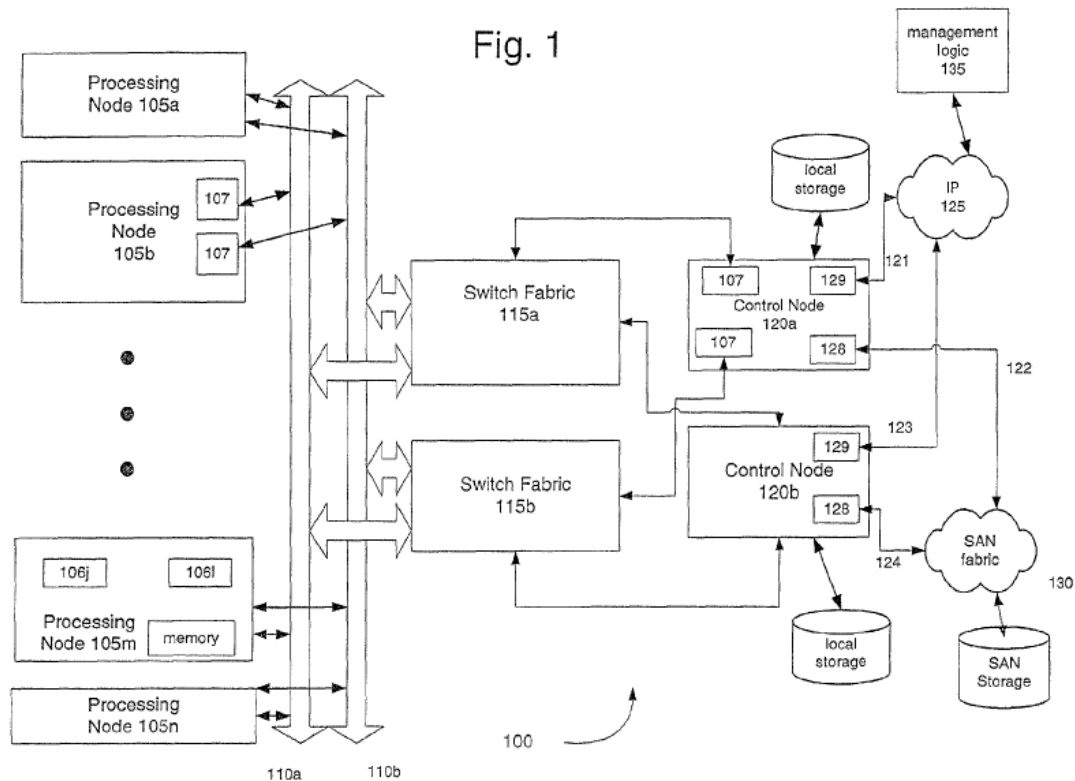Figure 1 of the '044 patent is reproduced below:

Fig. 1

Figure 1 depicts hardware platform 100, which includes processing nodes

105a-105n connected to switch fabrics 115a, 115b via high-speed

interconnects 110a, 110b. *Id.* at 3:10–12. Switch fabrics 115a, 115b are

also connected to at least one control node 120a, 120b in communication

with external Internet Protocol (IP) network 125 and storage area network

(SAN) 130. *Id.* at 3:13–16. In some embodiments, processing nodes 105a–

105n, control nodes 120a, 120b, and switch fabrics 115a, 115b are contained

in a single chassis and interconnected via a fixed, pre-wired mesh of

point-to-point (PtP) links. *Id.* at 3:20–24. Figure 1 depicts additional

components not described.

Under software control, the platform supports multiple, simultaneous, and independent processing area networks (PANs), which are each configured to have a corresponding subset of processors that may communicate via a virtual local area network emulated over the PtP mesh. *Id.* at 3:65–4:3. An administrator defines the network topology of a PAN and specifies media access control (MAC) address assignments of the various nodes. *Id.* at 6:4–7. The MAC address is virtual, identifying a virtual interface, and is not tied to any specific physical node. *Id.* at 6:7–9. The virtual local area network provides communication among a set of computer processors, but excludes processors not in the defined set. *Id.* at 2:8–11. A virtual storage space is also defined and established with a defined correspondence to the address space of a storage network. *Id.* at 2:11–13.

The '044 patent further describes that the control node, via software (without any physical re-cabling), may change the PAN configuration to allow a new processor to inherit the storage and networking personality of another. *See id.* at 23:3–7, 28:14–19. This may be done to swap a new processor into a PAN to replace a failing one. *Id.* at 29:19–21. In response to a failure by a computer processor, a computer processor is allocated to replace the failed processor, and the MAC address of the failed processor is assigned to the processor that replaces the failed processor. *Id.* at 2:13–17. The virtual storage space and defined correspondence to the address space of the storage network is also assigned to the processor that replaces the failed processor. *Id.* at 2:17–19. The virtual local area network is then reestablished to include the processor that replaced the failed processor and to exclude the failed processor. *Id.* at 2:19–22.

B. Illustrative Claim

Claims 1 and 4 are independent claims. Claim 1 is illustrative of the subject matter of the claims at issue:

1. A platform for computer processing, connectable to an external communication network and a storage network and comprising:

a plurality of computer processors connected to an internal communication network;

configuration logic to define and establish (a) a virtual local area communication network over the internal network, wherein each computer processor in the virtual local area communication network has a corresponding virtual MAC address and the virtual local area network provides communication among a set of computer processors but excludes the processors from the plurality not in the defined set, and (b) a virtual storage space with a defined correspondence to the address space of the storage network; and

failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor, the failover logic including logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor, logic to assign the virtual storage space and defined correspondence of the failed processor to the processor that replaces the failed processor, and logic to reestablish the virtual local area network to include the processor that replaces the failed processor and to exclude the failed processor.

C. Instituted Grounds of Unpatentability

Petitioner relies on the following references:

1. U.S. Patent No. 6,779,016, issued Aug. 17, 2004 ("Aziz") (Ex. 1006).
2. U.S. Patent No. 6,856,591, issued Feb. 15, 2005 ("Ma") (Ex. 1007).

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