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Paper 29
Entered: November 20, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-01346
Patent 8,161,344 B2

Before MINN CHUNG, DANIEL J. GALLIGAN, and JOHN A. HUDALLA, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, NVIDIA Corporation ("Petitioner") challenges the patentability of claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 of U.S. Patent No. 8,161,344 B2 ("the '344 patent," Ex. 1001), which is assigned to Polaris Innovations Limited ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1, 4, 8–12, 16, 18, 43, 45, and 48–51 of the '344 patent are unpatentable in this proceeding but has not proven by a preponderance of the evidence that claims 2, 19, 20, 22, 26–30, and 44 are unpatentable. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

On July 25, 2017, Petitioner requested *inter partes* review of claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 of the '344 patent. Paper 2 ("Pet."). Patent Owner elected not to file a Preliminary Response. *See* Paper 7 (waiving right to file Preliminary Response). We instituted trial on all grounds of unpatentability, which are as follows:

1. Whether claims 1, 2, 4, 8–12, 19, 20, 22, 26–30, 43–45, and 48–51

are unpatentable under 35 U.S.C. § 102(b) over ADSL;[1]

2. Whether claims 16 and 18 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of ADSL and Voith;[2] and

3. Whether claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 are unpatentable under 35 U.S.C. § 103(a) over Grube.[3]

Paper 8 ("Dec. on Inst."), 23.

During the trial, Patent Owner filed a Response (Paper 14, "PO Resp."), and Petitioner filed a Reply (Paper 18, "Pet. Reply"). An oral hearing was held on August 17, 2018, a transcript of which appears in the record. Paper 25 ("Tr."). Following the hearing, with our authorization (Paper 26), the parties filed additional briefing addressing the broadest reasonable interpretation of "data arrangement alteration." Papers 27, 28.

B. Real Parties in Interest

Patent Owner identifies itself, Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 6, 2.

C. Related Matters

Petitioner and Patent Owner cite the following judicial matter involving the '505 patent: *Polaris Innovations Ltd. v. Dell Inc. & NVIDIA Corp.*, Case No. 4:16-cv-07005 (N.D. Cal.). Pet. 97; Paper 4, 2–3. The '344 patent is also at issue in IPR2017-01781, in which we are issuing a final written decision concurrently with this Decision.

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[1] American National Standard for Telecommunications – Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface, ANSI T1.413-1998 c.1 (© 1999) (Ex. 1004).
[2] US 5,737,337, issued Apr. 7, 1998 (Ex. 1006).
[3] US 5,606,577, issued Feb. 25, 1997 (Ex. 1005).

D. The '344 Patent and Illustrative Claim

The '344 patent generally relates to circuits for error coding. Ex. 1001, Abstract, 1:11–12. Figure 1A, reproduced below, illustrates an embodiment of such a circuit.

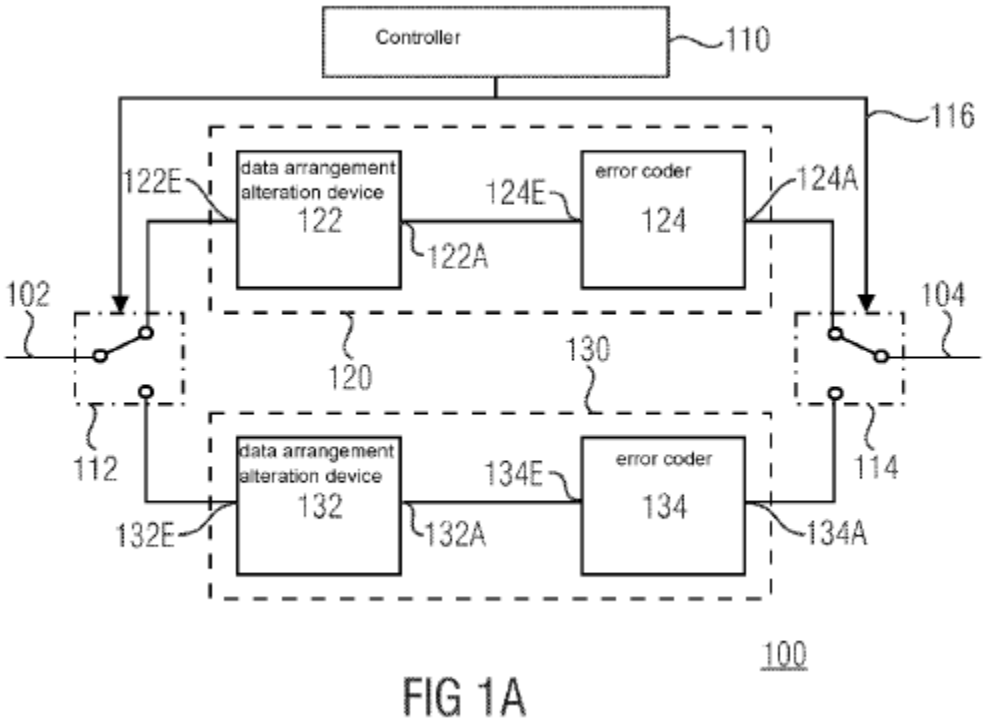

FIG 1A

Figure 1A illustrates an error coding circuit having controller 110, input 102, first error coding path 120, second error coding path 130, and output 104. Ex. 1001, 3:27–30. As illustrated in Figure 1A, each of error coding paths 120 and 130 has a data arrangement alteration device and an error coder. Ex. 1001, 3:30–34. The '344 patent explains that control indicator 116 is used to select between the first and second error coding paths. Ex. 1001, 4:41–47.

Of the claims at issue in the present proceeding, claims 1, 16, 19, and 43 are independent claims. Claim 1 is illustrative and is reproduced below.

> 1. A circuit for creating an error coding data block for a first data block, the circuit comprising:
>
> a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding; and
>
> a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding;
>
> the first error coding path and the second error coding path being selected as a function of a control indicator, and at least the first error coding path comprising a data arrangement alteration device.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Tredennick, testifies that "[a] person of ordinary skill in the art as of the time of the '344 patent (POSITA) would have had a Bachelor's degree in Electrical Engineering and at least 2 years of experience working in the field of semiconductor logic design." Ex. 1003 ¶ 13. Neither Patent Owner, nor its declarant, Dr. Przybylski, offers a different assessment of the level of ordinary skill in the art. *See* Ex. 2002 ¶ 38 ("I am applying the definition of the level of experience of a person of ordinary skill in the art that has been put forward by Dr. Tredennick in his declaration. I do not necessarily agree with the definition offered there, but I do not presently believe that the exact level of experience of a person of ordinary skill impacts my opinions offered herein.").

Based on the evidence of record, we adopt Dr. Tredennick's statement of the level of ordinary skill in the art with the exception of the language "at least." Thus, we determine that the skill level of a person of ordinary skill in the art would have been that of a person with a bachelor's degree in

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