UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

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Case IPR2017-01413
Patent 6,069,507

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Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Petitioner[1] filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 10, 11, 13, and 15 of U.S. Patent No. 6,069,507 (Ex. 1001, "the '507 patent"). We instituted trial only as to claims 13 and 15 on the sole alleged ground of anticipation by Kim.[2] Pet. 3. Subsequent to the Supreme Court's decision in *SAS Institute v. Iancu*, 138 S. Ct. 1348 (2018), we instituted trial on the remaining claims and grounds presented in the Petition. Paper 16. Thus, included for trial are claims 10, 11, 13, and 15 on the sole alleged ground of anticipation by Kim.

Prior to our adding claims 10 and 11 to the trial, Patent Owner[3] filed a Patent Owner Response (Paper 11, "PO Resp.") addressing only claims 13 and 15.[4] Ordinarily, arguments in a Preliminary Response do not carry automatically over to the Patent Owner Response. However, after we added claims 10 and 11 to the trial, we allowed Patent Owner to rely on its Preliminary Response (Paper 6) insofar as it addressed claims 10 and 11, and Patent Owner waived the opportunity to supplement its Patent Owner Response to address claims 10 and 11. Paper 19. Petitioner filed a Reply addressing all challenged claims and grounds. Paper 22 ("Reply"). Patent Owner filed a Sur-Reply. Paper 25 ("SR").

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[1] Samsung Electronics Co., Ltd.

[2] U.S. Patent No. 5,875,219.

[3] ProMOS Technologies, Inc.

[4] Patent Owner also submitted the declaration of Mr. Bill Gervasi in support of the Patent Owner Response. Ex. 2002.

Oral argument was consolidated for IPR2017-01412 and IPR2017-01413, and held on June 21, 2018. A transcript of the consolidated oral argument has been entered as Paper 32.

We find that Petitioner has shown by a preponderance of the evidence that each of claims 10, 11, 13, and 15 is unpatentable.

B.   Related Matters

Both Petitioner and Patent Owner have identified the following action as involving the '507 patent: *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.,* No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 5. Petitioner filed another petition for *inter partes* review of the '507 patent in IPR2017-01412. Petitioner further identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038; IPR2017-00039; and IPR2017-00040. Pet. 1–2. Patent Owner additionally identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01417, IPR2017-01418, and IPR2017-01419. Paper 5.

C.   The '507 Patent

The '507 patent relates to delay-locked loops (DLLs) and to reducing delay line length in DLLs. Ex. 1001, 1:7–9. The '507 patent notes that "[i]n order to achieve sufficient coverage of frequency ranges and guarantee desired resolution, DLLs generally require long delay lines." *Id.* at 1:14–18. Figure 1 is reproduced below:
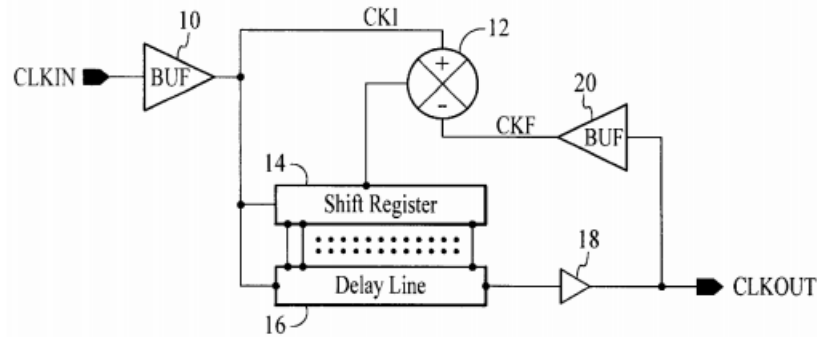
FIG. 1

(PRIOR ART)

Figure 1 illustrates a diagram of what the '507 patent regards as typical digital DLL according to the prior art. *Id.* at 2:24.

With respect to the prior art shown in Figure 1, input clock signal CLKIN is received at buffer 10 which provides a buffered clock signal CKI and which is coupled to phase detector 12, shift register 14, and delay line 16. *Id.* at 1:20–23. Delay line 16 is coupled to buffer 18 through which an output clock signal, CLKOUT, is produced. *Id.* at 1:23–25. The CLKOUT signal passes through buffer 20 to produce a feedback clock signal, CKF, to phase detector 12. *Id.* at 1:25–27. Phase detector 12 determines whether a phase difference exists between the buffered input signal CKI and feedback clock signal CKF. *Id.* at 1:27–29. The phase difference determines an appropriate shift in the buffered input clock signal via adjustment of shift register 14 to select sufficient delay via delay line 16. *Id.* at 1:29–32.

The '507 patent explains that there are several disadvantages with prior art type DDLs as clock speeds continue to increase. *Id.* at 1:34–36. To achieve high resolution and coverage of wide frequency ranges, the delay cells in delay line 16 and associated register cells in shift register 14 increase in number. *Id.* at 1:37–40. That expansion in length of the delay line leads

to larger silicon area requirements and higher power consumption, as well as longer lock-in time and larger frequency signal distortion. *Id.* at 1:43–47.

The '507 patent aims to overcome these disadvantages via the following disclosed method:

> [A] method for reducing delay line length in a digital delay locked loop (DLL) includes determining a phase difference between an input clock signal and a feedback clock signal, and maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°. The method also includes delaying the input clock signal to compensate for the phase difference, wherein a number of delay cells utilized is reduced by approximately one-half.

Id. at 2:3–11. In that regard, Figure 2 of the '507 patent is reproduced below:
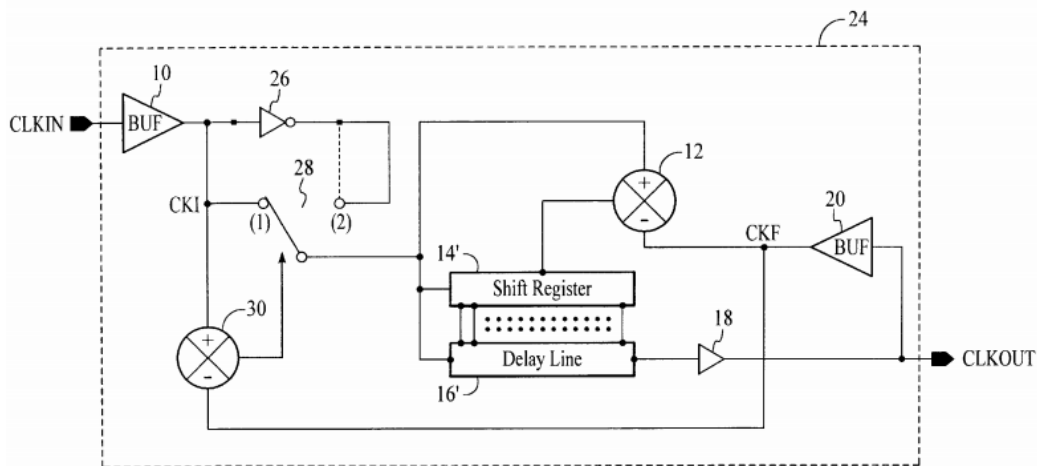

FIG. 2

Figure 2 illustrates a diagram of a DLL according to the '507 patent. *Id.* at 2:25–26. With respect to Figures 1 and 2, the '507 patent states that like components have been similarly numbered in the two figures. *Id.* at 2:49–51. As compared to the DLL of the prior art mentioned in the '507 patent, DLL 24 in Figure 2 of the '507 patent adds inverter 26, switch 28, and second phase detector 30. *Id.* at 2:55–57. According to the '507 patent, the length of delay line 16' and the corresponding number of cells in shift

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