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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01415
Patent 6,208,574 B1

Before JAMESON LEE, KEVIN F. TURNER, and MATTHEW J. McNEILL, *Administrative Patent Judges.*

McNEILL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

On May 12, 2017, Petitioner, Samsung Electronics Co. Ltd., filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 4–18 and 21–27 of U.S. Patent No. 6,208,574 B1 (Ex. 1001, "the '574 patent"). In an initial decision, we instituted *inter partes* review of each of the challenged claims. Paper 6 ("Dec. Inst.").

ProMOS Technologies Inc. ("Patent Owner") filed a Patent Owner Response (Paper 10, "PO Resp."), and Petitioner filed a Reply (Paper 12, "Reply").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued under 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that claims 4–18 and 21–27 of the '574 patent are unpatentable.

B. Related Matters

Petitioner concurrently filed a Petition challenging claims 1–3 and 30–37 of the '574 patent in IPR2017-001414. Pet. 1. Petitioner identifies U.S. Patent No. 6,088,270 ("the '270 patent") as related to the '574 patent. Pet. 2. Petitioner indicates that the '270 patent is the subject of *inter partes* review in IPR2017-00036. *Id*.

Petitioner indicates that Patent Owner asserted the '574 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:16-cv-00335-SLR-SRF (D. Del.). Pet. 1. Petitioner indicates Patent Owner has also asserted the following patents in that action: U.S. Patent Nos. 6,069,507; 6,172,554; 6,562,714; 7,375,027; and 6,559,044. *Id.* Petitioner concurrently filed IPR petitions challenging the other asserted

patents in the following *inter partes* review proceedings: IPR2017-01412, IPR2017-01413, IPR2017-01416, IPR2017-01417, IPR2017-01418, and IPR2017-01419. *Id.*

Petitioner also filed several IPR petitions involving patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Pet. 1–2. Petitioner identifies the following *inter partes* review proceedings for the patents involved in that suit: IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. *Id.*

C. The '574 Patent

The '574 patent relates to sense amplifiers in integrated circuit memories. Ex. 1001, 1:9–11. Integrated circuit memories often include a large number of memory cells set forth in a memory array. *Id.* at 1:14–15. Memory arrays are often organized into rows and columns. *Id.* at 1:35–36. Rows represent the memory cells located along a word line. *Id.* at 1:36–37. Columns are organized perpendicularly to the rows and represent the memory cells located along a bit line. *Id.* at 1:37–40. Generally, each column is connected to a sense amplifier. *Id.* at 1:40–41. In a large memory cell with thousands of columns and rows, the voltage that reaches sense amplifiers at different ends of the array may be appreciably different as a result of resistance along the lines, causing inefficient or slow operation. *Id.* at 2:15–39. The '574 patent relates to additional circuitry that may be connected to the sense amplifiers to alleviate these issues. *Id.* at 4:61–5:39.

One embodiment of the '574 patent is represented in Figure 5, which is reproduced below.

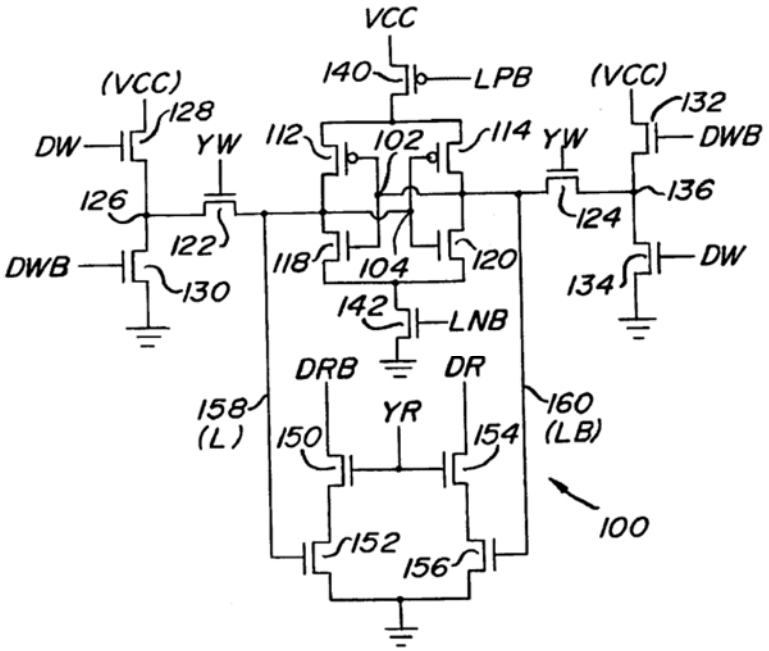

FIG. 5

Figure 5 depicts sense amplifier 100 having a latch formed by transistors 112, 114, 118, and 120. *Id.* at 6:6–9. Node 102 is coupled to the gate electrodes of P-channel transistor 112 and N-channel transistor 118. Node 102 is also coupled to the source-drain path of pass transistor 124. *Id.* at 6:28–31. Node 104 is coupled to the gate electrodes of P-channel transistor 114 and N-channel transistor 120. *Id.* at 6:9–13. Node 104 is also coupled to the source-drain path of pass transistor 122. *Id.* at 6:28–31. Pass transistors 122 and 124 are driven by column write select signal YW. *Id.* at 6:15–16.

Transistor 122 is coupled to node 126 between the source of local data write driver transistor 128 and the drain of local data write driver transistor 130. *Id.* at 6:32–35. Transistors 128 and 130 are N-channel transistors having their source-drain paths coupled in series. *Id.* at 6:35–36. The drain of transistor 128 is coupled to VCC and the source of transistor 130 is

coupled to ground. *Id.* at 6:36–38. Data write signal DW is coupled to the gate electrode of transistor 128, and its complement DWB is coupled to the gate electrode of transistor 130. *Id.* at 6:38–40. Transistors 132 and 134 on the opposite side of sense amplifier 100 have a similar arrangement, though DW and DWB are applied oppositely. *Id.* at 6:40–47.

Figure 5 also depicts local sense amplifier drive transistors 140 and 142. *Id.* at 7:16–18. Transistor 140 is coupled to the source electrodes of transistors 112 and 114. *Id.* at 6:53–55. The source electrode of transistor 140 is coupled to VCC (or LATCHP). *Id.* at 6:55–56. The gate of transistor 140 is coupled to LPB, which is the logical complement of LATCHP. *Id.* at 6:56–57. Transistor 142 is similarly configured with N-channel transistors 118 and 120, but the gate electrode of transistor 142 is coupled to signal LNB, the logical complement of LATCHN. *Id.* at 6:59–65.

The lower portion of Figure 5 also depicts a local column read amplifier comprising N-channel transistors 150, 152, 154, and 156. *Id.* at 6:66–7:1. The source-drain paths of transistors 150 and 152 are coupled in series, and the drain electrode of transistor 150 receives signal DRB, the logical complement of a data read signal DR. *Id.* at 7:1–4. The gate electrode of transistor 150 is coupled to column read signal Y_R. *Id.* at 7:7–8. The source electrode of transistor 152 is coupled to ground. *Id.* at 7:4–5. The gate electrode of transistor 152 is coupled to node 104. *Id.* at 7:5–7.

The source-drain paths of transistors 154 and 156 are similarly configured, being coupled in series between data read signal DR and ground on the right side of the figure. *Id.* at 7:8–10. The gate electrode of transistor 156 is coupled to node 102. *Id.* at 7:11–13.

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