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Paper 23
Entered: November 28, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01416
Patent 6,172,554 B1

Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges.*

TURNER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition for *inter partes* review of claims 1–3, 14–16, 22, and 28–36 of U.S. Patent No. 6,172,554 B1 (Ex. 1001, "the '554 Patent"). Paper 1 ("Pet."). We instituted review of all claims 1–3, 14–16, 22, and 28–36 on all grounds asserted in the Petition. Paper 7 ("Dec. on Inst."). ProMOS Technologies Inc. ("Patent Owner") filed a Patent Owner Response.[1] Paper 12. In response thereto, Petitioner filed a Reply. Paper 15. Oral hearing was held on August 16, 2018. A copy of the transcript for the oral hearing has been entered as Paper 22.

We determine that Petitioner has shown by a preponderance of the evidence that each of claims 1–3, 14–16, 22, and 28–36 is unpatentable.

A. Related Matters

The parties inform us that the challenged patent is the subject of a district court proceeding in the District of Delaware, captioned *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 4. In that action, Patent Owner has asserted other patents against Petitioner, and Petitioner has filed *inter partes* review petitions against those other patents in IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01417, IPR2017-01418, and IPR2017-01419. *Id.*

Petitioner also identifies these *inter partes* review proceedings, initiated by petitions filed by Petitioner, as involving additional patents

[1] Patent Owner also filed a declaration of Mr. Dhaval Brahmbhatt in support of the Patent Owner Response (PO Resp.). Ex. 2001.

asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:15-cv-00898-SLR-SRF (D. Del.): IPR2017-00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038; IPR2017-00039; and IPR2017-00040. Pet. 1–2.

B. The '554 Patent

The '554 Patent is titled "Power Supply Insensitive Substrate Bias Voltage Detector Circuit." Ex. 1001, [54]. The patent issued on January 9, 2001 from an application filed on September 24, 1998. *Id.* at [45], [22]. The patent is directed to "a circuit provid[ing] a bias voltage V1 which is substantially insensitive to variations of a power supply voltage powering the circuit." *Id.* at Abstract, 1:6.

The '554 Patent discloses that voltage generating circuits known as back-bias generators may be used in semiconductor devices which require the substrate region to be biased to a predetermined voltage, such as in dynamic random access memories (DRAM), where the substrate region is negatively biased to prevent the DRAM cells from losing stored information. Ex. 1001, 1:8–15. Such a back-bias generator includes a voltage multiplier circuit, commonly referred to as charge pump, for providing the negative Back-Bias Voltage (V_{BB}), and usually includes a V_{BB} detector circuit, which regulates the charge pump such that V_{BB} is maintained as close to a target V_{BB} value as possible. *Id.* at 1:15–21. The detector circuit constantly senses the V_{BB} voltage level, and if V_{BB} becomes more negative than the target V_{BB}, the detector circuit turns off the charge pump thereby allowing V_{BB} to drift back to the target V_{BB}; and if V_{BB} becomes less negative than the target

V_{BB}, the detector circuit turns on the charge pump to pump V_{BB} back to the target V_{BB}. *Id.* at 1:22–28.

A conventional V_{BB} detector circuit 17 is illustrated in Figure 1, reproduced below, along with Figure 3A illustrating an alternative, conventional V_{BB} detector circuit 37.

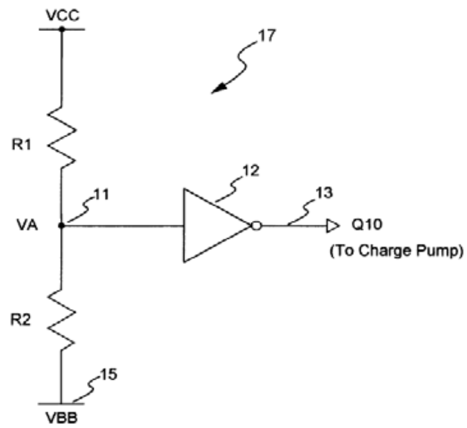

FIG. 1
(Prior Art)

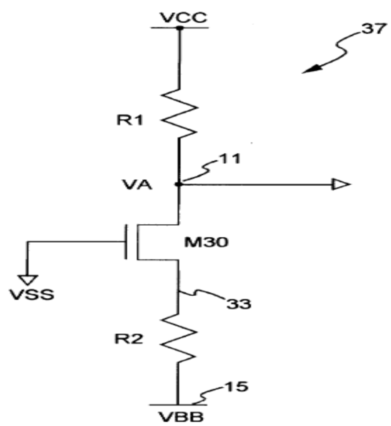

FIG. 3A
(Prior Art)

The conventional V_{BB} detector circuit 17, in Figure 1, has serially connected resistors R1 and R2 coupled between the power supply V_{CC} and V_{BB} terminal 15, where V_{CC} is provided by a power supply external to the device, and V_{BB} is generated internally by a charge pump, which is not shown. *Id.* at 1:29–33. Inverter 12 has its input terminal connected to node 11 which is the node between R1 and R2, and its output connected to the charge pump. *Id.* at 1:33–37.

Resistors R1 and R2 are selected so that the voltage V_A equals the trip point of inverter 12, such that if the charge pump causes V_{BB} to become more negative than the target value, V_A drops below the trip point of inverter 12, causing Q10 to go high. *Id.* at 1:43–49. The high level at Q10 turns off the charge pump, allowing V_{BB} to increase back to the target value. *Id.* Alternatively, if V_{BB} becomes less negative than the target V_{BB}, V_A rises above the trip point of inverter 12, causing Q10 to go low, which turns on the charge pump causing V_{BB} to become more negative. *Id*. at 1:49–54.

In Figure 3A (not reproduced here), the '554 Patent depicts another prior art detector circuit 37 that prevents V_{BB} from becoming positive. Circuit 37 is identical to circuit 17 of Figure 1 except that NMOS transistor M30 is connected between node 11 and R2, where that transistor causes the charge pump to turn on and pump V_{BB} to a more negative voltage. *Id*. at 2:29–37, Fig. 3A.

The '554 Patent details that the conventional circuits have drawbacks, including that V_{BB} varies with changes to V_{CC}, such that higher voltages can result in increases in junction leakage. *Id*. at 1:55–67. Also, the conventional circuits may not prevent V_{BB} from becoming positive, which can damage the device. *Id*. at 2:23–28. Because of these drawbacks, the '554 Patent discloses embodiments of V_{BB} detector circuits wherein V_{BB} is made insensitive to V_{CC} variations, and also wherein the range of possible V_{BB} values is increased without compromising power consumption. *Id*. at 2:56–59. Figures 4A and 5A are reproduced below:

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