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Paper 7
Entered: November 20, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01417
Patent 7,375,027 B2

Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108(b)

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I. INTRODUCTION

A. Background and Summary

On May 12, 2017, Petitioner[1] filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 1–10 of U.S. Patent No. 7,357,027 B2 (Ex. 1001, "the '027 patent"). Patent Owner[2] did not file a preliminary response. To institute an *inter partes* review, we must determine that the information presented in the Petition shows "that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Having considered the Petition and its supporting evidence, we determine that Petitioner has shown a reasonable likelihood that it would prevail in establishing the unpatentability of each of claims 1–10 of the '027 patent.

B. Related Matters

Both Petitioner and Patent Owner have identified the following action as involving the '027 patent: *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 4. In that action, Patent Owner has asserted other patents against Petitioner. Pet. 1. Petitioner has filed *inter partes* review petitions against those other patents in IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01418, and IPR2017-01419. Paper 4.

Petitioner identifies these *inter partes* review proceedings, initiated by petitions filed by Petitioner, as involving additional patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.,* No. 1:15-cv-00898-SLR-SRF (D. Del.): IPR2017-

[1] Samsung Electronics Co., Ltd.

[2] ProMOS Technologies, Inc.

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00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038; IPR2017-00039; and IPR2017-00040. Pet. 1–2.

C. The '027 Patent

The '027 patent is directed to the field of manufacturing semiconductor devices, and more particularly to opening a contact via to a surface of a material in a semiconductor device. Ex. 1001, 1:6–9. The '027 patent explains that a problem with preexisting method of opening a contact via to a surface of a material in a semiconductor device is that the semiconductor material at the bottom of the contact via is etched twice, thus subjecting that material to damage. *Id.* at 1:13–30. Specifically, the '027 patent describes that in the prior art, a first etching step is applied which goes through a photoresist layer down to the surface of the semiconductor material, subjecting the surface to the effects of etching once. *Id.* at 1:19–21. After the first etching step, a liner material is applied to the via and the surface of the semiconductor material within the via. *Id.* at 1:21–23. Then, an anisotropic etching step is performed to remove the liner material at the bottom of the aperture, which has the undesirable effect of subjecting the surface of the semiconductor material within the via to the effects of etching a second time. *Id.* at 1:23–37.

The '027 patent discloses a method of providing a contact via to a surface of a material that avoids the damaging effects of the second etching step in prior art techniques. *Id.* at 1:38–48. Specifically, the '027 patent describes:

> In one aspect of the invention, a contact via to a surface of a material is performed by forming a first dielectric layer on the surface, forming a second dielectric layer on the first dielectric layer, providing a first aperture which extends from a surface of the second dielectric layer toward the contact surface area of the

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> material for a distance which is less than a combined technique of the first and second dielectric layers. Next, a third dielectric layer is provided covering a surface of the aperture and an exposed surface of the first dielectric layer. A portion of the third dielectric layer and a portion of the first dielectric layer are removed to expose a portion of the contact surface area of the material.

Id. at 1:48–59.

Of all challenged claims, claim 1 is the only independent claim. Claim 1 is reproduced below:

> 1. A method of providing a contact via to a surface of a substrate, the method comprising:
>
> forming a first dielectric layer on the surface;
>
> forming a second dielectric layer on the first dielectric layer;
>
> providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the substrate for a distance which is less than a combined thickness of the first and second dielectric layers;
>
> providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer; and
>
> removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.

Ex. 1001, 4:17–32.

Notably, in the "providing a first aperture" step, the aperture does not extend all the way to the surface of the substrate because it starts at the surface of the second dielectric layer and extends for a distance that is less than the combined thickness of the first and second dielectric layers. The surface of the substrate is not exposed until the step of "removing a portion of the third dielectric layer and a portion of the first dielectric layer."

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Figure 3 of the '027 patent is reproduced below:

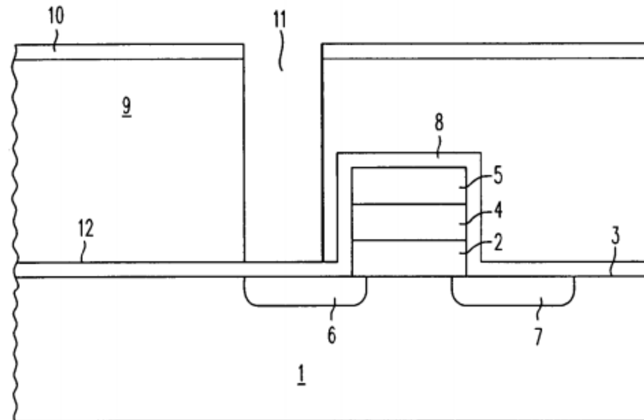

Figure 3 illustrates a cross-section of the semiconductor structure in the midst of contact via formation. Ex. 1001, 2:19–27. Protective layer 8 constitutes a first dielectric layer. *Id.* at 2:55–57. Reference numeral 9 designates a second dielectric layer that has been applied over first dielectric layer 8. *Id.* at 2:66–67. Initial via 11 has been etched through second dielectric layer 9 but does not extend through to the surface of semiconductor substrate 1. *Id.* at 3:3–6.

Figure 5 of the '027 patent is reproduced below:

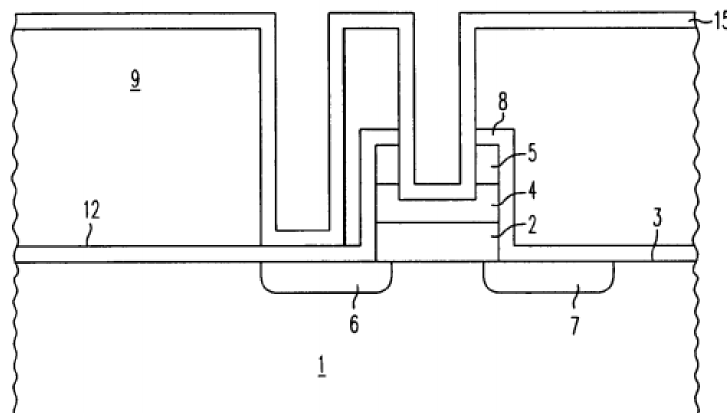

FIG. 5

Figure 5 illustrates the deposition of third dielectric layer 15 over the initial aperture and the exposed surface of the first dielectric

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