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Paper 33
Entered: November 27, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01418
Patent 6,559,044 B1

Before JAMESON LEE, KEVIN F. TURNER, and JOHN A. HUDALLA, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Petitioner[1] filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 1–23 of U.S. Patent No. 6,559,044 B1 (Ex. 1001, "the '044 patent"). We instituted review of claims 1–23 on all grounds asserted in the Petition. Paper 7 ("Decision on Institution"). Patent Owner[2] filed a Patent Owner Response.[3] Paper 13 ("PO Resp."). Petitioner filed a Reply.[4] Paper 19. An oral hearing was held on August 16, 2018. A copy of the transcript for the oral hearing has been entered as Paper 32.

Petitioner has shown, by a preponderance of the evidence, that each of claims 1–4, 6, 8–14, 16–18, and 20–22 is unpatentable. Petitioner has not, however, shown that any of claims 5, 7, 15, 19, and 23 is unpatentable.

B. Related Matters

Both Petitioner and Patent Owner have identified the following action as involving the '044 patent: *ProMOS Technologies, Inc. v. Samsung*

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[1] Samsung Electronics Co., Ltd.

[2] ProMOS Technologies, Inc.

[3] Patent Owner has not submitted objective evidence of nonobviousness, i.e., secondary considerations, for consideration. Patent Owner submitted the declaration of Mr. Dhaval Brahmbhatt in support of the Patent Owner Response. Ex. 2004.

[4] Patent Owner filed a paper styled as a "Motion to Exclude" (Paper 24), but the substance of the paper is actually a motion to strike. By way of explanation, a motion to exclude must be based on admissibility issues under the Federal Rules of Evidence, but Patent Owner's motion is not of that type. We informed the parties that Patent Owner's motion will be treated as a Motion to Strike. Paper 28. Petitioner filed an Opposition. Paper 29. The Motion to Strike is addressed in Section II.L. below.

Electronics Co., Ltd., No. 1:16-cv-00335-SLR (D. Del.). Pet. 1; Paper 4. In that action, Patent Owner also asserted other patents against Petitioner. Pet. 1. Petitioner has filed *inter partes* review petitions against those other patents in IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01417, and IPR2017-01419. Paper 4.

Petitioner also identifies these *inter partes* review proceedings, initiated by petitions filed by Petitioner, as involving additional patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:15-cv-00898-SLR-SRF (D. Del.): IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. Pet. 1–2.

C. The '044 Patent

The '044 patent pertains generally to a method for manufacturing a semiconductor device and particularly to a method for forming contacts in such a device. Ex. 1001, 1:7–9. The '044 patent describes that in a conventional process, (1) a plurality of active devices, such as transistors and memory cells, are formed over a semiconductor substrate, (2) one or more metal layers are formed over the active devices, and (3) contacts, through vias, serve to electrically connect certain active regions of the active devices to one of the metal layers. *Id.* at 1:19–25. With that background, the '044 patent states that it is desirable to reduce the number of required processing steps associated with forming an integrated circuit. *Id.* at 1:32–34. The '044 patent disclosure, however, does not articulate how the disclosed invention, relative to the prior art methods of manufacturing a

semiconductor device, reduces the number of required processing steps associated with forming an integrated circuit.

The '044 patent summarizes its invention as follows:

> In accordance with the invention, there is provided a method for manufacturing a semiconductor device that includes providing at least two active devices over a substrate, each of the active devices includes a gate electrode provided over a gate oxide, a silicide formed over the gate electrode, a cap formed over the silicide, and a pair of spaced-apart diffused regions formed in the substrate. The method also includes depositing a first layer of dielectric material over the substrate and active devices, providing a first photoresist over the first layer of dielectric material, defining and patterning the first photoresist, etching the first layer of dielectric material unmasked by the first photoresist to form a first opening, wherein the first opening exposes a first silicide of a first active device, removing the first photoresist, depositing a second layer of dielectric material over the first layer of dielectric material and in the first opening, providing a mask over the second layer of dielectric material, providing a second photoresist over the mask, defining and patterning the second photoresist, and forming a second opening and a third opening, wherein the second opening is aligned with the first opening and exposes the first silicide of the first active device, and the third opening exposes one of the pair of the spaced-apart diffused regions of a second active device.
>
> Also in accordance with the present invention, there is provided a method for forming contacts in a semiconductor device including a plurality of active devices over [ ] a substrate that includes depositing a first layer of dielectric material over the substrate and plurality of active devices, forming a first opening in the first layer of dielectric material, depositing a second layer of dielectric material over the first layer of dielectric material and in the first opening, providing a mask over the second layer of dielectric material, wherein the mask material is distinguishable over silicon oxides, and forming a second opening and a third opening in the second layer of dielectric material, wherein the second opening is aligned with the first opening and exposes a first silicide of a first active device, and

> the third opening exposes one of diffused regions of a second active device.

Id. at 1:40–2:12.

Figure 1D of the '044 patent is reproduced below:

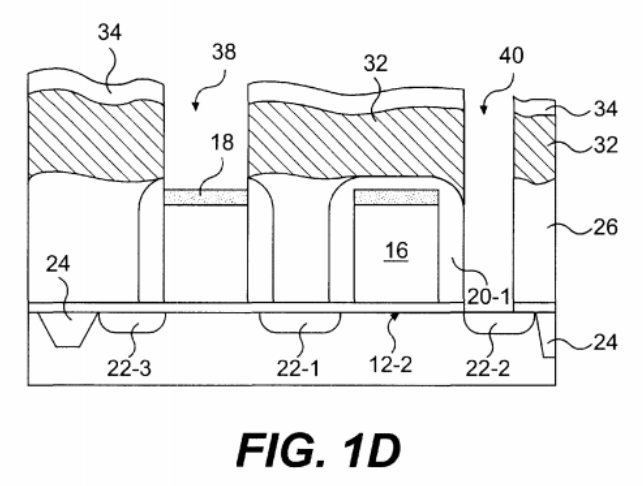

FIG. 1D

Figure 1D illustrates a cross-sectional view of the semiconductor structure at a point in the fabrication process after the formation of the second and third openings. *Id.* at 2:41–43, 3:66–4:6. The '044 patent states the following regarding Figure 1D:

> Referring to FIG. 1D, with hardmask 34 in place, an etching step is performed to form vertical openings 38 and 40. Vertical opening 38, aligned with vertical opening 30 shown in FIG. 1C, exposes silicide 18, and will later become a contact for gate electrode 16. Vertical opening 40 extends through to substrate 10, exposing diffused region 22-2, and will later become a contact for one of the source and drain regions of active device 12-2. In one embodiment, the etching step is a self-aligned contact step that forms vertical openings for gate and source/drain contacts of an active device at the same time. In addition, etchants for the etching step may be one of C_5F_8 or C_4F_8. Conventional semiconductor processes follow to fill vertical openings 38 and 40 with conductive materials to complete formation of contacts.

Id. at 3:66–4:12.

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