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Paper No. 10
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BROADCOM CORPORATION,
Petitioner,

v.

TESSERA, INC.,
Patent Owner.

Case IPR2017-01470
Patent 6,856,007 B2

Before BARBARA A. PARVIS, ROBERT J. WEINSCHENK, and STACY B. MARGOLIES, *Administrative Patent Judges*.

MARGOLIES, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Broadcom Corporation ("Petitioner") filed a Petition for *inter partes* review of claims 1, 11–13, 16, and 18 of U.S. Patent No. 6,856,007 B2 (Ex. 1001, "the '007 patent"). Paper 1 ("Pet."). Tessera, Inc. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

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Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented shows that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claim 18 of the '007 patent.

A. Related Matters

The parties identify the following matters in which the '007 patent has been asserted: (1) *In re Matter of Certain Semiconductor Devices, Semiconductor Device Packages, and Products Containing Same*, ITC Investigation No. 337-TA-1010 ("ITC 1010 Investigation")[1]; and (2) *Tessera, Inc. v. Broadcom Corporation*, Civil Action No. 1:16-cv-00379 (D. Del). Pet. 1–2; Paper 4, 1; *see* 37 C.F.R. § 42.8(b)(2).

B. The '007 Patent

The '007 patent, titled "High-Frequency Chip Package," describes as background that semiconductor chips used in cellular telephones and wireless data communication devices to process radio frequency (RF) signals "typically generate substantial amounts of heat." Ex. 1001, [54], 2:6–10. The '007 patent states that RF chips connections to a circuit board

[1] The preliminary record here is different from the record before the ALJ in the ITC 1010 Investigation, including different declarants providing testimony in support of Broadcom's unpatentability/invalidity contentions. *Compare* Pet. 15–53 (citing Ex. 1002 (Declaration of Dr. Suhling)), *with* Ex. 2001, 163–192 (citing Direct Witness Statement of Dr. Lall).

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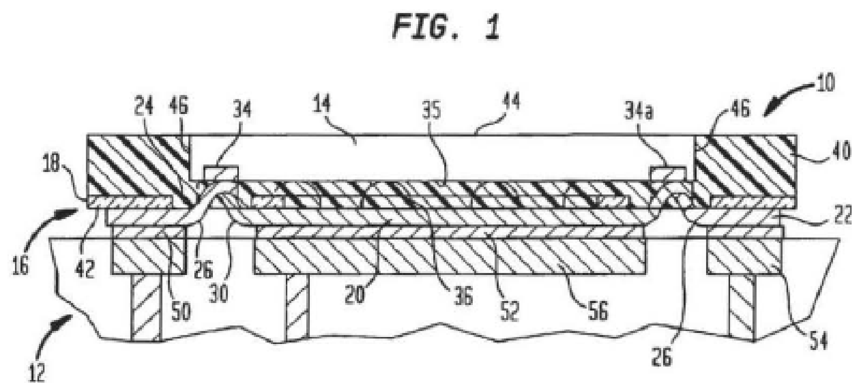
"should be made with low-inductance leads having controlled, predictable impedance at the frequencies handled by the chip." *Id.* at 2:10–15. The '007 patent also states that "it would be desirable to provide packages which are particularly well suited to RF chips using the same production equipment and techniques used with other package designs." *Id.* at 2:17–20.

The '007 patent describes "a chip carrier having a large thermal conductor which can be solder-bonded to a circuit board so as to provide enhanced thermal conductivity to the circuit board and electromagnetic shielding" and "a conductive enclosure which partially or completely surrounds the packaged chip to provide additional heat dissipation and shielding." *Id.* at Abstract. Figure 1 of the '007 patent, below, illustrates a sectional view of an embodiment of the chip assembly:



Id. at 7:14–15. As illustrated in Figure 1 above, the chip assembly includes packaged chip 10 mounted to circuit board 12. *Id.* at 7:16–17. Packaged chip 10 includes die 14 and chip carrier 16. *Id.* at 7:17–18. According to the '007 patent, chip carrier 16 "has a large metallic thermal conductor 20 in a central region and a plurality of terminals 22 in a peripheral region surrounding the central region." *Id.* at 7:23–26. The patent discloses that each terminal 22 has a terminal lead 26 associated with it and that "[t]he

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terminals, leads and thermal conductor form an electrically continuous structure." *Id.* at 7:28–29, 7:48–49.

The '007 patent states that "[t]he packaged semiconductor chip is provided with thin layers of solder 50 on the terminals 22, 22*a* and with a thin layer of solder 52 on thermal conductor 20." *Id.* at 9:48–50; *see id.* at Fig. 2 (showing terminals 22, 22a). According to the '007 patent, "[d]esirably, the solder layers are less than about 75 microns thick, most preferably between 20 and 50 microns thick." *Id.* at 9:53–55.

The '007 patent states that, "using conventional surface-mounting soldering techniques, the terminals are soldered to the contact pads 54 of the circuit board, whereas the thermal conductor 20 is soldered to the thermal conductor mounting 56 of the circuit board." *Id.* at 9:61–65. The patent adds that "[m]ost preferably, the bond between the thermal conductor and the thermal conductor mounting covers substantially the entire surface area of the thermal conductor, as, for example, at least 80% of the thermal conductor surface area." *Id.* at 9:65–10:2. The '007 patent states that "the bond between the thermal conductor 20 and the thermal conductor mounting of the circuit panel 12 . . . covers a substantial area and thus has substantial strength and fatigue resistance." *Id.* at 9:40–44.

C. Illustrative Claims

Claims 1, 11, 12, and 18 are illustrative of the subject matter of the challenged claims and read as follows:

> 1. A packaged semiconductor chip comprising:
>
> (a) a first semiconductor chip having a front face, a rear face, edges bounding said faces and contacts exposed at said front face; and

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(b) a chip carrier having inner and outer surfaces, the inner surface of said chip carrier facing in an upward direction toward said chip, said chip carrier having a plurality of terminals and a metallic thermal conductor having a unitary solder-wettable area exposed at said outer surface, said unitary solder-wettable area having an area larger than the area of each of said terminals, said thermal conductor being at least partially aligned with said chip, at least some of said terminals being electrically connected to at least some of said contacts of said chip.

11. An assembly comprising

a packaged chip as claimed in claim 1,

a circuit panel having contact pads and a thermal conductor mounting, and

a unitary layer of solder bonded to said thermal conductor mounting,

said chip carrier being disposed on said circuit panel with said outer face of said chip carrier facing downwardly toward said circuit panel, said terminals of said chip carrier being connected to said contact pads of said circuit panel,

wherein substantially all of said unitary solder-wettable area of said thermal conductor of said chip carrier is bonded by said unitary layer of solder to said thermal conductor mounting of said circuit panel.

12. A packaged chip as claimed in claim 1, further comprising *a unitary layer of solder* covering substantially all of said unitary solder wettable area.

18. A packaged semiconductor chip comprising:

(a) a first semiconductor chip having a front face, a rear face, edges bounding said faces and contacts exposed at said front face;

(b) a chip carrier having inner and outer surfaces, the inner surface of said chip carrier facing in an upward direction toward said chip, said chip carrier having a plurality of terminals and a metallic thermal conductor exposed at said outer surface, said thermal conductor having area larger than the area of each of said

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